

# Current-limiting and ultrafast system for the characterization of Resistive Random Access Memories

J. Diaz-Fortuny\*, M. Maestro, J. Martin-Martinez, A. Crespo-Yepes, R. Rodriguez, M. Nafria and X. Aymerich  
Departament d'Enginyeria Electrònica, Universitat Autònoma de Barcelona (UAB), Bellaterra, Spain  
\*Corresponding author: javier.diaz@uab.es

**Abstract**— A new system for the ultrafast characterization of Resistive Switching phenomenon is developed to acquire the current during the Set and Reset process in a microsecond time scale. A new electronic circuit has been developed as a part of the main setup system, which is capable of (i) applying a hardware current limit ranging from nanoampers up to miliampers and (ii) converting the Set and Reset exponential gate current range into an equivalent linear voltage. The complete system setup allows measuring with a microsecond resolution. Some examples demonstrate that, with the developed setup, an in-depth analysis of Resistive Switching phenomenon and Random Telegraph Noise can be made.

**Keywords**—Resistive switching, Resistive Random Access Memories (RRAM), Random telegraph noise, ultrafast measurement.

## I. INTRODUCTION

Resistive Random Access Memories (RRAM) have become one of the most promising candidates for the next generation non-volatile memories. They are based on Resistive Switching (RS) phenomenon [1-3] that, in metal-insulator-metal (MIM) and metal-insulator-semiconductor (MIS) structures, consists in the voltage-controlled resistance change of the dielectric. Two processes allow the resistance changing between two states: firstly the Set process, which provokes the change from High Resistance State (HRS) to Low Resistance State (LRS) and, secondly, the Reset process, that provokes the opposite change, from LRS to HRS. The value of the resistance that characterizes each state can differ in several orders of magnitude. In some materials, both states, LRS and HRS, are associated to a Conductive Filament (CF) through the dielectric that is fully formed at LRS and partially destroyed at HRS [4-6]. The destruction/formation of the CF (i.e., switching between states) which can be observed as a sudden event, can be achieved by a proper biasing of the device (Fig. 1). To allow Set/Reset cycling, it is crucial to impose a limit to the current that flows through the device during the Set process, otherwise the CF cannot be destroyed again being impossible to achieve the HRS anymore. It is worth point out that instabilities in the form of Random Telegraph Noise (RTN) can be observed during the HRS, with time constants that can be in the seconds range time scale [7-8].

Typically, semiconductor parameter analyzers are used to obtain the current-voltage characteristics linked to the RS phenomenon, and the current limit is imposed by the instrument itself. However, most of the semiconductor analyzers' mainframes have a low sampling rate of 10ms (depending on the current range to be measured), so that relevant information of the Set and Reset processes could be lost. Optional ultrafast modules can be added to get sampling rates down to 10ns, but at the expense of a considerable cost increase [9-10]. Moreover, sometimes the procedure to limit the current is unclear when a semiconductor analyzer is used, so that the correct interpretation of the results becomes difficult.

As an alternative, in this work, a low-cost experimental setup, capable of capturing fast current transients (with more than 1sample/10 $\mu$ s) and which also includes a current limitation module, is presented. After a detailed explanation of the setup, its use to the ultrafast characterization of the Set and Reset processes in RRAM is shown. Finally, we show other applications of the proposed setup, such as an ultrafast characterization of Random Telegraph Noise (RTN) at the HRS of RS devices [11-14].

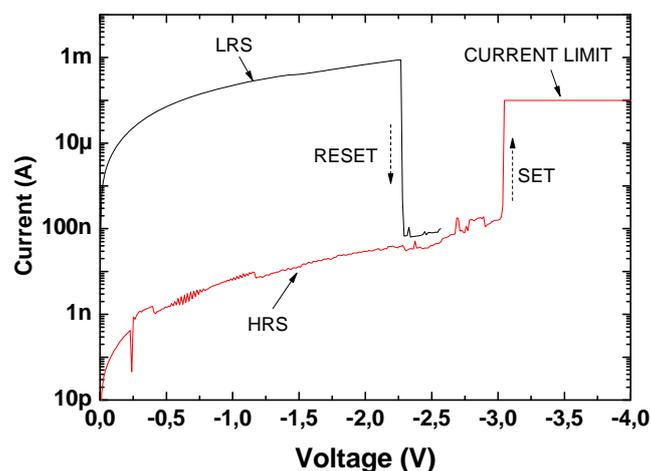


Figure 1. Typical I-V characteristics recorded during a Resistive Switching cycle. Set and Reset events are indicated, as well as the current limit level during Set and the LRS and HRS currents.

## II. DESING OF THE CIRCUIT

The scheme of the designed experimental setup is presented in Fig. 2. A voltage signal ( $V_{app}$ ) is applied to one of the terminals of the device under test (DUT). In this work, the voltage has been applied using a Source Measure Unit (SMU) in a semiconductor parameter analyzer, which also allows measuring the current through this terminal. The current measured with the SMU will be compared to that at the output of the developed setup. Though a SMU has been used in our case, any instrument capable of applying voltage signals can be connected to this terminal, providing a high versatility to the experiments that can be performed with this setup. The other terminal of the DUT is connected to a high impedance buffer and to the current limit control unit (CLCU). The goal of the buffer is to measure the voltage at the other DUT terminal, so that the actual voltage drop at the DUT can be obtained. The CLCU allows the user to tune, using a hardware approach, the required current limit, in order to avoid the sample destruction. One tunable input ( $V_{control}$ ) on the CLCU allows the user to set a suitable current limit for each measurement during the Set process and a very high current limit for the Reset process. The output of the CLCU is connected to a logarithmic current-to-voltage converter (Log-IVC) which converts the current into an equivalent voltage at the output stage. This type of conversion allows measuring the complete range of the input current during the process. The corresponding output voltage of the Log-IVC is derived to a digital storage oscilloscope (DSO). The DSO trigger level is adjusted to acquire the data at the precise moment that the Set and Reset events occur, with a resolution of microseconds.

The CLCU circuit diagram is shown in Fig. 3. The current limit level in the DUT is controlled by fixing the current through the T1 MOSFET, which is connected in series with the DUT. This is done by applying a fine-controlled voltage ( $V_A$ ) to its gate. This voltage is selected with the aid of the OPAMP configuration in Fig. 3. The values of R2 and R5 are selected during the initial configuration phase so as to provide a T1 gate voltage suitable for the minimum value of the current limit (100nA in our case). The user can increase the current limit, up to 10mA, by simply tuning  $V_{control}$  (see Fig.4b).

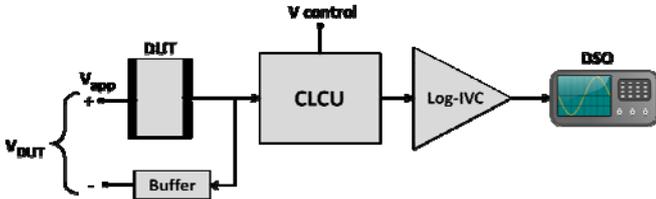


Figure 2. Block diagram of the developed setup.

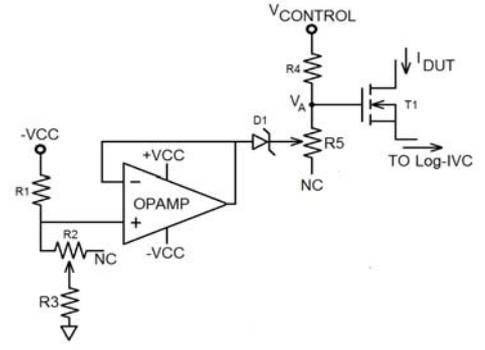


Figure 3. CLCU circuit schematics.

To check the CLCU operation, a resistance of 10k $\Omega$  has been connected as DUT.  $V_{app}$  has been ramped, different  $V_{control}$  values have been considered (to change the current limit) and the voltage drop at DUT ( $V_{DUT}$ ) has been measured. Figure 4 (left) shows  $V_{DUT}$  as a function of  $V_{app}$  for four different  $V_{control}$ . Note that depending on the  $V_{control}$  value, the CLCU limits  $V_{DUT}$  so that a maximum current flowing through the device is not exceeded. The dependence of the current limit imposed by the CLCU on  $V_{control}$  is presented in Fig.4 (right). A large range, from 100nA to 10mA, can be achieved using this method, which is enough for a correct formation of the CF, independently of the instrumentation used to apply voltage to the DUT. The output of the CLCU is connected to the Log-IVC and the final signal is captured with the DSO, allowing the registration of the information with sampling rate of  $\sim 1\text{sample}/10\mu\text{s}$ . Note that larger sampling rates could be obtained if a high-performance DSO was used for the measurements.

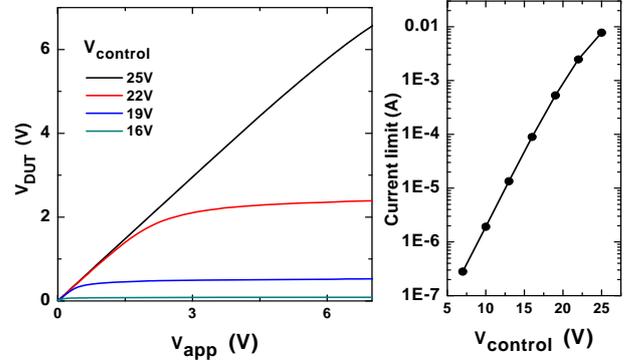


Figure 4. (left)  $V_{DUT}$  at a function of  $V_{app}$ , for four different  $V_{control}$ . The CLCU adjusts the voltage drop on the device so that the current limit, whose value depends on  $V_{control}$ , is not exceeded. Right: a large range of current limit values can be achieved by simply using the  $V_{control}$  input. These measurements were performed using a 10k $\Omega$  resistor as DUT.

## III. EXPERIMENTAL RESULTS.

To check the operation of the system described previously, some experimental results are presented. To show the advantages of the developed setup when compared to traditional systems, firstly, the Set and Reset processes of

RRAM are characterized. Secondly, RTN traces are measured, demonstrating that more details of these events can be revealed using our setup.

The samples used were MIS (metal-insulator-semiconductor) capacitors with 200nm thick Ni top metal electrode, a 20nm thick HfO<sub>2</sub> layer and, as bottom electrode, an n-type silicon substrate. To perform all the measurements, the setup shown in Fig. 2 was employed. For comparison, the currents were simultaneously measured with a SMU.

### A. Set and Reset events

As it is well-known, Set and Reset are events that can occur “instantaneously” or at least in a time scale so short that it is very difficult to measure what it is actually happening. Using the circuit described in this work, it is possible to get more details and more information on these events.

In Fig. 5 the current captured by the SMU is shown as a function of the stress voltage applied to the DUT electrode ( $V_{app}$ ). To limit the current during the Set process to 0.1mA the CLCU was used. At a certain voltage, around 2.6V, the change from the HRS to LRS is observed as an abrupt increase of the current, with no intermediate steps. However, in the inset of Fig. 5, which is a capture of the same event measured by the DSO, it can be observed that different current instabilities occur during the Set. In this case the capture with the DSO was configured to get 2500 current values in 25ms, i.e. a sample every 10 $\mu$ s, around the Set event, in contrast to 2 or 3 samples that can be obtained with a typical SMU in the same timeframe. Note that some current changes are observed with the proposed setup, whereas they are hidden when the SMU is used. Another important point is that, whereas the SMU shows the current vs the applied voltage, our setup measures the current vs time and  $V_{DUT}$  (the actual voltage drop on the device) can be also registered (from the buffer output). Therefore, our setup shows not only the voltage dependence of the current, but also its evolution during the transient, with a large time resolution.

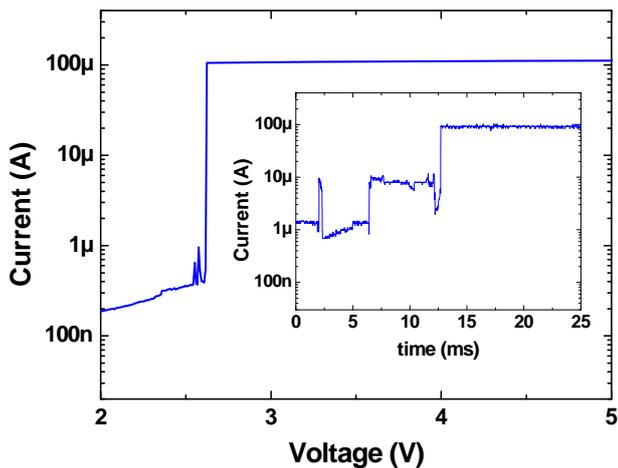


Figure 5. Set process in a MIS structure measured by a conventional SMU. Inset: The same event measured with the proposed setup.

Equivalent pictures can be obtained for the Reset process (no current limit is needed in this case, so that it is effectively removed by setting this value to 10mA). In Fig 6, the gate current as a function of the voltage applied is displayed. The main figure shows the I-V curve measured with the SMU, whereas the inset depicts the I-t trace measured with our setup. The main figure shows that the current initially increases as voltage increases, but at certain value of the voltage (1.6V) the current drops abruptly around three orders of magnitude. This corresponds to the Reset process (i.e. switch from the LRS to HRS). Note that in this case, just before the Reset, a current spike is observed. If the SMU is used, this event is only registered in two sampling values, therefore typical measurements of Reset process barely provides enough information about it. The inset in the Fig. 6 corresponds to the same event captured by the DSO, where the Reset process is registered with high time resolution. In this figure, the rapid increase of the current before the Reset event can be seen with much more detail, allowing a better study of this particular phenomenon. Therefore, when the setup aforementioned is used to measure the LRS and HRS change more information is registered. Furthermore, although the current drop during the Reset also occurs abruptly, it is possible to observe intermediate phenomena during this drop adjusting the time scale and measuring it in shorter intervals.

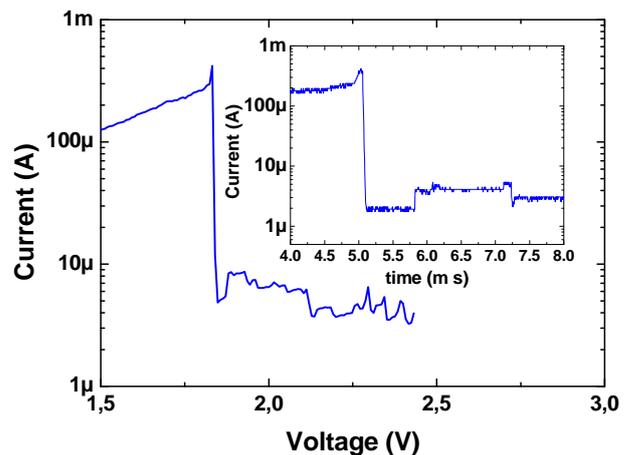


Figure 6. Reset process measured by SMU. Inset: The same Reset process measured with our system.

### B. Random telegraph noise at HRS

As shown previously, the fast sampling rate of the developed setup allows measuring very fast events that could be hidden when using a SMU. To further show this point, RTN signals have been measured. To observe RTN signals on the current through the DUT, a constant voltage was applied to the top electrode, once the sample was switched to the HRS state. The current through the dielectric was collected at the top electrode by the SMU, getting the RTN signal in Fig. 7 (top). Figure 7 (middle) is a zoom of the top figure between 46.8 s and 47.6s, where we can see that in that time interval, the SMU only has captured nine current values, i.e. one event every 0.1s, and no apparent RTN occurs. However, in Fig. 7 (bottom), which shows the capture with the DSO, a RTN

signal appears in a time interval equivalent to 0.25s (in the timeframe within the red bars in Fig. 7 middle). This is because of the ability of DSO to measure 2500 points per capture, i.e. a sample every 100 $\mu$ s, so that the presence of a RTN signal is revealed in the time period where the SMU showed a constant current. Then, the great advantage of using the circuit lies on the fact that, by properly selecting the time scale of the DSO events can be measured with a large time resolution, events that would not appear in SMU's measurements.

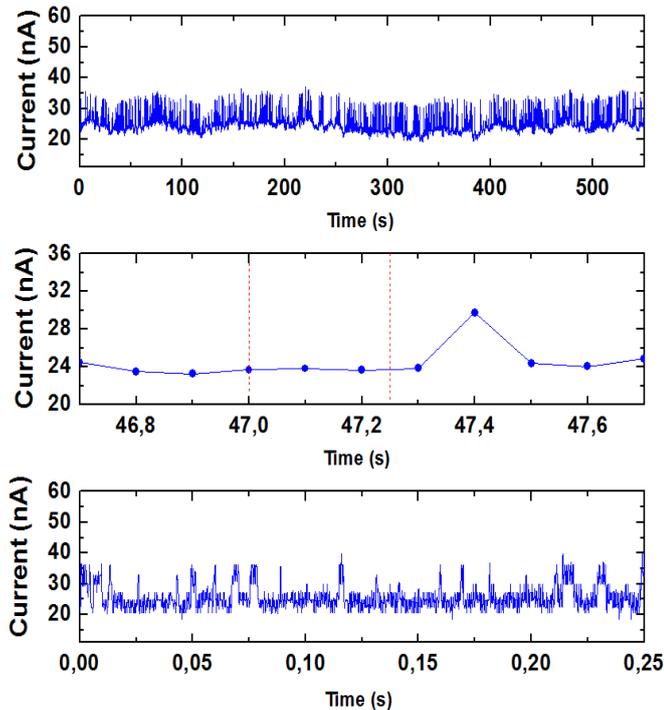


Figure 7. Top: RTN signal measured with a SMU in a time interval of 550s. Middle: Zoom of 0.25s in the previous signal. Bottom: RTN signal of 0.25s duration acquired by circuit. This time interval corresponds to the interval between red dashed lines in the figure in the middle.

#### IV. CONCLUSIONS

A complete understanding of the Resistive Switching phenomenon is needed to advance in the development of RRAM devices, which must be gained from its characterization. However, typical characterization systems show several limitations, such as a too low sampling rate and a not fully understood current limitation mechanism. To overcome these problems, in this work, a low cost setup has been developed with the aim of characterizing the RS phenomenon, which provides (i) a large time resolution (more than 1 sample/10 $\mu$ s), and (ii) a precise current limitation circuit with a large dynamic range (100nA-10mA). To show the capabilities of the setup, the Set and Reset processes in RRAM have been measured in the time domain, revealing current instabilities which are hidden when using conventional instrumentation. Additionally, Random Telegraph Noise (RTN) at the High Resistive State (HRS) has been measured in a time scale where traditional instrumentation shows

constant currents. In summary, the characterization system presented in this work is a low-cost solution that can highlight details of the processes involved in RRAM, which can be relevant to their accurate modeling. Though the system performance has been demonstrated through measurements on RRAM, it can be also used for the characterization of other electron devices.

#### ACKNOWLEDGMENT

This work has been partially funded by the Spanish MINECO (TEC2010-16126 and TEC2013-45638-C3-R), the Generalitat de Catalunya (2014 SGR 384). The authors would also like to thank IMB-CNM for sample provision.

#### REFERENCES

- [1] W. Rainer, R. Dittmann, G. Staikov, and K. Szot. "Redox-Based Resistive Switching Memories – Nanoionic Mechanisms, Prospects, and Challenges." *Advanced Materials* 21, no. 25–26, July 13, 2009.
- [2] The international Technology Roadmap for Semiconductors – ITRS 2013 Edition Emerging Research Devices (<http://www.itrs.net>), 2013.
- [3] F. Yoshii. "Review of Emerging New Solid-State Non-Volatile Memories." *Jap. Journal of Appl. Physics* 52, no. 4R, April 1, 2013.
- [4] J. Suñe, E. Miranda, D. Jimenez, S. Long, and M. Liu. "From Dielectric Failure to Memory Function: Learning from Oxide Breakdown for Improved Understanding of Resistive Switching Memories." *NVMTS, 2011 11th Annual*, 1–6, 2011.
- [5] S. Akihito. "Resistive Switching in Transition Metal Oxides." *Materials Today* 11, no. 6, June 2008.
- [6] R. Waser and M. Aono. "Nanoionics-Based Resistive Switching Memories." *Nature Materials* 6, no. 11, November 2007.
- [7] D. Veksler, G. Bersuker, B. Chakrabarti, E. Vogel, S. Deora, K. Matthews, D. C. Gilmer, H-F. Li, S. Gausepohl, P. D. Kirsch. "Methodology for the statistical evaluation of the effect of random telegraph noise (RTN) on RRAM characteristics" *Electron Devices Meeting (IEDM), 2012 IEEE International*, 2012.
- [8] D. Veksler, G. Bersuker, L. Vandelli, A. Padovani, L. Larcher, A. Muraviev, B. Chakrabarti, E. Vogel, D. C. Gilmer, P. D. Kirsch. "Random telegraph noise (RTN) in scaled RRAM devices". *Reliability Physics Symposium (IRPS), 2013 IEEE International*. MY.10.1 - MY.10.4, 2013.

- [9] KEYSIGHT TECHNOLOGIES, “Characterizing Random Noise in CMOS image sensors, RTS noise measurements using the B1500A’s WGFMU module”. Application Note, July 31, 2014, 5990-3705EN, available at [www.keysight.com](http://www.keysight.com).
- [10] KEITHLEY, “Ultra-Fast I-V Applications for the Model 4225-PMU Ultra-Fast I-V Module.”, July 2, 2012, available at [www.tek.com/keithley](http://www.tek.com/keithley).
- [11] N. Raghavan, R. Degraeve, L. Goux, A. Fantini, D.J. Wouters, G. Groeseneken, and M. Jurczak. “RTN Insight to Filamentary Instability and Disturb Immunity in Ultra-Low Power Switching HfOx and AlOx RRAM.” In 2013 Symposium on VLSI Technology (VLSIT), T164–T165, 2013.
- [12] S. Choi, Y. Yang, and Wei Lu. “Random Telegraph Noise and Resistance Switching Analysis of Oxide Based Resistive Memory.” *Nanoscale* 6, no. 1, December 9, 2013.
- [13] S. Balatti, S. Ambrogio, A. Cubeta, A. Calderoni, N. Ramaswamy, and D. Ielmini. “Voltage-Dependent Random Telegraph Noise (RTN) in HfOx Resistive RAM.” In RPS, 2014 IEEE International, MY.4.1–MY.4.6, 2014.
- [14] F. M. Puglisi, P. Pavan, A. Padovani, and L. Larcher. “A Study on HfO2 RRAM in HRS Based on I–V and RTN Analysis.” *Solid-State Electronics*. Accessed July 25, 2014.