Design of Integrated Systems for Digital Processing 2015/2016

Code: 43344
ECTS Credits: 6

Degree	Type	Year	Semester
4314660 Computer Engineering	OB	1	2

Contact

Name: Jordi Carrabina Bordoll

Email: Jordi.Carrabina@uab.cat

Use of languages

Principal working language: english (eng)

Teachers

Lluís Antoni Teres Teres

David Castells Rufas

Prerequisites

Knowledge on the following subjects is recommented:

Digital Sistemes and Hardware Description Languages
Electronic Systems Design
Computer Architecture
Parallel Programming

Objectives and Contextualisation

The main objective of this course is to learn, understand and be able to design electronic systems with the focus on embedded systems. These systems are composed of integrated circuits that manage their capacity of computation and communication through wired or wireless protocols. The study of these integrated systems will be oriented to the usual digital processing archtiectures in modern electronics: single-core (i.e. wireless sensor networks), multi-core (i.e. multimedia devices) and many core (high performance computing), and the different types of computation: data-flow and reactive. Application-oriented real and virtual platforms will be presented as the main design strategies for HW/SW co-design. We will review the different fabrication technologies available in the market, from silicon technologies to new processes for organic and flexible electronics, and we will use FPGA platforms to implement such systems in the labs.

Skills

- Communicate and justify conclusions clearly and unambiguously to both specialised and non-specialised audiences.
- Communicate orally and in writing in English.
- Define and communicate results, guaranteeing high levels of performance and quality.
- Design and develop computer systems, applications and services in embedded and ubiquitous systems.
- Integrate and apply the knowledge acquired and solve problems in new or little-known situations within broader (or multidisciplinary) contexts.

- Integrate knowledge and use it to make judgements in complex situations, with incomplete information, while keeping in mind social and ethical responsibilities.
- Launch, lead and manage manufacturing processes for computer hardware, safeguarding persons and goods and overseeing product quality and certification
- Responsibly manage information and knowledge when leading multidisciplinary groups and/or projects.
- Solve problems in new or little-known situations within broader (or multidisciplinary) contexts related to the field of study.
- Understand and apply ethical responsibility, legislation and codes of practice to professional activity in computer engineering.

Learning outcomes

1. Communicate and justify conclusions clearly and unambiguously to both specialised and non-specialised audiences.
2. Communicate orally and in writing in English.
3. Define and communicate results, guaranteeing high levels of performance and quality.
4. Design application-specific integrated circuits (ASICs)
5. Design integrated circuits on the basis of hardware description languages implemented by application-specific integrated circuits (ASICs) and/or FPGAs.
6. Integrate and apply the knowledge acquired and solve problems in new or little-known situations within broader (or multidisciplinary) contexts.
7. Integrate knowledge and use it to make judgements in complex situations, with incomplete information, while keeping in mind social and ethical responsibilities.
8. Know the hardware description languages for highly complex circuits.
9. Launch, lead and manage manufacturing processes for computer hardware, safeguarding persons and goods and overseeing product quality and certification
10. Responsibly manage information and knowledge when leading multidisciplinary groups and/or projects.
11. Solve problems in new or little-known situations within broader (or multidisciplinary) contexts related to the field of study.
12. Understand and apply ethical responsibility, legislation and codes of practice to professional activity in computer engineering.
13. Use digital programmable logic devices.

Content

1. Introduction to the Design of Integrated Systems for Digital Processing
Main concepts on Embedded Systems
Models of Computation
Design and Technology Evolution in Silicon Microelectronics

2. Technologies and Design Methodologies for Integrated Circuit Design
Electronic Design Automation Tools
(Seminar on microelectronic design)
(Seminar on algorithms of EDA tools)
Introduction to VHDL
VHDL Modeling, simulation and synthesis
ASIC and FPGA Implementation

4. Systems-on-a-Chip Design
Physical and Virtual (IPs) Components
SoC Architectures
Performance and Power
Design Space Explotarion

4. Embedded Platforms
Selection Criteria
Mechanical formats

Communication Subsystems
Standardization and certification

5. Complex Systemes and Applications
Introduction to NoCs and MPSoCs
Programming models for embedded multi-core systems
Introduction to SystemC/TLM

Laboratori: Processament Digital Integrat sobre FPGA

Methodology

The course will be mainly driven by the lectures, that will use adhoc material (presentations and documents) available in the virtual campus of the UAB.

Two seminars are schedulled and others can also be added, according to the parallel activity at UAB, in order to analyse in depth specific topics.

Laboratory work will let the students to apply and experiment the concepts acquired on FPGA platforms widelly used in industry.

According to the personal interests of every student, a scientific and/or technologic paper will be selected in order to get familiar and evaluate the knowledge that is available through specialized journals and publications.

Activities

Title	Hours	ECTS	Learning outcomes
Type: Directed			
Laboratory Sessions	15	0.6	2, 3, 8, 5, 10, 11, 1, 7, 6, 13
Lectures	26	1.04	2, 3, 8, 5, 4, 10, 11, 1, 7, 6, 12, 9, 13
Thematic Seminars	4	0.16	2, 3, 10, 11, 7, 6, 9
Type: Supervised			
Selection and follow-up of a selected scientific and/or technologic paper	12	0.48	2, 3, 10, 11, 1, 7, 6, 12
Type: Autonomous			
Preparation of laboratory activities	10	0.4	8, 5, 11, 7, 6, 13
Study	65	2.6	8, 5, 4, 10, 11, 7, 6, 12, 13

Evaluation

Evaluation is based on:

• 2 parcial exams containign both theoretical concepts and exercices. M;inimum mark on those exams is 3 (over 10)

• Team work at lab scheduled in 5 sessions with the need to deliver the corresponding reports (delivered individually). This is mandatory to pass the course evaluation.

• Individual work on the critical review of a specific scientific and/or technological paper

A method to recover failed parcial exams will be provided.

Any change on the above evaluation method will be communicated in advance

Evaluation activities

Title	Weighting	Hours	ECTS	Learning outcomes
Critical review of a personalized scientific-Technologic paper	15%	10	0.4	2, 10, 11, 1, 7, 6
Laboratory work reports	35%	5	0.2	2, 3, 8, 5, 10, 1, 7, 13
1st Parcial Exam	25%	2	0.08	2, 3, 8, 5, 4, 10, 11, 1, 7, 6, 12, 9, 13
2nd parcial exam	25%	1	0.04	2, 3, 8, 5, 4, 10, 11, 1, 7, 6, 12, 9, 13

Bibliography

L. Terés, Y. Torroja, S. Olcoz, E. Villar: "VHDL: Lenguaje estándar de diseño electrónico".

P. Bricaud, M. Keating "Reuse Methodology Manual for System-On-A-Chip Designs".

R. Rajsuman "System-on-a-Chip: Design and Test".

I. Grout "Digital Systems Design with FPGAs and CPLDs.

F. Balarin et al.: "Hardware-Software Co-Design of Embedded Systems: The POLIS Approach".