Linear Models for Diode Surface Mount Packages

Application Note 1124

Introduction

When linear or non-linear analyses are performed on diode circuits, both the diode chip and its package must be accurately modeled. The diode chip or die itself may be modeled using SPICE parameters, or by a three element linear model as shown in Figure 1.

The three-lead SOT-23 and SOT-323 packages may be modeled as shown in Figure 2. The element values are given in Table 1.

The four-lead SOT-143 package is modeled as shown in Figure 3, with circuit element values given in Table 1.

The six-lead SOT-363 package is described in Figure 4 with element values specified in Table 1.

Note that two package linear equivalent circuits exist for the SOT-3x3 packages. One provides accurate modeling from DC to 3 GHz, while the other can be used at frequencies as high as 6 GHz.

These data are subject to change without notice. Please contact your Avago Technologies Component salesperson for the latest revision of this application note.

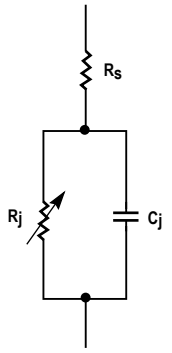


Figure 1. Linear model of a diode chip

Table 1.

	Element:	L_L	C_L	C_P	C_C	L_B
	Description:	Leadframe Inductance	Leadframe Capacitance	Package Capacitance	Coupling Capacitance	Bondwire Inductance
	Units:	nH	pF	pF	pF	nH
SOT-23/SOT-143	to 3 GHz	0.50	0	0.080	0.060	1.0
SOT-3x3	to 3 GHz	0.40	0	0.030	0.035	0.70
SOT-3x3	to 6 GHz	0.80	0.050	0.030	0.035	0.70

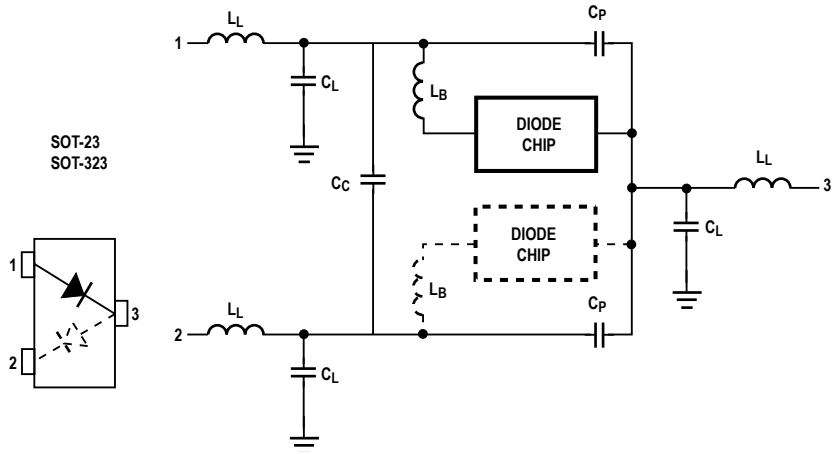


Figure 2. Model of the SOT-23 and SOT-323 packages

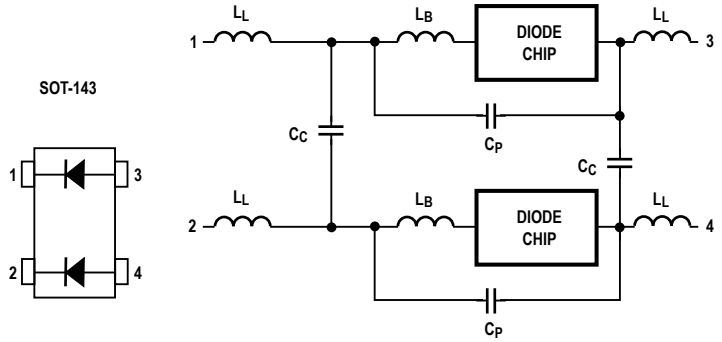


Figure 3. Model of the SOT-143 package

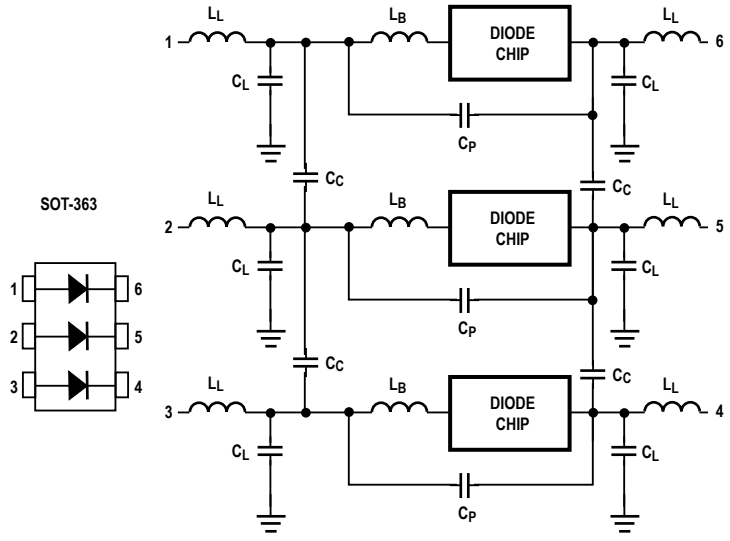


Figure 4. Model of the SOT-363 package

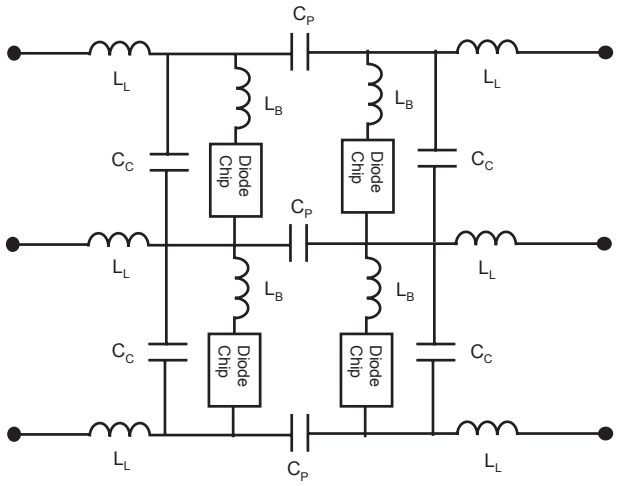


Figure 5. HSMS-28XP Package Model

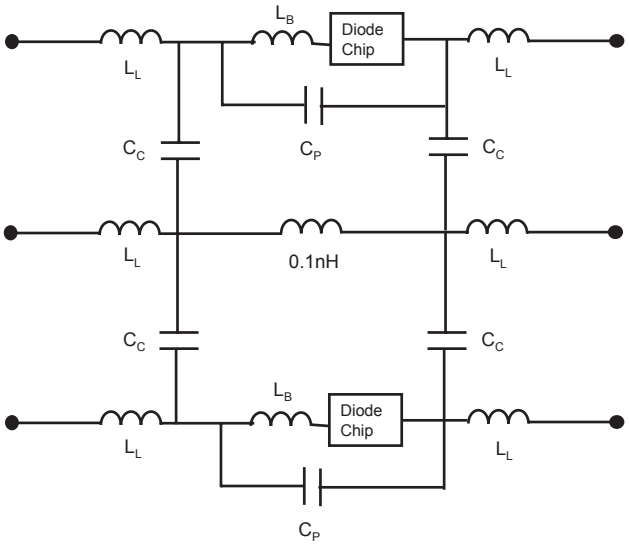


Figure 6. HSMS-28XK Package Model

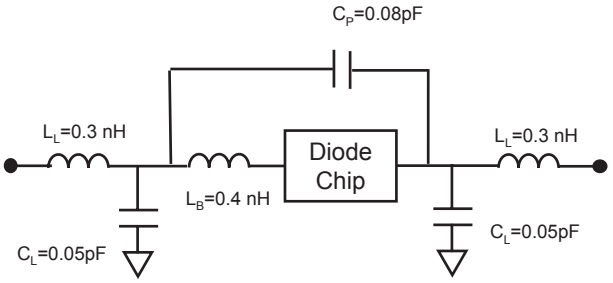


Figure 7. SOD-523 Package

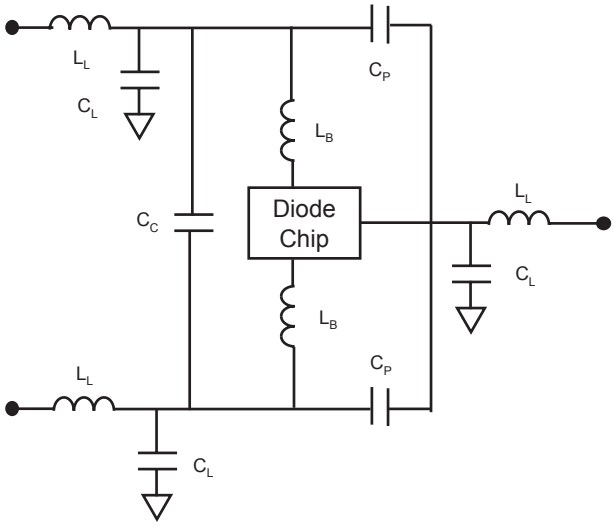


Figure 8. HSMX-48XB

For 1-mil gold wirebonds, inductance of the bond wire in nanohenries is roughly equal to its length in millimeters... 0.4mm of bond wire is equal to 0.4 nanoHenries of inductance, 1 mil of bond wire is equal to 25 pico-Henries of inductance, or 40 mils of bondwire is equal to one nanohenry.

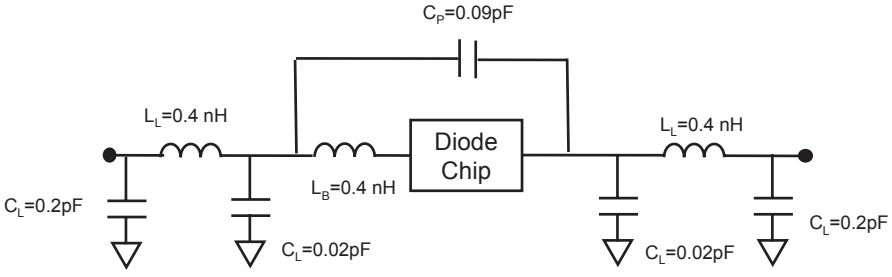


Figure 9. SOD-323 Package

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

AV02-0038EN - January 15, 2007

HPND- 4005
Beam Lead PIN Diode

Data Sheet

Description

The HPND-4005 planar beam lead PIN diode is constructed to offer exceptional lead strength while achieving excellent electrical performance at high frequencies. High beam strength offers users superior assembly yield, while extremely low capacitance allows high isolation to be realized.

Nitride passivation and polyimide coating provide reliable device protection.

Applications

The HPND-4005 beam lead PIN diode is designed for use in stripline or microstrip circuits. Applications include switching, attenuating, phase shifting, limiting, and modulating at microwave frequencies. The extremely low capacitance of the HPND-4005 makes it ideal for circuits requiring high isolation in a series diode configuration.

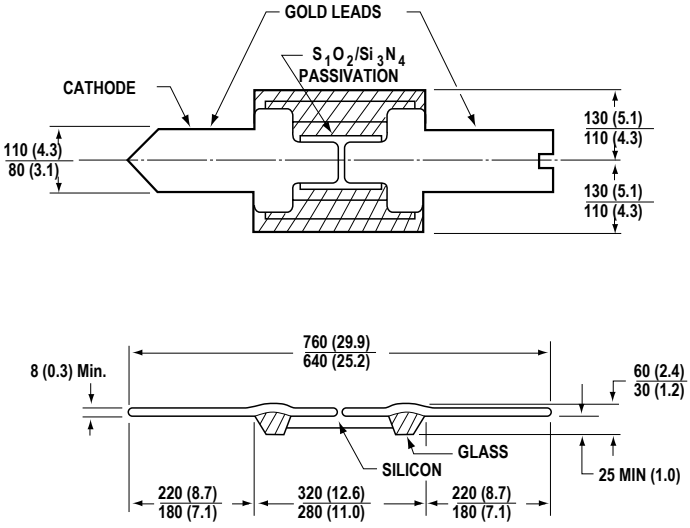
Maximum Ratings

Operating Temperature	-65°C to +175°C
Storage Temperature	-65°C to +200°C
Power Dissipation at TCASE = 25°C (Derate linearly to zero at 175°C.)	250 mW
Minimum Lead Strength	4 grams pull on either lead
Diode Mounting Temp	220°C for 10 sec. max.

Features

- High Breakdown Voltage: 120 V Typical
- Low Capacitance: 0.017 pF Typical
- Low Resistance: 4.7 Ω Typical
- Rugged Construction: 4 Grams Minimum Lead Pull
- Nitride Passivated

Outline 21



DIMENSIONS IN μm (1/1000 inch)

Electrical Specifications at $T_A = 25°C$

Part Number	Breakdown Voltage V_{BR} (V)		Series Resistance R_S (Ω)[2]		Capacitance C_T (pF)[1,2]		Forward Voltage V_F (V)	Reverse Current I_R (nA)	Minority Carrier Lifetime τ (ns)[2]	
HPND-	Min.	Typ.	Typ.	Max.	Typ.	Max.	Max.	Max.	Min.	Typ.
4005	100	120	4.7	6.5	0.017	0.02	1.0	100	50	100
Test Conditions	$I_R = 10\ \mu A$		$I_F = 20$ mA $I_F = 100$ MHz		$V_R = 10$ V f = 10 GHz		$I_F = 20$ mA	$V_R = 30$ V	$I_F = 10$ mA $I_R = 6$ mA	

Notes:

1. Total capacitance calculated from measured isolation value in a series configuration.
2. Test performed on packaged samples.

Typical Parameters

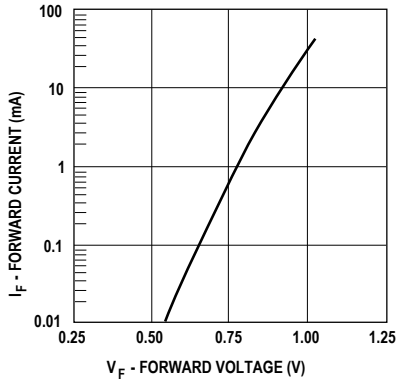


Figure 1. Typical Forward Conduction Characteristics.

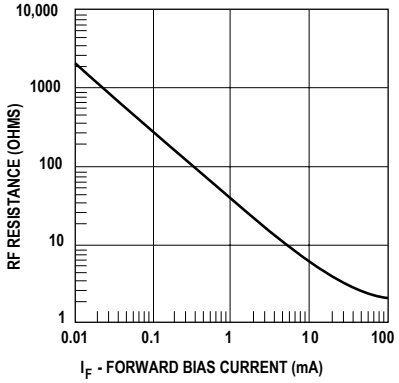


Figure 2. Typical RF Resistance vs. Forward Bias Current.

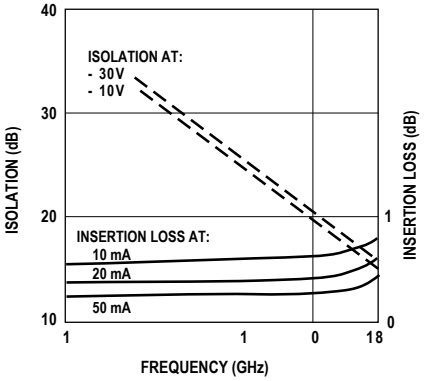


Figure 3. Typical Isolation and Insertion Loss in the Series Configuration (Z_O = 50 ½).

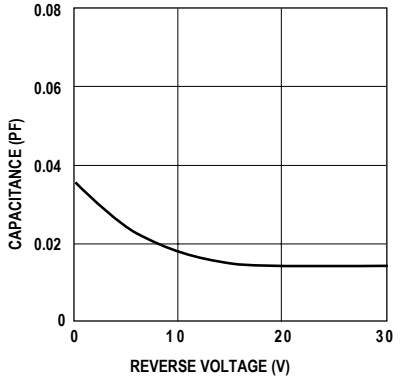


Figure 4. Typical Capacitance at 10 GHz vs. Reverse Bias.

Bonding and Handling Procedures for Beam Lead Diodes

1. Storage

Under normal circumstances, storage of beam lead diodes in Avago-supplied waffle/gel packs is sufficient. In particularly dusty or chemically hazardous environments, storage in an inert atmosphere desiccator is advised.

2. Handling

In order to avoid damage to beam lead devices, particular care must be exercised during inspection, testing, and assembly. Although the beam lead diode is designed to have exceptional lead strength, its small size and delicate nature requires that special handling techniques be observed so that the devices will not be mechanically or electrically damaged. A vacuum pickup is recommended for picking up beam lead devices, particularly larger ones, e.g., quads. Care must be exercised to assure that the vacuum opening of the needle is sufficiently small to avoid passage of the device through the opening. A #27 tip is recommended for picking up single beam lead devices. A 20X magnification is needed for precise positioning of the tip on the device. Where a vacuum pickup is not used, a sharpened wooden Q-tip dipped in isopropyl alcohol is very commonly used to handle beam lead devices.

3. Cleaning

For organic contamination use a warm rinse of trichloroethane, or its locally approved equivalent, followed by a cold rinse in acetone and methanol. Dry under infrared heat lamp for 5–10 minutes on clean filter paper. Freon degreaser, or its locally approved equivalent, may replace trichloroethane for light organic contamination.

- Ultrasonic cleaning is not recommended.
- Acid solvents should not be used.

4. Bonding

Thermocompression: See Application Note 979 "The Handling and Bonding of Beam Lead Devices Made Easy". This method is good for hard substrates only.

Wobble: This method picks up the device, places it on the substrate and forms a thermo-compression bond all in one operation. This is described in the latest version of MIL-STD-883, Method 2017, and is intended for hard substrates only.

Resistance Welding or Parallel-GAP Welding: To make

welding on soft substrates easier, a low pressure welding head is recommended. Suitable equipment is available from HUGHES, Industrial Products Division in Carlsbad, CA.

Epoxy: With solvent free, low resistivity epoxies (available from ABLESTIK and improvements in dispensing equipment, the quality of epoxy bonds is sufficient for many applications.

5. Lead Stress

In the process of bonding a beam lead diode, a certain amount of "bugging" occurs. The term **bugging** refers to the chip lifting away from the substrate during the bonding process due to the deformation of the beam by the bonding tool. This effect is beneficial as it provides stress relief for the diode during thermal cycling of the substrate. The coefficient of expansion of some substrate materials, specifically soft substrates, is such that some bugging is essential if the circuit is to be operated over wide temperature extremes.

Thick metal clad ground planes restrict the thermal expansion of the dielectric substrates in the X-Y axis. The expansion of the dielectric will then be mainly in the Z axis, which does not affect the beam lead device. An alternate solution to the problem of dielectric ground plane expansion is to heat the substrate to the maximum required operating temperature during the beam lead attachment. Thus, the substrate is at maximum expansion when the device is bonded. Subsequent cooling of the substrate will cause bugging, similar to bugging in thermocompression bonding or epoxy bonding. Other methods of bugging are preforming the leads during assembly or prestressing the substrate.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

AV01-0593EN - October 12, 2006

HSMP-381x, 481x

Surface Mount RF PIN

Low Distortion Attenuator Diodes

Data Sheet

Lead (Pb) Free
RoHS 6 fully
compliant

Description/Applications

The HSMP-381x series is specifically designed for low distortion attenuator applications. The HSMP-481x products feature ultra low parasitic inductance in the SOT-23 and SOT-323 packages. They are specifically designed for use at frequencies which are much higher than the upper limit for conventional diodes.

A SPICE model is not available for PIN diodes as SPICE does not provide for a key PIN diode characteristic, carrier lifetime.

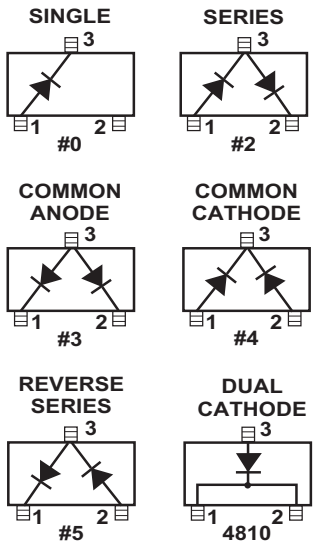
Features

- Diodes Optimized for:
  - Low Distortion Attenuating
  - Microwave Frequency Operation
- Surface Mount Packages
  - Single and Dual Versions
  - Tape and Reel Options Available
- Low Failure in Time (FIT) Rate[1]
- Lead free

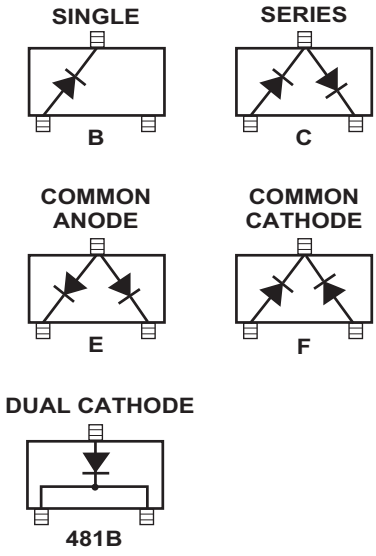
Note:

1. For more information see the Surface Mount PIN Reliability Data Sheet.

Package Lead Code Identification, SOT-23 (Top View)



Package Lead Code Identification, SOT-323 (Top View)



Absolute Maximum Ratings[1] $T_C = +25°C$

Symbol	Parameter	Unit	SOT-23	SOT-323
I_f	Forward Current (1 µs Pulse)	Amp	1	1
P_{IV}	Peak Inverse Voltage	V	Same as V_{BR}	Same as V_{BR}
T_j	Junction Temperature	°C	150	150
T_{stg}	Storage Temperature	°C	-65 to 150	-65 to 150
θ_{jc}	Thermal Resistance [2]	°C/W	500	150

Notes:
1. Operation in excess of any one of these conditions may result in permanent damage to the device.
2. $T_C = +25°C$, where T_C is defined to be the temperature at the package pins where contact is made to the circuit board.

Electrical Specifications $T_C = +25°C$ (Each Diode)

Conventional Diodes

Part Number HSMP-	Package Marking Code	Lead Code	Configuration	Minimum Breakdown Voltage V_{BR} (V)	Maximum Total Capacitance C_T (pF)	Minimum Resistance at $I_F = 0.01mA$, RH (Ω)	Maximum Resistance at $I_F = 20mA$, R_L (Ω)	Maximum Resistance at $I_F = 100mA$, RT (Ω)	Resistance at $I_F = 1mA$, R_M (Ω)
3810	E0	0	Single	100	0.35	1500	10	3.0	48 to 70
3812	E2	2	Series						
3813	E3	3	Common Anode						
3814	E4	4	Common Cathode						
3815	E5	5	Reverse Series						
381B	E0	B	Single						
381C	E2	C	Series						
381E	E3	E	Common Anode						
381F	E4	F	Common Cathode						
Test Conditions				$V_R = V_{BR}$ Measure $I_R \leq 10uA$	$V_R = 50V$ f = 1MHz	$I_F = 0.01mA$ f = 100MHz	$I_F = 20mA$ f = 100MHz	$I_F = 100mA$ f = 100MHz	$I_F = 1mA$ f = 100MHz

High Frequency (Low Inductance, 500 MHz – 3 GHz) PIN Diodes

Part Number HSMP-	Package Marking Code	Lead Code	Configuration	Minimum Breakdown Voltage V_{BR} (V)	Maximum Series Resistance R_S (Ω)	Series Resistance $I_F = 1mA$, R_M (Ω)	Typical Total Capacitance C_T (pF)	Maximum Total Capacitance C_T (pF)	Typical Total Inductance L_T (nH)
4810	EB	B	Dual Cathode	100	3	48 - 70	0.35	0.4	1
481B	EB	B	Dual Cathode						
Test Conditions				$V_R = V_{BR}$ Measure $I_R \leq 10\mu A$	$I_F = 100mA$ f = 100MHz	$I_F = 1mA$ f = 100MHz	$V_R = 50V$ f = 1MHz	$V_R = 50V$ f = 1MHz	f = 500MHz - 3GHz

Typical Parameters at $T_C = 25°C$

Part Number	Series Resistance	Carrier Lifetime	Reverse Recovery Time	Total Capacitance
HSMP-	R_S (Ω)	τ (ns)	T_{rr} (ns)	C_T (pF)
381x	53	1500	300	0.27 @ 50 V
Test Conditions	I_F = 1 mA f = 100 MHz	I_F = 50 mA I_R = 250 mA	V_R = 10 V I_F = 20 mA 90% Recovery	f = 1 MHz

Typical Parameters at $T_C = 25°C$ (unless otherwise noted), Single Diode

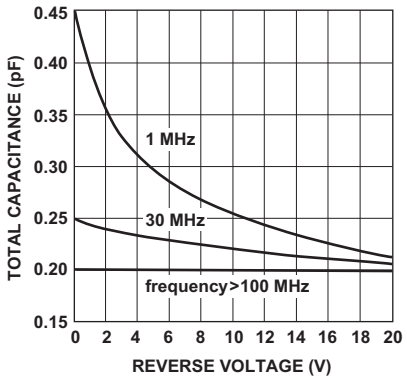


Figure 1. RF Capacitance vs. Reverse Bias.

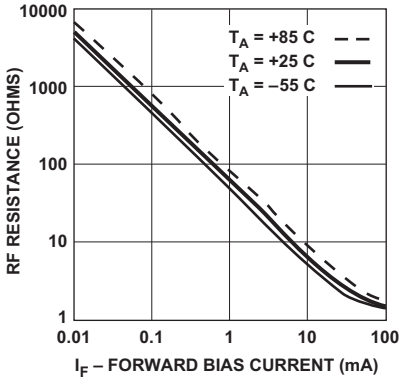


Figure 2. RF Resistance vs. Forward Bias Current, f = 100MHz

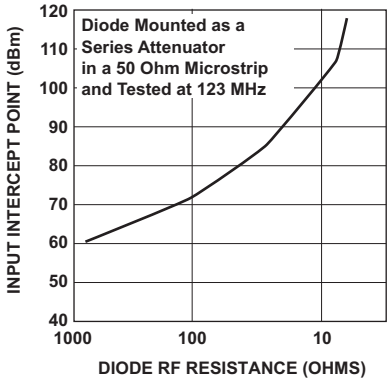


Figure 3. 2nd Harmonic Input Intercept Point vs. Diode RF Resistance.

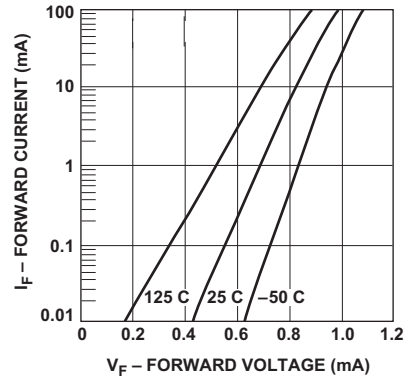


Figure 4. Forward Current vs. Forward Voltage.

Typical Applications for Multiple Diode Products

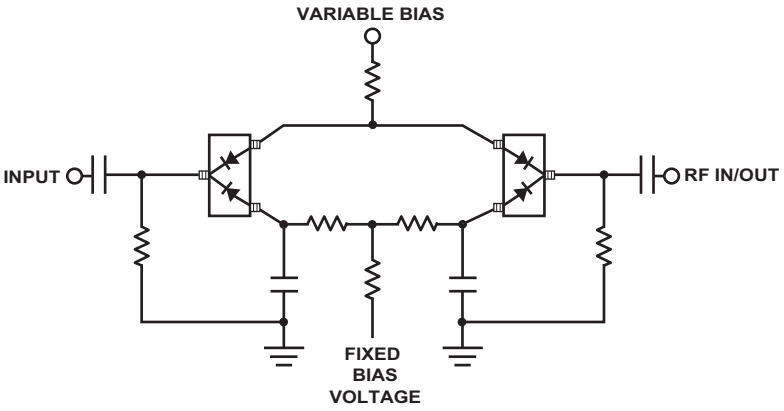


Figure 5. Four Diode π Attenuator. See Application Note 1048 for Details.

Notes:
3. Typical values were derived using limited samples during initial product characterization and may not be representative of the overall distribution.

Typical Applications for HSMP-481x Low Inductance Series

Microstrip Series Connection for HSMP-481x Series

In order to take full advantage of the low inductance of the HSMP-481x series when using them in series applications, both lead 1 and lead 2 should be connected together, as shown in Figure 7.

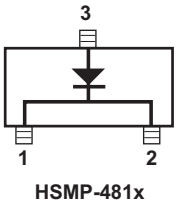


Figure 6. Internal Connections.

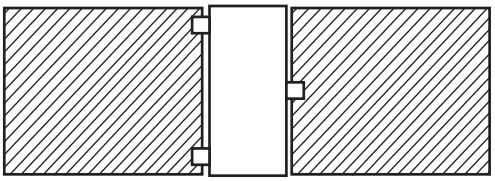


Figure 7. Circuit Layout.

Microstrip Shunt Connections for HSMP-481x Series

In Figure 8, the center conductor of the microstrip line is interrupted and leads 1 and 2 of the HSMP-481x series diode are placed across the resulting gap. This forces the 1.5 nH lead inductance of leads 1 and 2 to appear as part of a low pass filter, reducing the shunt parasitic inductance and increasing the maximum available attenuation. The 0.3 nHof shunt inductance external to the diode is created by the via holes, and is a good estimate for 0.032" thick material.

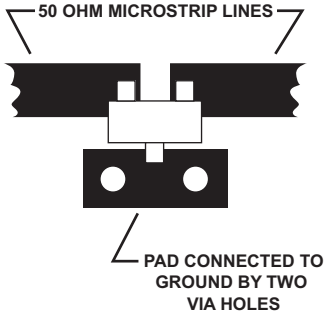


Figure 8. Circuit Layout.

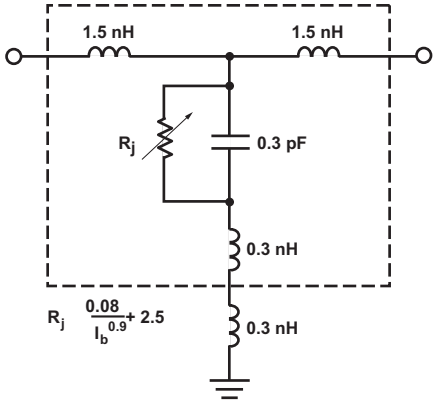


Figure 9. Equivalent Circuit.

Typical Applications for HSMP-481x Low Inductance Series (continued)

Co-Planar Waveguide Shunt Connection for HSMP-481x Series

Co-Planar waveguide, with ground on the top side of the printed circuit board, is shown in Figure 10. Since it eliminates the need for via holes to ground, it offers lower shunt parasitic inductance and higher maximum attenuation when compared to microstrip circuit.

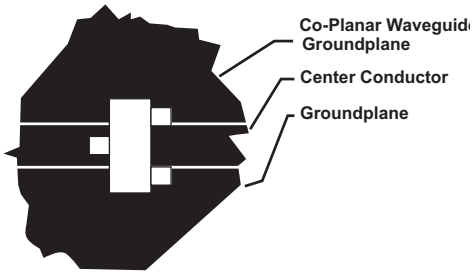


Figure 10. Circuit Layout.

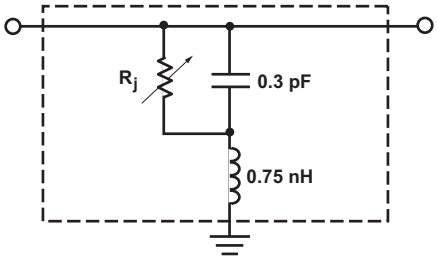
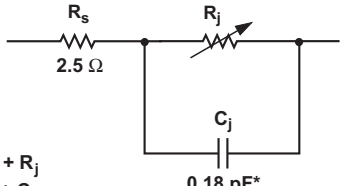


Figure 11. Equivalent Circuit.

Equivalent Circuit Model HSMP-381x Chip*



$R_T = 2.5 + R_j$

$C_T = C_P + C_j$

$R_j = \frac{80}{I^{0.9}}\ \Omega$

* Measured at -20 V

I = Forward Bias Current in mA

*See AN1124 for package models.

Assembly Information

SOT-323 PCB Footprint

A recommended PCB pad layout for the miniature SOT-323 (SC-70) package is shown in Figure 12 (dimensions are in inches). This layout provides ample allowance for package placement by automated assembly equipment without adding parasitics that could impair the performance.

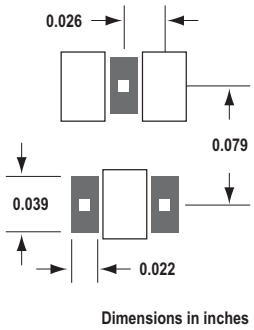


Figure 12. Recommended PCB Pad Layout for Avago's SC70 3L/SOT-323 Products.

SOT-23 PCB Footprint

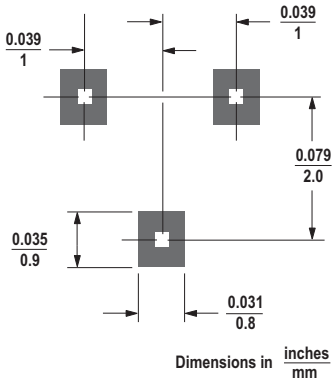


Figure 13. Recommended PCB Pad Layout for Avago's SOT-23 Products.

SMT Assembly

Reliable assembly of surface mount components is a complex process that involves many material, process, and equipment factors, including: method of heating (e.g., IR or vapor phase reflow, wave soldering, etc.) circuit board material, conductor thickness and pattern, type of solder alloy, and the thermal conductivity and thermal mass of components. Components with a low mass, such as the SOT-323/-23 package, will reach solder reflow temperatures faster than those with a greater mass.

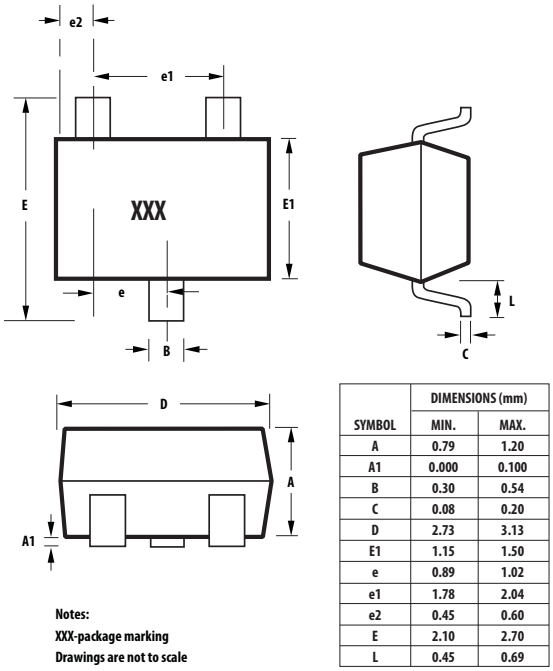
After ramping up from room temperature, the circuit board with components attached to it (held in place with solder paste) passes through one or more preheat zones. The preheat zones increase the temperature of the board and components to prevent thermal shock and begin evaporating solvents from the solder paste. The reflow zone briefly elevates the temperature sufficiently to produce a reflow of the solder.

The rates of change of temperature for the ramp-up and cool-down zones are chosen to be low enough to not cause deformation of the board or damage to components due to thermal shock. The maximum temperature in the reflow zone (T_{MAX}) should not exceed 260°C.

These parameters are typical for a surface mount assembly process for Avago diodes. As a general guideline, the circuit board and components should be exposed only to the minimum temperatures and times necessary to achieve a uniform reflow of solder.

Package Dimensions

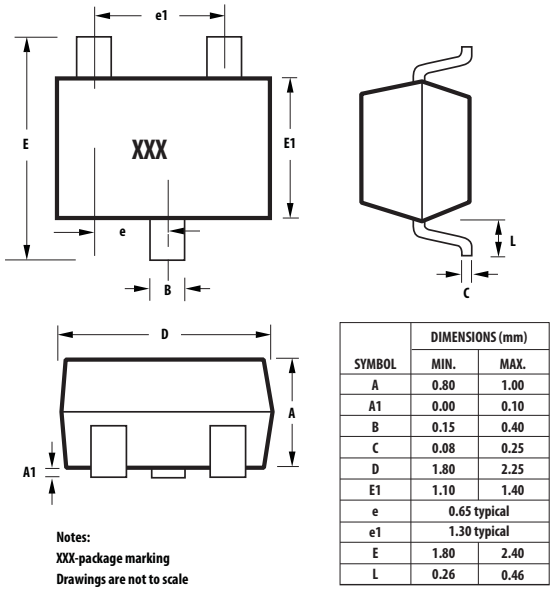
Outline 23 (SOT-23)



Notes:
XXX-package marking
Drawings are not to scale

SYMBOL	DIMENSIONS (mm)	
	MIN.	MAX.
A	0.79	1.20
A1	0.000	0.100
B	0.30	0.54
C	0.08	0.20
D	2.73	3.13
E1	1.15	1.50
e	0.89	1.02
e1	1.78	2.04
e2	0.45	0.60
E	2.10	2.70
L	0.45	0.69

Outline SOT-323 (SC-70)



Notes:
XXX-package marking
Drawings are not to scale

SYMBOL	DIMENSIONS (mm)	
	MIN.	MAX.
A	0.80	1.00
A1	0.00	0.10
B	0.15	0.40
C	0.08	0.25
D	1.80	2.25
E1	1.10	1.40
e	0.65 typical	
e1	1.30 typical	
E	1.80	2.40
L	0.26	0.46

Package Characteristics

Lead Material ..... Copper (SOT-323); Alloy 42 (SOT-23)
Lead Finish ..... Tin 100% (Lead-free option)
Maximum Soldering Temperature ..... 260°C for 5 seconds
Minimum Lead Strength ..... 2 pounds pull
Typical Package Inductance ..... 2 nH
Typical Package Capacitance ..... 0.08 pF (opposite leads)

Ordering Information

Specify part number followed by option. For example:

HSMP - 381x - XXX

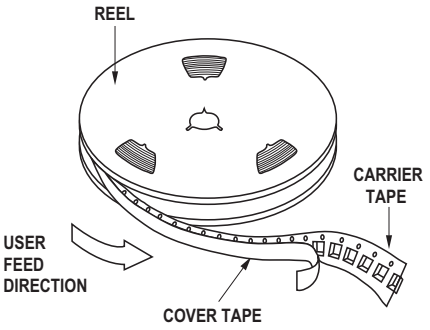
- XXX — Bulk or Tape and Reel Option
- 381x — Part Number; x = Lead Code
- HSMP — Surface Mount PIN

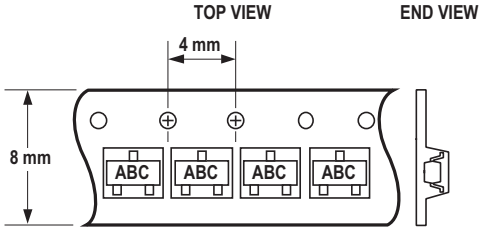
Option Descriptions

-BLKG = Bulk, 100 pcs. per antistatic bag
-TR1G = Tape and Reel, 3000 devices per 7" reel
-TR2G = Tape and Reel, 10,000 devices per 13" reel

Tape and Reeling conforms to Electronic Industries RS-481, "Taping of Surface Mounted Components for Automated Placement."

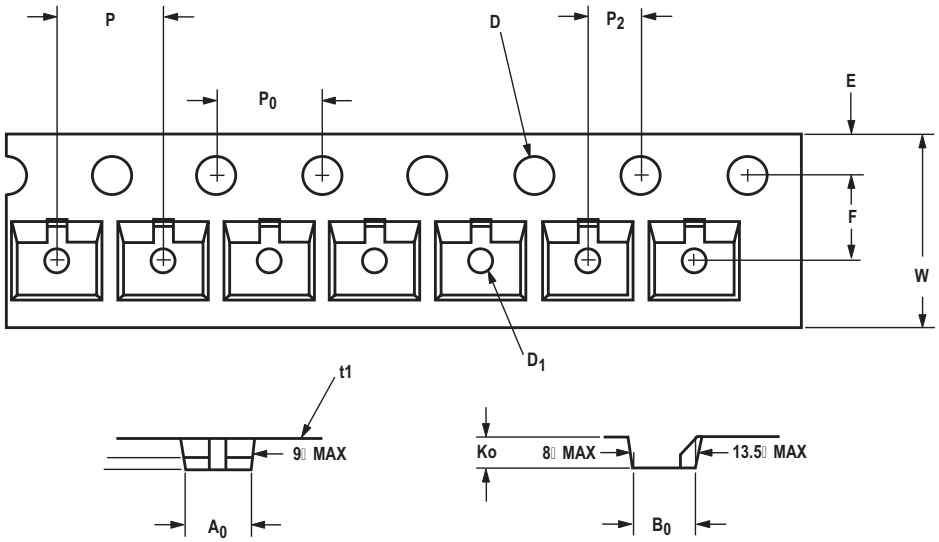
Device Orientation
For Outlines SOT-23/323





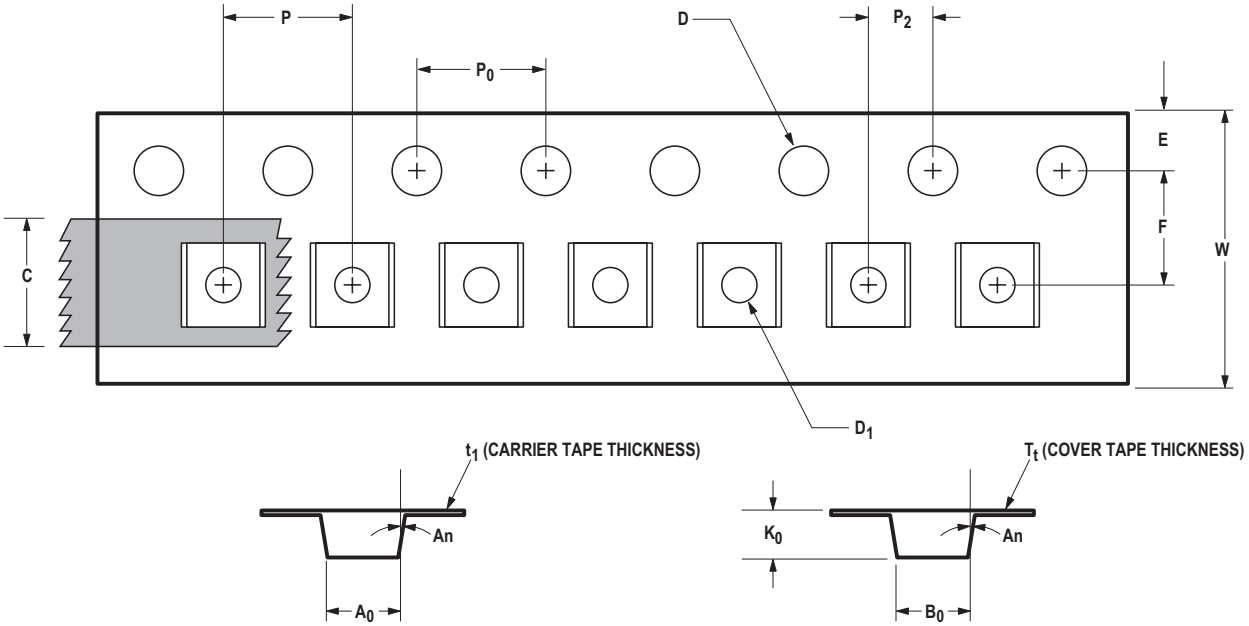
Note: "AB" represents package marking code.
"C" represents date code.

Tape Dimensions and Product Orientation
For Outline SOT-23



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	3.15 ± 0.10	0.124 ± 0.004
	WIDTH	B_0	2.77 ± 0.10	0.109 ± 0.004
	DEPTH	K_0	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.05	0.039 ± 0.002
PERFORATION	DIAMETER	D	1.50 + 0.10	0.059 + 0.004
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 + 0.30 - 0.10	0.315 + 0.012 - 0.004
	THICKNESS	t1	0.229 ± 0.013	0.009 ± 0.0005
DISTANCE BETWEEN CENTERLINE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002

Tape Dimensions and Product Orientation
For Outline SOT-323



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A_0	2.40 ± 0.10	0.094 ± 0.004
	WIDTH	B_0	2.40 ± 0.10	0.094 ± 0.004
	DEPTH	K_0	1.20 ± 0.10	0.047 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D_1	1.00 + 0.25	0.039 + 0.010
PERFORATION	DIAMETER	D	1.55 ± 0.05	0.061 ± 0.002
	PITCH	P_0	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 ± 0.30	0.315 ± 0.012
	THICKNESS	t_1	0.254 ± 0.02	0.0100 ± 0.0008
COVER TAPE	WIDTH	C	5.4 ± 0.10	0.205 ± 0.004
	TAPE THICKNESS	T_t	0.062 ± 0.001	0.0025 ± 0.00004
DISTANCE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P_2	2.00 ± 0.05	0.079 ± 0.002
ANGLE	FOR SOT-323 (SC70-3 LEAD)	An	8° C MAX	
	FOR SOT-363 (SC70-6 LEAD)		10° C MAX	

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

AV02-0402EN - December 22, 2009

ROGERS CORPORATION

Advanced Circuit Materials

Advanced Circuit Materials Division
100 S. Roosevelt Avenue
Chandler, AZ 85226
Tel: 480-961-1382, Fax: 480-961-4533
www.rogerscorporation.com

Data Sheet
1.3000

RO3000® Series High Frequency Circuit Materials

Features and Benefits:

- Low dielectric loss for high frequency performance (RO3003). Laminate can be used in applications up to 30-40 GHz.
- Excellent mechanical properties versus temperature for reliable stripline and multilayer board constructions.
- Uniform mechanical properties for a range of dielectric constants. Ideal for multilayer board designs with a range of dielectric constants. Suitable for use with epoxy glass multilayer board hybrid designs.
- Stable dielectric constant versus temperature and frequency for RO3003. Ideal for band pass filters, microstrip patch antennas, and voltage controlled oscillators.
- Low in-plane expansion coefficient (matched to copper). Allows for more reliable surface mounted assemblies. Ideal for applications sensitive to temperature change and excellent dimensional stability.
- Volume manufacturing process for economical laminate pricing.

Typical Applications:

- Automotive Collision Avoidance Systems
- Automotive Global Positioning Satellite Antennas
- Cellular and Pager Telecommunications Systems
- Patch Antennas for Wireless Communications
- Direct Broadcast Satellites
- Datalink on Cable Systems
- Remote Meter Readers
- Power Backplanes

RO3000® High Frequency Circuit Materials are ceramic- filled PTFE composites intended for use in commercial microwave and RF applications. This family of products was designed to offer exceptional electrical and mechanical stability at competitive prices.

RO3000® series laminates are PTFE-based circuit materials with mechanical properties that are consistant regardless of the dielectric constant selected. This allows the designer to develop multilayer board designs that use different dielectric constant materials for individual layers, without encountering warpage or reliability problems.

The dielectric constant versus temperature of RO3000 series materials is very stable (Charts 1 and 2). These materials exhibit a coefficient of thermal expansion (CTE) in the X and Y axis of 17 ppm/°C. This expansion coefficient is matched to that of copper, which allows the material to exhibit excellent dimensional stability, with typical etch shrinkage (after etch and bake) of less than 0.5 mils per inch. The Z-axis CTE is 24 ppm/ C, which provides exceptional plated through-hole reliability, even in severe thermal environments.

RO3000® series laminates can be fabricated into printed circuit boards using standard PTFE circuit board processing techniques, with minor modifications as described in the application note "Fabrication Guidelines for RO3000® Series High Frequency Circuit Materials."

Available claddings are ½ , 1 or 2 oz./ft^2 (17, 35, 70 µm thick) electrodeposited copper foil.

RO3000® laminates are manufactured under an ISO 9002 certified system.

Chart 1: RO3003™ Laminate Dielectric Constant vs. Temperature

The data in Chart 1 demonstrates the excellent stability of dielectric constant over temperature for RO3003™ laminates, including the elimination of the step change in dielectric constant, which occurs near room temperature with PTFE glass materials.

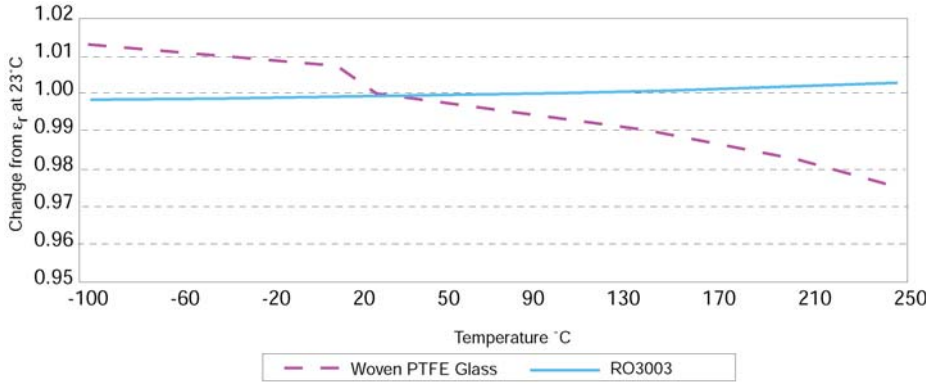


Chart 2: RO3006™ and RO3010™ Laminate Dielectric Constant vs. Temperature

The data in Chart 2 shows the change in dielectric constant vs. temperature for RO3006™ and RO3010™ laminates. These materials exhibit significant improvement in temperature stability of dielectric constant when compared to other high dielectric constant PTFE laminates.

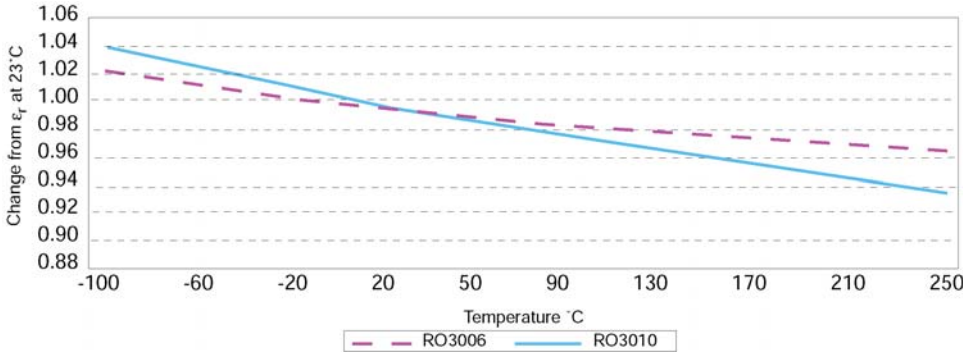
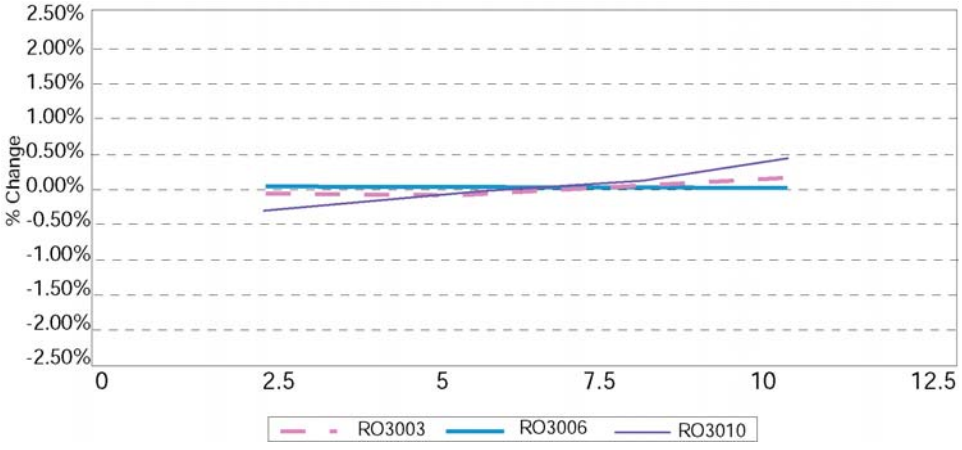


Chart 3: Dielectric Constant vs. Frequency for RO3000® Series Laminate

Chart 3 demonstrates the stability of dielectric constant for RO3000® series products over frequency. This stability simplifies the design of broad- band components as well as allowing the materials to be used in a wide range of applications over a very broad range of frequencies.



The data in Charts 1, 2 and 3 was produced using a modified IPC-TM-650, 2.5.5.5 method. For additional information request Rogers T.R. 5156 and T.M. 4924.

Typical Values **RO3000 Series High Frequency Laminates**

PROPERTY	TYPICAL VALUE (1)			DIRECTION	UNIT	CONDITION	TEST METHOD
	RO3003	RO3006	RO3010				
Dielectric Constant ε_r	3.00±0.04(2)	6.15±0.15	10.2±0.30	Z	-	10GHz 23°C	IPC-TM-650 2.5.5.5
Dissipation Factor	0.0013	0.0020	0.0023	Z	-	10GHz 23°C	IPC-TM-650 2.5.5.5
Thermal Coefficient of ε_r	13	-160	-280	Z	ppm/°C	10GHz 0-100°C	IPC-TM-650 2.5.5.5
Dimensional Stability	0.5	0.5	0.5	X,Y	mm/m	COND A	ASTM D257
Volume Resistivity	10^7	10^3	10^3		MΩ•cm	COND A	IPC 2.5.17.1
Surface Resistivity	10^7	10^3	10^3		MΩ	COND A	IPC 2.5.17.1
Tensile Modulus	2068 (300)	2068 (300)	2068 (300)	X,Y	MPa (kpsi)	23°C	ASTM D638
Water Absorption	<0.1	<0.1	<0.1	-	%	D24/23	IPC-TM-650 2.6.2.1
Specific Heat	0.93 (0.22)	0.93 (0.22)	0.93 (0.22)		J/g/K (BTU/lb/°F)		Calculated
Thermal Conductivity	0.50	0.61	0.66	-	W/m/K	100°C	ASTM C518
Coefficient of Thermal Expansion	17 24	17 24	17 24	X,Y Z	ppm/°C	-55 to 288°C	ASTM D3386-94
Td	500	500	500		°C TGA		ASTM D 3850
Color	Tan	Tan	Off White				
Density	2.1	2.6	3.0		gm/cm^3		
Copper Peel Strength	3.1 (17.6)	2.1 (12.2)	2.4 (13.4)		N/mm (lb/in)	After solder float	IPC-TM-2.4.8
Flammability	94V-0	94V-0	94V-0				UL
Lead Free Process Capatible	Yes	Yes	Yes				

(1) References: Internal T.R.'s 1430, 2224, 2854. Tests at 23°C unless otherwise noted. Typical values should not be used for specification limits.

(2) The nominal dielectric constant of an 0.060" thick RO3003® laminate as measured by the IPC-TM-650, 2.5.5.5 will be 3.02, due to the elimination of biasing caused by air gaps in the test fixture. For further information refer to Rogers T.R. 5242.

STANDARD THICKNESS:

RO3003:
0.005" (0.13 mm)
0.010" (0.25 mm)
0.020" (0.50 mm)
0.030" (0.75 mm)
0.060" (1.52 mm)

RO3006/3010:
0.005"(0.13 mm)
0.010"(0.25 mm)
0.025"(0.64 mm)
0.050"(1.28 mm)

STANDARD PANEL SIZE:

RO3003:
12" X 18" (305 X 457mm)
24" X 18" (610 X 457mm)
24" X 36" (610 X 915mm)

RO3006/3010:
18" X 12" (457 X 305mm)
18" X 24" (457 X 610mm)
18" X 36" (457 X 915mm)
18" X 48" (457 X 1.224m)

STANDARD COPPER CLADDING:

½ oz. (17μm), 1 oz. (35μm),
2 oz. (70μm) electrodeposited copper foil.

CONTACT INFORMATION:

USA:	Rogers Advanced Circuit Materials - ISO 9000:2000 certified	Tel: 480-961-1382	Fax: 480-961-4533
Belgium:	Rogers NV - Gent - ISO 9000:2000 certified	Tel: +32-9-2353611	Fax: +32-9-2353658
Japan:	Rogers Japan Inc.	Tel: 81-3-5200-2700	Fax: 81-3-5200-0571
Taiwan:	Rogers Taiwan Inc.	Tel: 886-2-86609056	Fax: 886-2-86609057
Korea:	Rogers Korea Inc.	Tel: 82-31-716-6112	Fax: 82-31-716-6208
Singapore:	Rogers Technologies Singapore Inc.	Tel: 65-747-3521	Fax: 65-747-7425
China:	Rogers (Shanghai) International Trading Co., Ltd	Tel: 86-21-63916088	Fax: 86-21-63915060

Revised 03/05, 0694-0305-.5 CC **Publication** #92-130