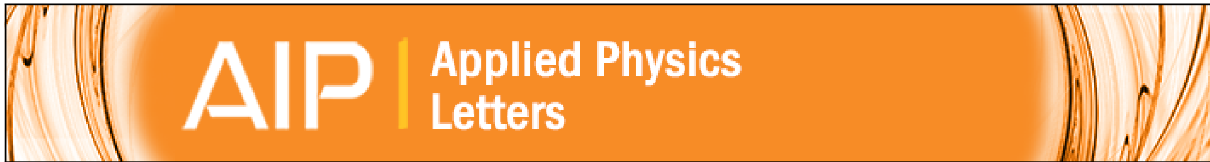

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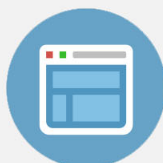

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HTML ABSTRACT + LINKS

Temperature-dependent transition to progressive breakdown in thin silicon dioxide based gate dielectrics

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The transition between well-defined soft and hard breakdown modes to progressive breakdown in ultrathin silicon dioxide based dielectrics is studied by means of the statistics of residual time (the time from first breakdown to device failure). By stressing metal-oxide-semiconductor test capacitors with an oxide thickness of 2.2 nm under different gate bias and temperatures, it is demonstrated that low voltages and temperatures favor stable hard and soft breakdown modes, while high temperatures and voltages lead to a progressive breakdown controlled regime. Our results support the idea that no significant change of the involved physics occurs in the transition from one breakdown regime to the other. The continuous transition from one regime to the other permits one to clearly identify progressive breakdown as hard breakdown, which always requires a certain time to reach the device failure conditions. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1925316]

Gate oxide breakdown (BD) has been a reliability concern for many generations of metal-oxide-semiconductor technology. The issue is more serious than ever for the ultrathin oxides of present interest because the time to the first BD diminishes by many orders of magnitude (at constant gate voltage) when scaling the oxide thickness (T_{OX}) from 3 to 1 nm.[1] However, the BD does not always cause device failure, and this relaxes the reliability constraints.[2] Dealing with the post-BD reliability is nevertheless difficult because the device failure criterion is application dependent and because the BD phenomenology apparently changes with T_{OX}. In the 3 to 5 nm T_{OX} range, two apparently stable BD modes have been identified as soft BD (SBD) and hard BD (HBD),[3] and a reliability model based on the HBD prevalence ratio (α_{HBD}) has been proposed.[4] On the other hand, it has been claimed that a distinction between HBD and SBD is meaningless in oxides thinner than ~2 nm because the BD current always increases continuously under stress until it is large enough to cause device failure.[5–7] The term "progressive breakdown" (PBD) has been coined to describe this type of BD,[6] and a related reliability methodology has been suggested.[5] Other reliability models based on the failure by superposition of multiple successive BD events have also been proposed. These models also rely on the assumption of the existence of a stable SBD mode that does not cause the device failure.[8,9]

In this letter, we report the transition from the HBD/SBD regime to the PBD regime as a function of the stress conditions. We have stressed poly-Si/SiO_2/Si(n) capacitors with T_{OX}=2.2 nm and oxide area of 10^{-4} cm^2 at different gate voltages (V_G) and temperatures (T). The samples are stressed in accumulation under constant voltage conditions and the evolution of the current is monitored. The stress is periodically stopped to measure the stress-induced leakage current (SILC) at a lower voltage (V_G=1.5 V) close to the operation conditions of these devices in digital circuits. The measure of the time to the first BD (t_{BD}) of each sample is based on the detection of a current step in the SILC. However, the stress experiment is not stopped at the first BD and it continues until the failure of the device. Based on recent results about the impact of BD on the performance of basic circuits,[10,11] devices are considered to fail when the gate leakage reaches a threshold of 10 μA at V_{SILC}. The residual time (t_{RES}) is defined as the interval elapsed between first BD and device failure (t_{FAIL}), that is, $t_{RES} \equiv t_{FAIL} - t_{BD}$. The residual time statistics and the comparison of the first BD and device failure distributions are the main tools used in this letter to investigate oxide BD.

The cumulative distributions of residual time $F_{RES}(t_{RES})$ measured at −30 °C are shown in Fig. 1 in the Weibull plot. First of all, we notice that F_{RES} (except for the case of V_G =4.5 V) is bimodal, that is, a short-T_{RES} mode and a long-T_{RES} mode separated by an intermediate plateau are clearly distinguished. It can be checked that the former corresponds to those devices that show HBD at the first BD and the latter

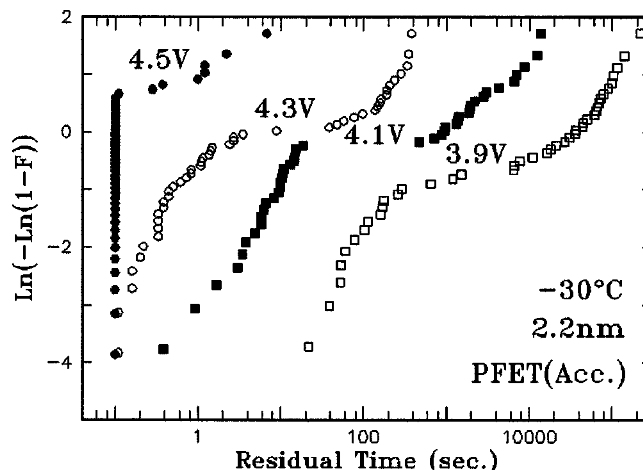

FIG. 1. Cumulative probability distribution of the residual time (F_{RES}) measured in poly-Si(n^+)/SiO_2/Si(n) capacitors with oxide thickness of 2.2 nm stressed in accumulation at −30 °C and at four different stress voltages.

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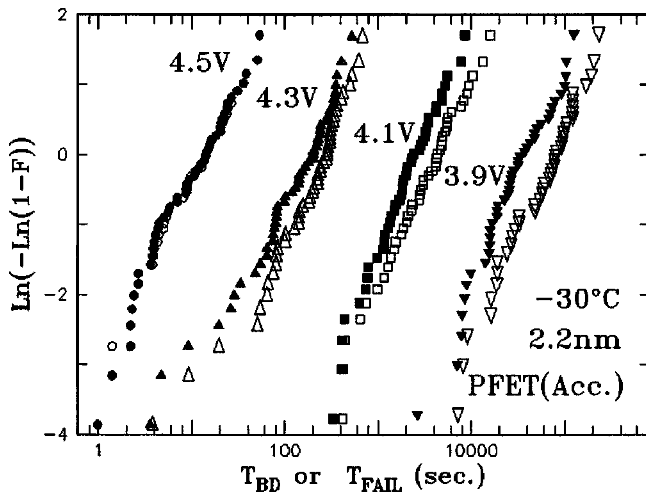

FIG. 2. Cumulative distributions of first breakdown (solid symbols) and device failure (open symbols) corresponding to the stress experiments defined in the caption of Fig. 1.

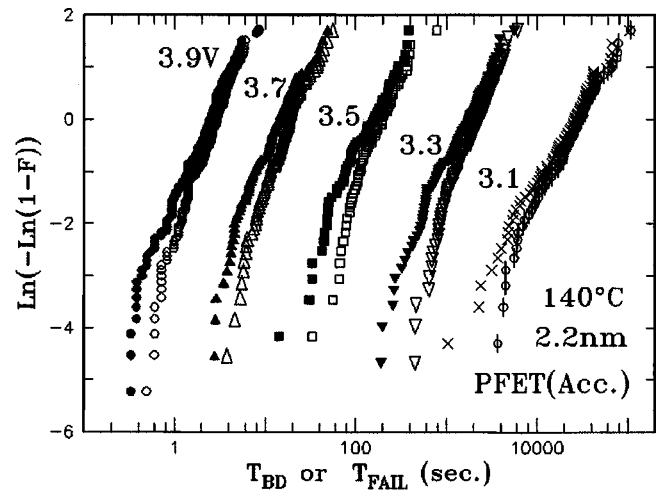

FIG. 4. Cumulative distributions of first breakdown (solid symbols) and final device failure (open symbols) measured in stress experiments performed at 140 °C and three different stress voltages (same as in Fig. 3).

to those that suffer one or more SBD events prior to HBD. The intermediate plateau corresponds to $F_{RES}=\alpha_{HBD}$. Although the residual time associated to HBD is short, it is nonzero and it increases as V_G is reduced. In other words, HBD is not instantaneous but progressive. This is consistent with the claim of Linder *et al.*, who identified PBD with the HBD mode.[5] In Fig. 2, the cumulative distribution of first BD (F_{BD}) and that of device failure (F_{FAIL}) are shown in the Weibull plot. It has been checked that all the devices fail due to the occurrence of a HBD event. The distributions F_{BD} and F_{FAIL} are roughly parallel in the Weibull plot, the vertical shift between them being $\ln(\alpha_{HBD})$, as predicted by the HBD prevalence ratio model,[4] The values of α_{HBD} measured from the Weibull plot shift are perfectly consistent with those required to fit the residual time distributions of Fig. 1. In agreement with previous results,[4] increasing V_G has the effect of increasing α_{HBD}, and this is why at V_G=4.5 V, almost all the devices show only HBD. In summary, the results obtained in 2.2 nm oxides stressed at T=−30 °C are perfectly compatible with the HBD prevalence ratio picture, which is based on the existence of two stable BD modes, SBD and HBD, as found in thicker oxides.[4] Examination of the post-BD current-voltage $I(V)$ characteristics (not shown here) also supports this claim. It is also true, however, that at high voltages only HBD is measured and, since HBD is found to be progressive (a nonzero residual time is needed to reach the device failure condition), one can say that PBD is the dominant mode at high stress voltages.

The results obtained when samples are stressed at T =140 °C are, however, qualitatively different. The range of V_G has been changed to keep T_{BD} and T_{FAIL} within a reasonable test window because T accelerates the BD. The measured F_{RES} is not bimodal in the considered V_G range (see Fig. 3), and F_{BD} and F_{FAIL} are not parallel in the Weibull plot (Fig. 4), but tend to diverge at low percentiles. These observations are compatible with F_{FAIL} being dominated by the PBD mode. Our preliminary interpretation of these results is that temperature favors HBD events and, even if V_G is reduced, no SBD events are observed at 140 °C. Hence, only PBD (i.e., progressive HBD) is the dominant mode under these stress conditions. However, to confirm this interpretation, we have stressed the devices at intermediate temperatures between −30 °C and 140 °C. Figure 5 shows the continuous transition from a bimodal residual time distribution at low temperatures to a single-mode distribution at higher

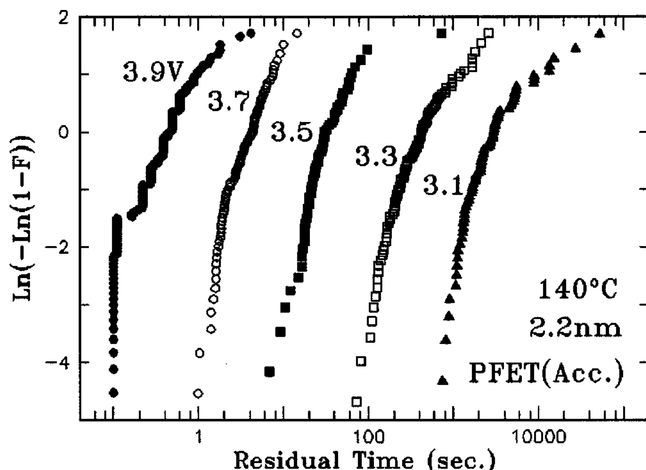

FIG. 3. Distribution of residual time obtained by stressing the simples at 140 °C and three stress voltages.

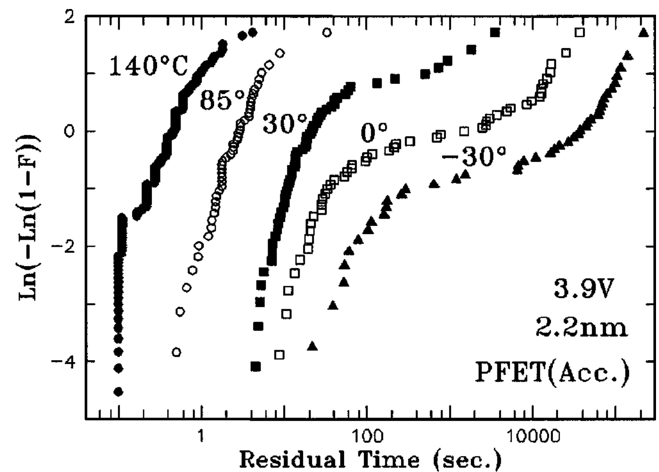

FIG. 5. Cumulative distributions of residual time obtained by stressing the devices under 3.9 V constant voltage conditions at different temperatures in the −30 to 140 °C range.

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values of T. While at low T, both progressive HBD and SBD coexist in the measurement window, SBD almost disappears at high T. In other words, α_{HBD} increases with T and the plateau of the bimodal F_{RES} moves up in the Weibull plot. Temperature has also the effect of reducing the time required for HBD to reach the device failure condition.

In this letter, we have shown a continuous transition from HBD/SBD modes to the PBD mode (which is actually HBD) as a function of T (Fig. 5) and V_G (Fig. 1). Our results suggest that the observation of PBD mode in ultrathin oxides is not related to an essential change in the physics of the BD, but rather to the fact that SBD tends to disappear at the stress conditions required to keep T_{BD} within reasonable limits. T_{OX} certainly plays a relevant role because α_{HBD} changes from 1 to nearly 0 quite abruptly as a function of voltage, and this change takes place at a value of V_G that depends on T_{OX}.[12] The thinner the oxide, the lower V_G at which this transition occurs.[12] Thus, for the same stress conditions, thinner oxides will appear as dominated by PBD, while the HBD/SBD picture seems adequate for thicker oxides. However, this does not mean that what is observed under stress conditions is representative of what happens under operating conditions. Depending on how the residual time associated with PBD, the width of the PBD time distribution, and α_{HBD} scale with T, V_G, and T_{OX}, the appropriate reliability methodology will be that of the HBD prevalence ratio model[4] or that of the PBD model.[5–7]

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