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Correlation between the nanoscale electrical and morphological properties of crystallized hafnium oxide-based metal oxide semiconductor structures

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The relationship between electrical and structural characteristics of polycrystalline HfO_2 films has been investigated by conductive atomic force microscopy under ultrahigh vacuum conditions. The results demonstrate that highly conductive and breakdown (BD) sites are concentrated mainly at the grain boundaries (GBs). Higher conductivity at the GBs is found to be related to their intrinsic electrical properties, while the positions of the electrical stress-induced BD sites correlate to the local thinning of the dielectric. The results indicate that variations in the local characteristics of the high-k film caused by its crystallization may have a strong impact on the electrical characteristics of high-k dielectric stacks. © *2010 American Institute of Physics*. [doi:10.1063/1.3533257]

Electrical characteristics of highly scaled devices may exhibit significant device-to-device variability,[1] which is ultimately associated with the discrete nature of charge and matter. Several variability sources, such as random dopant distribution, line edge roughness, gate oxide roughness, and granularity of the poly-Si gate (either during deposition or fabrication), have been identified.[2] In particular, as modeling results have shown, these may lead to variations in threshold voltage and mobility values.[2] Crystallization of the high-k gate dielectrics may also be expected to affect the electrical properties of scaled devices, leading—for instance—to device-to-device variations in the gate leakage current that influences device reliability. However, since standard characterization techniques can provide only averaged information about the electrical properties of devices, addressing the origin of the variability in the nanoscale requires advanced characterization methods with a high lateral resolution. In this respect, scanning probe microscopes have been shown to be powerful tools for characterizing the electrical properties of dielectrics.[3–7] Conductive atomic force microscopy (CAFM) has been widely used to evaluate the electrical conduction of polycrystalline high-k dielectrics. Whereas some studies have suggested that conduction through the polycrystalline films occurs primarily through the bulk of the grains,[8,9] others have demonstrated that the leakage current flows preferentially through the grain boundaries (GBs),[3,7,10,11] which agrees with the results of *ab initio* calculations.[12] Besides generally expected differences associated with the intrinsic properties of the studied materials, such a discrepancy could be caused by the limits of the CAFM lateral resolution, which are close to the characteristic GB width. As a consequence, topography can be directly correlated with current maps only under carefully selected measurement conditions. In this work, CAFM used under ultrahigh vacuum (UHV) conditions, which improve lateral resolution, has been employed to evaluate, at the nanoscale, the impact of crystallization of the high-k material in $HfO_2/SiO_2/Si$ structures on the morphological and electrical properties (and their relation, if any) of the stack.

Gate stack dielectrics consisting of a 5 nm thick atomic layer deposition HfO_2 film and a 1 nm SiO_2 interface layer grown on a Si epitaxial P-substrate were investigated. The gate stack was annealed at 1000 °C, which induced the crystallization of the high-k layer. Following earlier suggestions[13] to achieve the high lateral resolution required to correlate the morphological and electrical properties of the nanocrystalline dielectric, CAFM measurements were performed in UHV ($\sim 10^{-10}$ mbar). Current and topography maps were obtained in contact mode by applying a constant voltage to the tip (substrate grounded). Since under UHV conditions higher resistant tips are necessary to improve the lateral resolution,[13] although their radius is larger than that of other conductive tips, diamond-coated silicon tips were used for the conductivity measurements.[14]

The morphology of the high-k layer was investigated first. Figure 1(a) presents a topographical image showing a surface (1×1 μm^2) with a granular structure. A statistical analysis of the grains shows that their average size is ~ 15 nm,[15] information that is compatible with the grain size obtained from transmission electron microscope images. This granular structure has been attributed to the crystallization of the high-k layer after annealing;[7] grains in the image correspond to individual (or a cluster of) randomly oriented nanocrystals separated by GBs (depressions in the image). Note that direct information about the oxide thickness t_{ox} cannot be obtained from this image because t_{ox} depends not only on the morphology of the scanned top (dielectric/gate) interface [Fig. 1(a)], but also on that of the dielectric/substrate interface, and this information is not independently available in this experiment. However, it is reasonable to assume a similar grain morphology at both interfaces. Therefore, Fig. 1 suggests that t_{ox} is less at the grain boundaries (depression). The width of the GBs has been statistically estimated to be ~ 4 nm. This value is slightly higher than what is obtained from *ab initio* calculations[12] (<2 nm),

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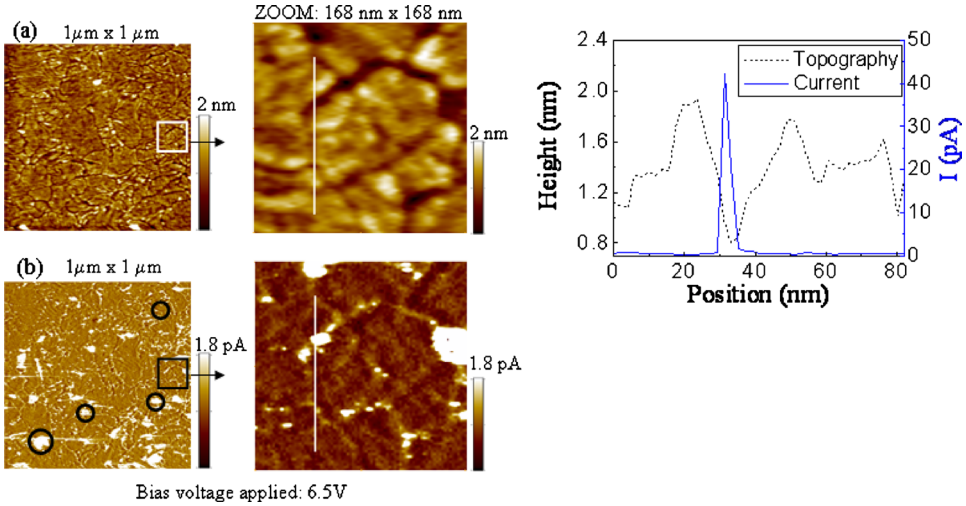

FIG. 1. (Color online) (a) Topographical and (b) current images obtained at 6.5 V of the $HfO_2/SiO_2/Si$ structure (area of 1×1 μm^2). A granular pattern is associated with the presence of nanocrystals. A zoom-in of both images is also shown. Circles in the current image correspond to the BD sites. (c) Topographical (dashed line) and current (continuous line) profiles obtained along the white lines in the zoom-in images show higher leakage current at the topographical depressions associated with the grain boundaries.

probably because we are close to the resolution limits of this technique.

The effect of the high-k crystallization on the electrical properties of the gate stack was investigated based on the image of the leakage current through the film [Fig. 1(b)] measured at 6.5 V at the same surface region as in Fig. 1(a). Note that in Fig. 1(b) a granular pattern overlaps with that of the topographical image (an enlargement of both images is also shown); leakage sites with current values on the order of picoamperes above the background level, which was measured over the nanocrystals, are mainly located at GBs.[16,17] For example, Fig. 1(c) shows topographical (dashed line) and current (continuous line) profiles across the white line plotted in Figs. 1(a) and 1(b) (zooms). Note that the positions with higher currents (leakage sites) are located along the topographical depressions associated with GBs. This qualitative observation has been verified statistically. Figure 2 shows the Z-axis relative position (Z_{rel}) of more than 70 leakage spots (exhibiting a current greater than 0.5 pA) with respect to the Z-axis mean value of the image, which has been arbitrarily considered to be the zero-reference level (dashed line) versus their maximum current. Note that most of the leakage sites are below this reference level (i.e., in the topographical depressions and, therefore, in the GBs). The average size of the leakage sites, those with current values of

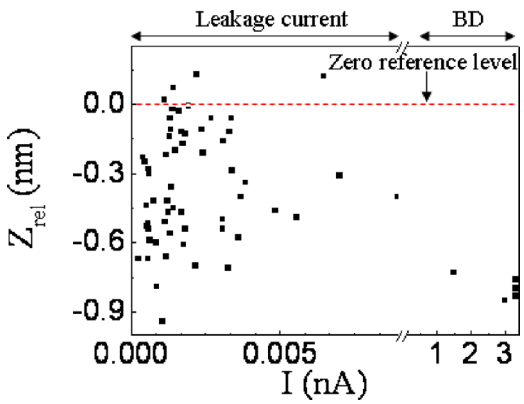

FIG. 2. (Color online) Z-axis relative position (Z_{rel}) of more than 70 leakage spots (with currents greater than 0.5 pA) vs their maximum current. Z_{rel} of a leakage site is defined as the Z-position with respect to Z-axis mean value of the image, which has been arbitrarily considered to be the zero-reference level (dashed line). Note that most are located in topographical depressions (below the reference level), that is, at the GBs.

picoamperes, was also statistically estimated to be ~3 nm, which is comparable to the width of the GBs, consistent with the suggestion that they are confined within the GB region. In addition to these leakage sites, breakdown (BD) sites [in circles in Fig. 1(b)], with currents greater than nanoamperes, can also be identified. These BD events were probably triggered by the constant voltage applied during the scan to obtain the topographical and the current image. Note that the BD spots are much larger (~20 nm) than the leakage spots, suggesting that BD may affect a larger area surrounding the GB. However, within the BD spot, the current measured over the GB region (~nA) is much greater than the current through the adjacent nanocrystals (~pA). Therefore, the results show a clear correlation between the oxide morphology (determined by the crystallization of the high-k layer) and the electrical properties of the gate dielectric: conductivity through the dielectric film is higher along the GBs, and the leakage and BD sites are mostly located near the GBs.

The localization of leakage and BD spots around the GBs could be related to (1) a decrease in the dielectric thickness, as observed on the topographical images, or (2) a higher density of traps at the GB, which could support the trap-assisted tunneling (TAT) current. To determine which factor dominates (if any), we investigated whether there is any correlation between the current through the leakage or BD sites and their Z_{rel}, which reflects the dielectric thickness at a given location: lower Z_{rel} values correspond to thinner dielectrics. Note that, in Fig. 2, two groups of sites can be distinguished. The first corresponds to the sites with the currents in the picoampere-range, where there is no apparent correlation between the leakage currents and dielectric thicknesses. This suggests that the conductivity of the leakage sites is primarily determined by the electrical properties of the GBs, which could be related to the O-vacancies accumulated at the GBs, as pointed out in other works,[12,18] rather than the dielectric thickness across the GB area. The second group in Fig. 2 includes the sites with the current values in the nanoampere-range (BD spots). These sites exhibit lower Z_{rel}'s, which correspond to the locations with smaller dielectric thicknesses. These results indicate that BD in the $HfO_2/SiO_2/Si$ stack is assisted by the higher electric field across the stack. However, the exact mechanism of the BD remains unclear. One of the possible scenarios is that a locally thinner high-k film results in a larger applied voltage

drop across the underlying SiO_2 film, causing its BD and, subsequently, overall stack BD, at this location.[19] Further studies of the HfO_2/metal stacks will help address the role of the electric field in the BD process.

In conclusion, the results show that crystallization of the HfO_2 layer is an important source of the nanoscale variability that affects the electrical properties of the material. As follows from the topography maps, the GBs correspond to the regions of thinner dielectrics. The accompanied current maps demonstrate that the leakage (in the picoampere-range) and BD (in the nanoampere-range) sites are concentrated mostly near the GBs. While the size of the leakage sites is comparable to the width of the GBs, the BD sites seem to encompass much larger areas reaching into the adjacent nanocrystals, although the conductivity across the BD area is still much higher over the GB. The analysis shows that the electrical properties of the GBs (e.g., the presence of the TAT defects) are responsible for their higher conductance than that of the grains. The BD sites were found to be induced primarily at the strongly depressed GB sites, suggesting a significant contribution from the electric field to the overall BD of the multilayer dielectric stack. Further work is needed to clarify the role of the dielectric thickness in the BD mechanism.

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