This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/LED.2010.2045732, IEEE Electron device letters

Recovery of the MOSFET and circuit functionality after the Dielectric Breakdown of Ultra-Thin High-k Gate Stacks.

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Abstract—The reversibility of the gate dielectric breakdown in ultra-thin high-k dielectric stacks is reported and analyzed. The electrical performance of MOSFETs after the dielectric recovery is modeled and introduced in a circuit simulator. The simulation of several digital circuits shows that their functionality can be restored after the BD recovery.

Index Terms—dielectric breakdown, dielectric breakdown reversibility, high-k, resistive switching, CMOS circuits.

I. INTRODUCTION

In highly-scaled technologies, the effect of the MOSFET gate dielectric breakdown (BD) on circuit functionality is not well understood yet [1]. Recently, we have reported a strong post-BD current reduction in MOS capacitors with ultrathin high-k dielectric stacks when the current during the BD transient is limited [2], suggesting that, as sometimes observed for SiO_2 [3-5], BD in these devices is a reversible phenomenon. Since a current limited BD can better represent the BD conditions of MOSFETs within circuits [6], the investigation of the impact of the gate BD reversibility on transistors and circuits performance is mandatory. In this work, we report the evidence of two conductivity states after dielectric BD in transistors with ultra-thin high-k dielectric. The procedure to switch between both states is discussed and the consequences of dielectric BD reversibility on the transistors characteristics and several circuits functionality is analyzed.

II. SAMPLES AND EXPERIMENTAL PROCEDURE.

The transistors used in this work were pMOSFETs with FUSI gate electrode and area 0.35μm^2. The gate dielectric stack (EOT= 1.9 nm) was formed by a HfSiON film (physical thickness of 2.9 nm, 60% Hf) on top of a 1.2 nm SiO_2 interfacial layer. The samples were subjected to a sequence of current limited (CL) stresses until reaching the dielectric BD, plus current non-limited stresses, following a measurement-stress-measurement scheme (Fig. 1). The gate voltage was either ramped (ramp voltage stress, RVS) or kept constant (constant voltage stress, CVS) during the stresses, while the rest of the transistor terminals were grounded. I_G, I_D, and I_S were measured during the stress steps of the sequence. As monitors of the device performance, the transistor I_D-V_D and I_D-V_G characteristics of the fresh sample and those after the successive CL-RVS (or CL-CVS) and RVS (or CVS) stresses were registered.

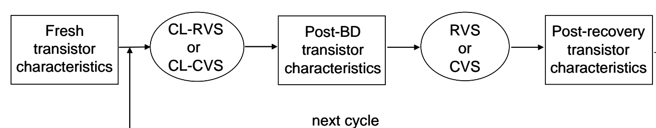

FIGURE 1: Measurement sequence designed to analyze the dielectric BD reversibility. To limit the current during the current limited stresses (CL-RVS or CL-CVS) the compliance of the measurement equipment was used

III. BD REVERSIBILITY PHENOMENOLOGY.

The MOSFET currents measured during the stresses, with or without current limit, have been studied. Figure 2a corresponds to the gate currents during several cycles of RVS stress. Curve I_F (thick line) corresponds to the gate current registered during the first CL-RVS (fresh device). When dielectric BD occurs, at V_{BD}, a fast current increase is observed until the current limit (0.5mA in this case) is reached. The post-BD gate current (I_{BD}) obtained during the following RVS (without current limit) is, as expected, much larger than I_F. However, at a given voltage (V_R), I_{BD} suddenly decreases several orders of magnitude. During the CL-RVS in the next cycle, at low voltages, the gate current (I_R) is larger than the fresh current (I_F) but lower than I_{BD}. This indicates a partial recovery of the insulator properties of the gate dielectric, suggesting that, in some conditions BD in ultra-thin high-k oxides is a reversible phenomenon, i.e., the BD path that was 'opened' can be 'closed'. If V_G continues increasing during the CL-RVS and V_{BD} is reached, BD is observed again, so that a high current level is measured. However, in the next RVS, after V_R, the current decreases again. This behavior can be observed for many iterations of the stress sequence. As an example, Fig. 2a shows the BD reversibility during the 1st, 60th and 200th cycles. Moreover, the phenomenon is qualitatively repetitive from sample to sample. It must be emphasized that during the RVS the voltage sweep is stopped immediately after V_R, to avoid the occurrence of a new BD event. If a BD reappeared during the RVS, BD would become irreversible (because the current is not limited) and the cycling would not be possible anymore [2]. These results indicate that,

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after a current limited BD, two conductivity states are present in the dielectric: a high conductivity one (BD, with gate current I_{BD}) and a low one (R, with gate current I_R). Switching between both states takes place when the two threshold voltages are reached (V_{BD} and V_R) and only if BD is produced under current limited conditions. Fig. 2b shows all the currents through the device during the 200th CL-RVS plus RVS iteration. During the BD state (I_G=I_{BD}), I_D≈I_G, which is indicative of a BD path located close to the drain [7]. This condition is also fulfilled during the R state (I_G=I_R) and is very stable during cycling, which suggests that the same BD path is controlling the stack conductivity during the BD and R states, which is smaller during the R state. Although this paper focuses on BD located close to the drain, because it is the most detrimental condition for the MOSFET performance [9], the same behavior is also observed for BD located in any position along the channel. Once the BD path has been opened, the switching between two different conductivity states in the dielectric can also be observed during CVS tests (Fig. 2c). As an example, during a ~ -2.8V CL-CVS, BD is also detected by a sudden current increase. After that, if a lower voltage CVS is applied, initially the current is larger

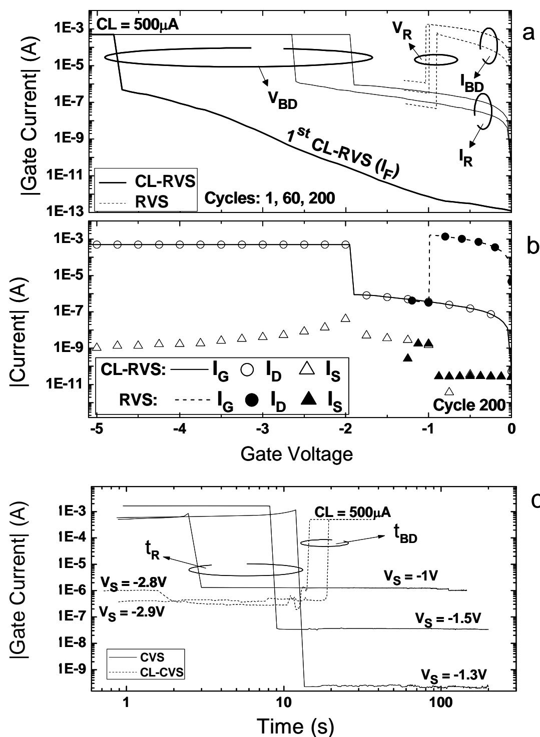

FIGURE 2: a) I_G-V_G curves measured in a p-MOSFET after successive CL-RVS plus RVS iterations. A high current is registered after the current limited BD (I_{BD}) which suddenly drops after V_R. During the CL-RVS in the next cycle , the gate current (I_R) is larger than the fresh current , but lower than I_{BD}, which indicates a partial recovery of the dielectric properties. b) Similar I_G and I_D indicate that the conductive path location does not change in the successive cycles when changing between BD and R states. c) The dielectric BD reversibility can also be observed if a sequence of CL-CVS + CVS is applied.

than the compliance level of the previous CL-CVS but, at a given time, the current decreases drastically and the dielectric partially recovers its insulating properties. This behavior is also repetitive for several cycles. The strong similarities of this phenomenon with the resistive switching mechanism observed in MIM structures for memory applications must be emphasized [2, 8].

The BD reversibility effect on the performance of the transistor has been evaluated from the I_D-V_D and I_D-V_G monitor curves. Fig. 3a (solid circles) shows the I_D-V_D characteristic of a fresh transistor, for different V_G. The I_D-V_D curve of the same transistor after a very hard dielectric BD located close to the drain (Fig. 3b) shows that, during the BD state, the transistor characteristics are completely distorted. However, if the sample is switched to the R state, the I_D-V_D curve is partially recovered (open circles in Fig. 3a). Similar conclusions can be drawn for the I_D-V_G curves (not shown). These results indicate that switching to the R state restores the device functionality, although degraded.

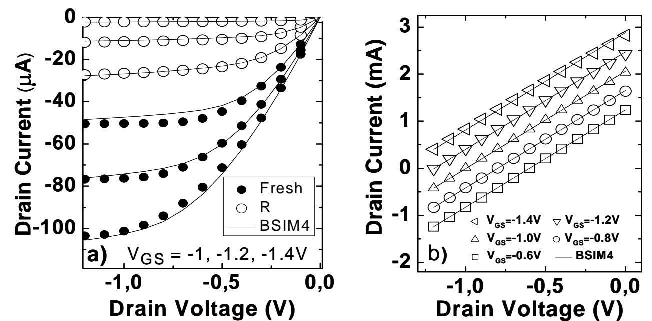

FIGURE 3: (a) Experimental (circles) and simulated (lines) I_D-V_D characteristic, for a fresh (solid circles) and recovered (open circles) pMOS transistor. (b) Experimental (symbols) and simulated (lines) I_D-V_D curves of the same device at the BD state. Dielectric BD took place close to the drain.

IV. BD RECOVERY IN CIRCUITS.

In order to transfer the BD reversibility effects on the transistor up to circuit level, they have been included in the SPICE model that describes the MOSFET performance. A ring oscillator and simple logic gates have been considered as examples. The fresh, BD and recovered transistor characteristics have been described using a combination of the BSIM4 MOSFET compact model (to describe the channel current) plus the D-R gate current model (to account for the BD gate current) [9] (zoom in Fig. 4. top), with model parameters extracted from the experimental data. The modeled characteristics of transistors at the BD and R states (lines in Fig. 3) have been introduced in a circuit simulator to study the performance of a five stage ring oscillator. The BD path has been considered to be located at the drain of the third stage pMOS (Fig 4 top). The circuit output (Fig. 4 bottom) shows that, when at BD, the circuit does not oscillate anymore. However, when back to the R state, the circuit oscillates again, but with a ~2 times lower frequency, which indicates that, after the dielectric recovery, the functionality of the circuit can be restored, although damaged. The functional recovery of logic gates has been also observed. Table 1 summarizes the results obtained in inverters, NAND and NOR gates, always considering that BD takes place in the

drain of a pMOS transistor. For all the circuits under study, some of the outputs are erroneous after dielectric BD (shaded cells). However, the correct logic outputs are always restored when the transistor is switched to the R state.

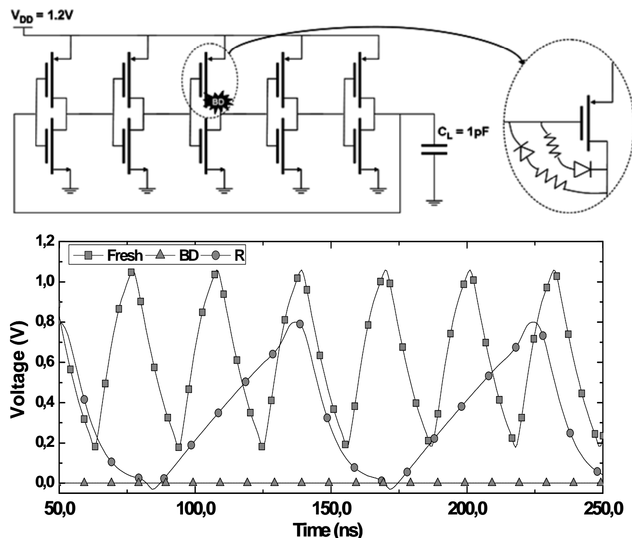

FIGURE 4: Top: A 5 stage ring oscillator was simulated to analyse the effects of dielectric BD and recovery on the circuit functionality. BD has been considered to be located at the drain of the third stage pMOS transistor. The pMOS electrical characteristics have been described using BSIM4 and D-R models (zoom) [TED08]. Bottom: Circuit response when the third stage pMOS transistor is fresh (■), and working at BD (▲), or at R states (●).

Input		INV			NAND			NOR		
A	B	F	BD	R	F	BD	R	F	BD	R
0	0	1	0	1	1	0	1	1	0	1
1	0	0	1	0	1	1	1	0	0	0
0	1	-	-	-	1	0	1	0	1	0
1	1	-	-	-	0	0	0	0	0	0

Table 1: Output logic states obtained for inverters, NAND and NOR gates for fresh transistors (F), after the dielectric BD in one of the pMOS transistors of the circuit (BD) and after switching to the R state of the broken transistors (R). The shaded cells indicate wrong values of the output as a consequence of the BD. Correct logic states are restored when the gate is switched to the R state.

V. CONCLUSIONS.

In ultra-thin high-k dielectric stacks of MOS devices, two post-BD conductivity states can be observed: BD and R, being the current during the BD state (I_{BD}) larger than during the R state (I_R). The switching between both states takes place at threshold voltages V_{BD} and V_R and only if the current is limited during the BD transient. The location along the channel of the BD path remains constant during cycling, even in the R state, suggesting that BD and R conductivity states are controlled by the same conductive path. When the dielectric switches back to the R state, both the isolation dielectric properties and the transistor output characteristics are partially recovered. The MOSFET can be modeled, independently of the dielectric conductivity state (BD or R) using a combination of the BSIM4 and D-R models, with the adequate parameter set. This model has been included in a circuit simulator to analyze the effect of the dielectric BD recovery on the functionality of different logic gates. The simulations show that the circuit response, which sometimes can be wrong after BD, can be restored if the gate conductivity is switched to the R state. This result suggests that, after a gate BD event, the circuit functionality could be recovered and, consequently, depending on the failure criteria, the circuit lifetime increased.

ACKNOWLEDGMENT

This work has been partially supported by the Spanish MICINN (TEC2007-61294), and the DURSI of the Generalitat de Catalunya (2009 SGR-783).

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