Injected Charge to Recovery as a parameter to characterize the breakdown reversibility of ultrathin HfSiON gate dielectric

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***Abstract*— The injected charge to recovery (Q_R) is presented as a parameter to characterize the dielectric breakdown (BD) reversibility in MOSFETs with ultrathin high-k hafnium based gate dielectric. The procedure to recover the dielectric is explained and the dependences of Q_R with the current limit during BD, the polarity of the BD-recovery stresses and the number of stress cycles are analyzed.**

***Index Terms*—dielectric breakdown (BD), BD reversibility, high-k, reliability, resistive switching, CMOS.**

I. Introduction

Gate dielectric breakdown (BD) is one of the most important failure mechanisms in CMOS technologies [1] and it is characterized by a change of the insulator conductivity state from a low (pre-BD state) to a higher one (post-BD condition) whose currents can differ in several orders of magnitude. Traditionally, the conductivity change due to the BD has been considered to be irreversible. However, several years ago it was shown that in SiO_2, in some occasions, BD could be reversible [2], i.e., a low conductivity state could be reached after BD. More recently, we have reported the presence of two interchangeable conductivity states after BD in ultrathin Hf based gate stacks [3], when the current during the BD transient is limited. This phenomenology has strong similarities with the resistive switching (RS) effect [4-6], typically observed in MIM structures with a thicker insulator (several tenths of nm) [5] which today is having an increasing interest for its applications in RRAM devices [6]. From the reliability point of view, the existence of two conductivity states indicates that the insulator properties of the dielectric can be at least partially recovered [7, 8], and consequently, a partial restoration of the device and circuit functionality is produced [8]. However, a better understanding of the reversibility of the dielectric breakdown phenomenon needs large modelling and characterization efforts [9].

In this work, a methodology to study the BD reversibility is described and the charge-to-recovery (Q_R) parameter is presented as a magnitude to characterize the phenomenon. The procedure to recover the low-conductivity state of the dielectric is explained and the dependences of Q_R and gate current with some of the electrical parameters of the BD reversibility tests analysed.

II. Samples and experimental procedure

The samples used in this work were pMOSFETs with FUSI gate electrode and a dielectric stack (EOT=1.9 nm) formed by a HfSiON film (physical thickness of 2.9 nm, 60% Hf) on top of a 1.2 nm SiO_2 interfacial layer. The channel length of the transistors ranges from 1 µm to 0.15 µm, with a fixed channel width of 0.15 µm, which results in area values between ~ 0.15µm^2 to ~ 0.025 µm^2.

A methodology to study the BD reversibility has been developed (Figure 1). Current Limited - Ramped Voltage Stresses (CL-RVS) were applied to the gate to provoke the dielectric BD, followed by a Stepped Ramp Voltage Stress (S-RVS) [10] without current limitation, to recover the dielectric, following an iterative sequence, as shown in Figure 1. During the S-RVS the gate voltage is increased in aprox. 0.1 V every ~150 seconds. In all cases, the duration of the S-RVS was 1200s. Although the BD reversibility can be observed during constant-voltage stresses as well [8], S-RVS were chosen instead to warrant the BD recovery in a reasonable testing time, because the selection of the voltage at which the recovery can be observed during the stress time is critical. Negative voltage CL-RVS were always applied whereas the polarity of the S-RVS could be either positive or negative. The fresh I_G-V_G transistor characteristic was registered after each stress to observe the differences in the gate current between the broken-down (BD) and recovered (R) states.

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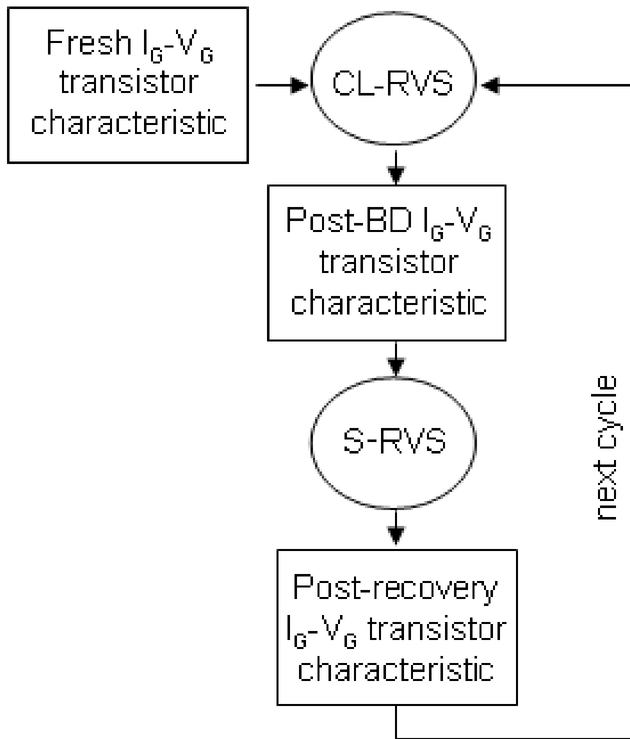

Figure 1: Iterative stress-measurement sequence designed to analyze the BD reversibility.

III. BD REVERSIBILITY PHENOMENOLOGY

Figure 2 shows typical gate currents measured during the CL-RVS stresses used to provoke the dielectric BD. Curve I_F corresponds to the gate current registered during the first CL-RVS (thick line). At breakdown voltage (V_{BD}), the current grows quickly up to the current limit (500uA in this case) and the BD state is reached.

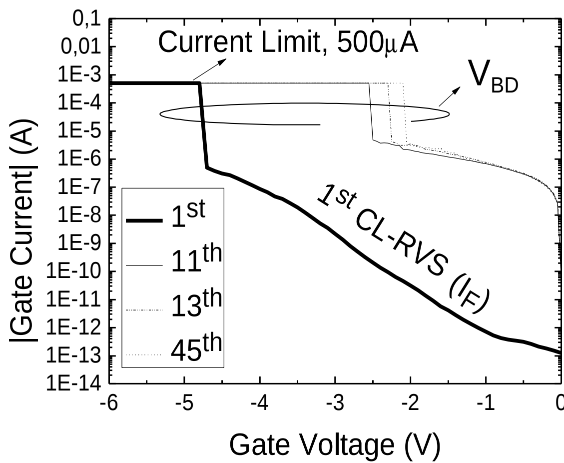

Figure 2: I_G-V_G curves measured during the CL-RVS that lead to the BD state after different cycles of the measurement sequence shown in Fig. 1. At V_{BD}, BD is produced and a high current level is reached (BD state).

A typical example of the gate current (I_G) evolution during the S-RVS is shown in Figure 3, which corresponds to I_G during the S-RVS of the 13th cycle of the sequence. The voltage during the S-RVS, which starts at -0.6V and decreases every 150s until reaching -1.5V, is also indicated in the upper axis of the figure. Initially, I_G is high (~400μA) due to the breakdown provoked during the previous CL-RVS, and increases with the stress voltage at each voltage step (BD state). However, after ~420s of S-RVS, when V_G=-0.95V, I_G suddenly decreases three orders of magnitude, i.e., the dielectric BD recovery (R) is observed, which indicates that the previously 'opened' BD path has been 'closed'[8]. In some cases, as in Figure 3, new recoveries can be observed (R'). If a new CL-RVS is applied after the S-RVS, the current trend shown in Figure 2 is again observed (thin curves) and a high current level will be measured in the next S-RVS until a new recovery is reached. This behaviour is observed for many iterations of the stress sequence shown in Figure 1. Moreover, the phenomenon is qualitatively repetitive from sample to sample. This result indicates that after the first current limited BD is produced, two conductive states are present in the dielectric: a high conductivity one (BD state, with gate current I_{BD}), and a low one (R state, with gate current I_R). The conduction in both states is local and controlled by the same BD path [4]. Switching between both states takes place by applying the adequate gate voltages and only if the BD is produced under current limited conditions.

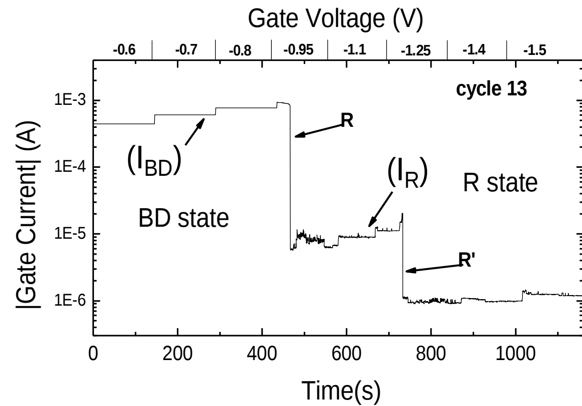

Figure 3: I_G obtained during the 13th cycle S-RVS of the sequence shown in Fig. 1. BD was provoked during the previous CL-RVS. Different recoveries (R and R') can be clearly observed.

Other examples that illustrate different aspects of the I_G evolution during the S-RVS are represented in Figure 4 and Figure 5. I_G during the S-RVS corresponding to the 7th, 11th and 45th cycles in the same sample are shown in Figure 4. As expected, when the oxide remains in the BD state, the current through the gate dielectric stack increases with the gate voltage, with a resistive-like behaviour. However, after the BD reversibility takes place (R state) the gate current seems to be independent of the gate voltage and shows fluctuations that

could be caused by electronic instabilities in the previously opened conductive path [11]. Since the voltage during the S-RVS increases continuously until the end of the stress (1200s), the appearance of new BD events after reaching the R state (Figure 5) is possible. In some cases, the new BD can be recovered again, as it is shown in Figure 5 (R_2), which indicates that the path (or another path), has been 'opened' and 'closed' again. However, in other cases, the new BD event reaches higher currents than the ones corresponding to the BD state (because the S-RVS is not a current limited stress) and BD becomes irreversible, being impossible to observe the BD reversibility anymore [3].

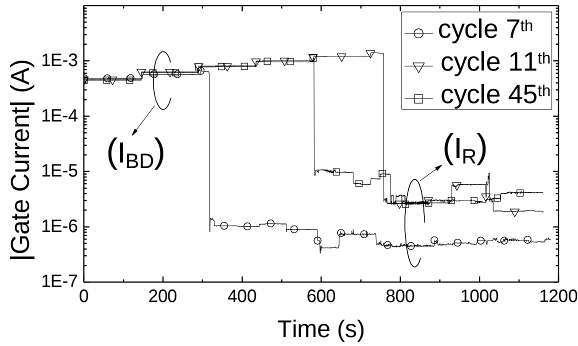

Figure 4: I_G evolution during the 7th, 11th and 45th S-RVS of the sequence in the same sample.

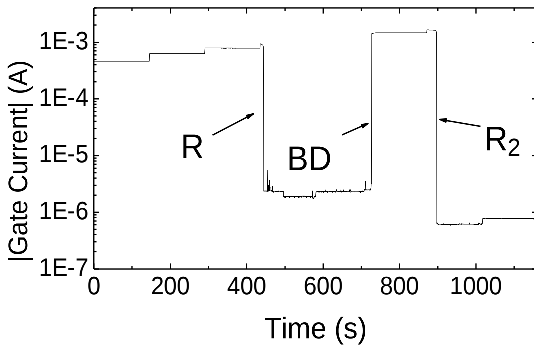

Figure 5: Example of I_G evolution during a S-RVS. New BD and recovery (R_2) events can appear during the S-RVS after the first recovery (R).

IV. Charge-to-recovery analysis

In order to characterize the BD reversibility, in analogy to the charge-to-BD as the parameter to characterize the BD events [1], we propose to use the charge-to-recovery, Q_R, defined as the charge injected in the dielectric until the first recovery event is observed in each of the S-RVS (R in Figure 3 and 5). In the next paragraphs, the dependence of Q_R on the polarity of the S-RVS and the current limit during the CL-RVS will be analysed.

S-RVS polarity dependence of Q_R

To analyse the dependence of Q_R on the S-RVS polarity BD was always produced by a negative CL-RVS whereas positive or negative S-RVS were applied to reverse BD. Figure 6 shows the Q_R values obtained after successive cycles in two samples, one of them subjected to positive S-RVS (open symbols) and the other to negative S-RVS (solid symbols). In the case of positive S-RVS, the BD-recovery sequence was reproducible during more than 600 cycles. From our measurements, no dependence of Q_R on the number of stress cycles was inferred, independently of the polarity of the S-RVS. However, lower dispersion of Q_R values is obtained when the polarity of the CL-RVS and the S-RVS are opposite. To show more clearly this result, the Q_R distributions of the data shown in Figure 6 were drawn in a Weibull plot (Figure 7). A larger dispersion of Q_R can be clearly observed for the samples subjected to negative voltage S-RVS (same polarity as the CL-RVS).

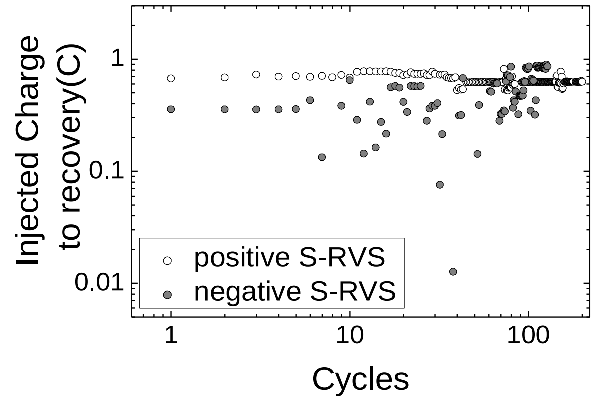

Figure 6: Q_R as a function of the number of cycles. BD state was reached applying a negative CL-RVS in all the cases. However, positive (open cycles) or negative (close circles) S-RVS were applied to induce BD recovery.

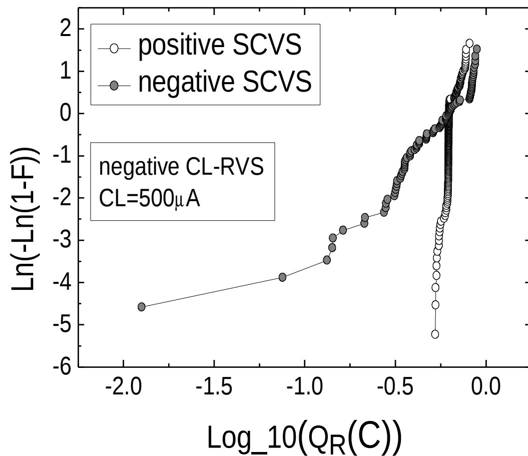

Figure 7: Weibull plot of the Q_R data shown in Figure 6. Samples were subjected to negative CL-RVS followed by positive (open symbols) or negative (solid symbols) S-RVS. Lower dispersion is observed when the polarities of the CL-RVS and S-RVS are opposite.

Dependence of Q_R on the CL-RVS current limit

The dependence of Q_R on the current limit fixed during the CL-RVS has been analyzed. In this study, the samples were subjected to negative CL-RVS to provoke BD (changing the current limit from sample to sample) followed by a positive S-RVS to reverse BD. Figure 8 shows the Q_R distributions obtained in three different samples after successive cycles, whose BD was induced using different current limits. A clear increase of the average value of Q_R with the current limit can be observed.

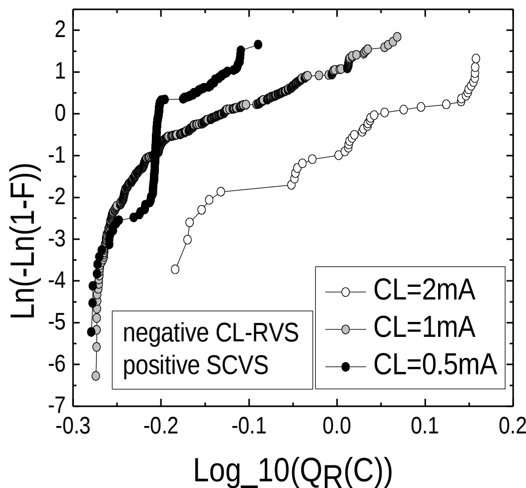

Figure 8: Q_R distributions obtained in samples broken down during CL-RVS with three different current limits. The polarity of the CL-RVS and the S-RVS was negative and positive, respectively. Higher current limit means larger average Q_R.

Dependence of post-BD and post-recovery I_G on the CL-RVS current limit

Figure 9 shows the I_G-V_G characteristics after the dielectric BD (post-BD) and after the BD recovery (post-R in Figure 9) for several cycles of the stress-measurement sequence shown in Figure 1. Several orders of magnitude between the post-BD and the recovered (post-R) gate currents can be observed. On the other hand, for the post BD gate currents represented in Figure 9, two BD modes can be distinguished: SBD (in the 9th cycle) and HBD (rest of the cycles)

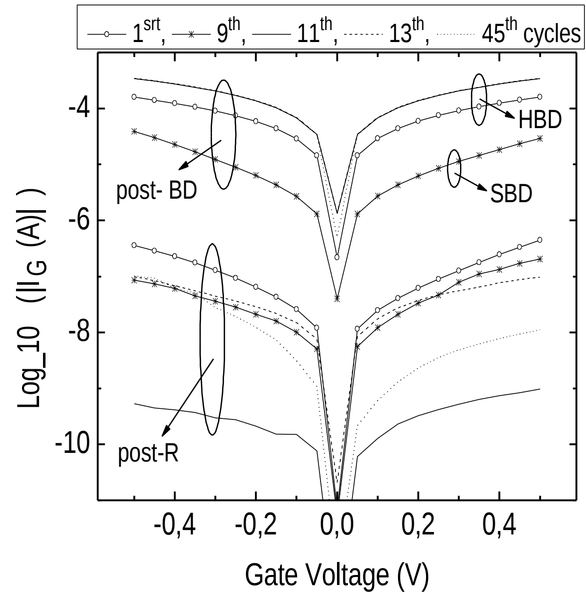

Figure 9: Typical I_G-V_G characteristics registered after the dielectric BD (post-BD) and after the BD Recovery (post-R) for different cycles on the same sample. For the post BD currents, two BD modes are distinguished, SBD (in 9th cycle) and HBD (rest of the cycles).

We have also investigated the dependence of the post-BD and recovered gate currents on the CL-RVS current limit, from the I_G-V_G characteristic registered after each CL-RVS (BD state) and S-RVS (R state). The post-BD and recovered gate currents were measured at V_G = -0,5V in the same samples where the Q_R distributions in Figure 8 were obtained. Figure 10 and Figure 11 show the post-BD and recovered gate current distributions, respectively, for CL-RVS current limits of 0.5, 1 and 2 mA. At the BD state (Figure 10), the gate current clearly increases with the current limit established during the CL-RVS, as has been observed for Q_R (Figure 8). Two regions can be clearly distinguished in Figure 10 for the distributions with the lower current limits of the CL-RVS: on one hand a region with a larger slope which corresponds to higher post-BD gate currents and on the other hand a second region with a lower slope which corresponds to lower post-BD gate currents. Note that these lower current levels correspond to the BD state. In previous papers about dielectric BD, when the dielectric soft BD (SBD) takes place, as in the 9th cycle of Fig.9, lower gate current is observed than for hard BD (HBD) [12]. For this reason, the current levels in the tails of the distribution shown in Figure 10 have been attributed to SBD events, whereas larger currents in the higher slope regions correspond to HBD. Note that we have

used the terms SBD and HBD to refer to the different BD modes observed during the BD state. Therefore, from Figure 10, it can be deduced that the probability to get Hard BD events increases with the current limit used to provoke the BD, as expected. On the contrary, at the R state (Figure 11) no relevant dependences of the gate current with the current limit are inferred. In summary, the current limit used to switch the sample to the BD state will influence Q_R, the BD mode and, consequently, the post-BD gate current, but it will not affect the current at the R state.

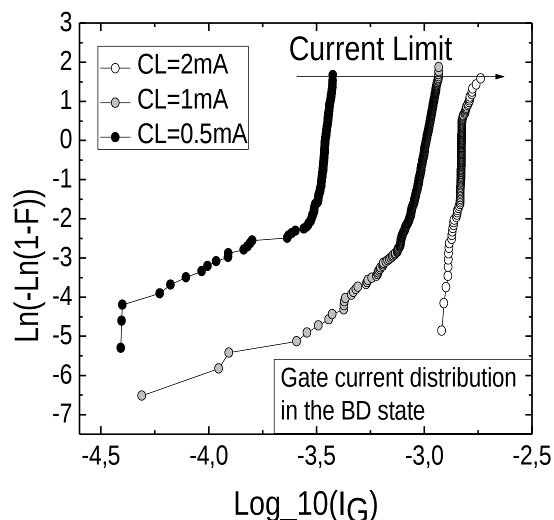

Figure 10: Post-BD I_G distributions, obtained after each CL-RVS for three different current limits, in the same samples of Figure 8.

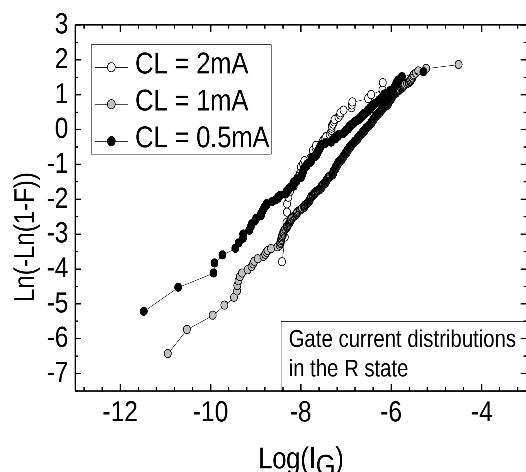

Figure 11: Recovered I_G distribution, obtained after each S-RVS, in the same samples of Figure 8 and Figure 10.

V. Conclusions

A procedure to analyse the gate dielectric BD recovery in transistors with ultrathin high-k gate dielectric has been presented, which allows to switch between the two post-BD conduction modes: BD and R states with the current during the BD state larger than during the R state. To switch to the BD state, current limited ramp voltage stresses (CL-RVS) are applied whereas to provoke the BD recovery the samples are subjected to a non-limited current S-RVS stress. The injected charge to the first recovery (Q_R) during the S-RVS has been proposed as a parameter to describe the BD reversibility phenomenon. The methodology has been applied to study some details of the BD-recovery process from the dependences of Q_R on the electrical test parameters. No dependence of Q_R with the number of iterations of the BD-recovery sequence has been observed. In addition, lower Q_R dispersion is obtained when the polarities of the CL-RVS and the S-RVS are opposite. On the other hand, Q_R and the BD state current increase with the current limit fixed during the CL-RVS. At the BD state, SBD and HBD modes can be observed and the probability of HBD increases with the current limit. However, a negligible dependence of the current during the R state with the CL-RVS current limit has been measured. How all these properties of the BD-recovery process affect the overall reliability of the device should be the aim of further analyses.

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