Temperature dependence of the Resistive Switching-related currents in ultra-thin high-k based MOSFETs.

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Abstract— In this work the temperature dependence of the resistive switching phenomenon in Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFETs) with an ultra-thin Hf-based high-k dielectric is studied through analysis of the gate and drain currents for the two dielectric conductivity states. These two different conductive states of the resistive switching have been associated with the Dielectric Breakdown (BD) and Dielectric BD Reversibility (R), respectively, and are related to the creation of a BD path through the dielectric that can be understood as a conductive filament. The results of the temperature dependence of the post-BD gate current are in agreement with those obtained from the study of the injected charge to recovery, which is a useful parameter with which to analyze the switch from the high to low conductivity state. The drain current in the MOSFETs for the two conductivity states, for different locations of the BD path along the channel (close to the source and close to the drain), and at several temperatures has also been studied. The results contribute to a better understanding of the resistive

switching phenomenon in ultra-thin gate dielectrics. This contribution could be useful for the developing of models to describe BD reversibility.

Index Terms—dielectric breakdown (BD), BD reversibility, high-k, reliability, CMOS, resistive switching, MOSFET

I. INTRODUCTION

One of the most important failure mechanisms in Metal-Oxide-Semiconductor (MOS) technologies is the gate dielectric Breakdown (BD) [1]; a state where the insulator conductivity changes (switches) from a low conduction state to a larger one with a current difference of several orders of magnitude. In deep submicron Complementary Metal-Oxide-Semiconductor (CMOS) technologies, high-k materials have been introduced to overcome the leakage problems associated with the scaling of SiO_2 as the gate dielectric and, hence, a complete analysis of the dielectric BD on these high-k materials is needed [2]. Recently it has been reported that dielectric BD in ultra-thin Hf-based high-k gate dielectric stacks can be a reversible phenomenon, with two interchangeable conductivity states in the dielectric that can be reached by applying the correct stress scheme and a current limited stress during the BD transient[3,4]. Moreover, it has been shown that when the dielectric switches back from the high conductivity state to the low conductivity state the device performance is partially restored and the circuit lifetime is increased [5].

A change between different conduction states in the dielectric material also characterizes the resistive switching (RS) phenomenon usually observed in Metal-Insulator-Metal/Metal-Insulator-Semiconductor (MIM/MIS) capacitors with a thick insulator (several tenths of a nanometer), which is being widely investigated as the operation principle of Resistive Random-Access-Memory (RRAM) non-volatile memories. This principle can be understood as the formation of a conductive filament that can be closed again, i. e. by destruction of the filament. Recently the similarities between the RS and the BD/recovery mechanisms have been reported and the authors suggest that the mechanisms can actually have the same origin[6]. Therefore, the exhaustive characterization of the RS phenomenon in ultra-thin high-k dielectrics has a twofold interest: one, for the development of memory devices based on this phenomenon and the other, from a reliability point of view, for the development of models that can help to evaluate the device and circuit performance and reliability. In this work, the temperature dependence of the resistive switching phenomenon in such ultra-thin films is studied through the analysis of the gate and drain currents in a MOSFET when the dielectric is at the low or high conductivity states. A recently presented stress methodology is used, which allows better control and characterization of the BD recovery process [7].

II. SAMPLES AND EXPERIMENTAL SET-UP

The samples used in this work were pMOSFETs with a Fully-Silicated (FUSI) gate electrode and dielectric stack Equivalent-Oxide-Thickness (EOT)=1.9 nm formed by an HfSiON film (2.9nm physical thickness) on top of a 1.2nm-thick SiO_2 interfacial

layer. Transistors with varying widths (ranging from 1μm to 0.15 μm) and having the same channel length (0.35 μm) were used. To characterize the BD reversibility, the stress-measurement scheme depicted in Figure 1 was adopted. After the measurement of the fresh electrical transistor characteristics (I_G-V_{GS} and I_D-V_{DS}) the samples were subjected to a stress sequence which consisted of a current-limited ramp voltage stress (CL-RVS) to provoke the dielectric BD (i.e, change from the low to the high conductivity state, or BD-state), plus a stair-case voltage stress (SCVS) without current limitation to recover the dielectric (i.e, switch back to the low conductivity state, R-state). An SCVS was chosen to switch to the low-conductivity state instead of the standard RVS because SCVS allows for the evaluation of the injected charge to recovery, Q_R, which has been shown to be a useful parameter to characterize the BD recovery [7]. Both stresses were applied to the gate with the rest of the terminals grounded. During the SCVS the gate voltage was decreased, starting from -0.6V, by approximately -0.1V every ~ 150s until a maximum of -1.3V at 1200s. After each CL-RVS and SCVS, the transistor characteristics were again recorded. In each sample the iterative sequence in Figure 1 was repeated for many cycles. The temperature of the measurements was increased in the same sample every 20 or 40 cycles, during which the temperature was maintained constant, and upon completion the temperature was increased by 50ºC starting from 25ºC and increasing up to 175ºC (Fig.1).

III. RS-RELATED GATE CURRENTS

Figure 2 shows the gate currents in a pMOSFET with W/L=1μm/0.35μm and at 25ºC during the CL-RVS (Figure 2a) and SCVS (Figure 2b), for the 1st, 3rd and 10th

cycles of the measurement sequence (Fig. 1). In Fig. 2a, I_{FRESH} corresponds to the gate current measured during the first CL-RVS (continuous line). At ~-5V a sudden increase of the gate current up to the current limit (500 μA in this case) is observed, which indicates that the dielectric BD has taken place and a conductive filament (BD path) has been created in the dielectric (forming phase) leading the dielectric to the BD state. After BD, the gate current measured during the following SCVS (continuous line in Figure 2b) is, as expected, greater (I_{BD}) than in the fresh device. However, at a given time a fast current drop of several orders of magnitude is observed (I_R), which indicates BD recovery; i.e., the BD path which had been 'opened' in the previous CL-RVS has been closed, reaching the low conductivity state (R-state).

In successive cycles, the BD path is again opened (at V_{BD} during the CL-RVS, Fig. 2.a) and closed during the SCVS (Fig. 2b). This change between stet high and a low conductivity state in the dielectric is observed for many iterations and is qualitatively repetitive from sample to sample [6].

In order to analyze the effect of temperature in the switching process, the sample temperature has been raised during cycling and Q_R was calculated in each iteration from the I_{BD} and time values until the first recovery event during the SCVS of each cycle (Figure 2b)[7]. Figure 3 shows the cumulative probability function of Q_R distributions measured in the same sample when the temperature was increased from 25ºC to 175ºC (with 50ºC increments) every 20 cycles. Concerning the steeper region of the distributions, Q_R dispersion increases when the temperature is increased. On the other hand, a clear decrease of the mean value of Q_R with temperature is observed; i.e., the injected charge needed to change from the high to the low conductivity state decreases

with temperature. A direct relation between Q_R and the degradation level of the BD path (i.e. the difficulty of the BD event) has been established (the more difficult the BD event, the larger the Q_R)[7], so that the results in Figure 3 seem to suggest that the damage (loss of insulator properties of the dielectric) created in the dielectric during the current-limited BD transient decreases with temperature. If a filamentary character of the BD path is considered, a lower I_{BD} measured when increasing the temperature could be caused by the higher resistance of the dielectric. Since Q_R depends on I_{BD} and time-to-recovery (Fig. 2b) the temperature dependence of these magnitudes has been analyzed showing that as the temperature increases, not only does the I_{BD} current decrease but also the time needed to reach the R state. Note that this time decreases linearly with temperature (Table I). Therefore, increasing the temperature favors the switching to the low conductivity state.

The temperature dependence on the RS-related gate currents in the device; namely the post-BD and the post–R I_G-V_G characteristics obtained after each CL-RVS and SCVS, respectively; have been analyzed for the different temperatures. The I_G-V_G curves are symmetric for both voltage polarities and for the two dielectric conductivity states. Figure 4 shows the I_G evolution with cycling measured at V_G = -0.5V after the BD transient (post-BD currents, red circles) and after the BD Recovery (post-R currents, open circles). Figure 4 shows that, though the current through the BD path is approx. constant within each of the isothermal cycles sets, the post-BD I_G decreases with temperature. This could be interpreted as a smaller amount of damage in the dielectric during the BD transient with increasing temperature or as a temperature dependent post-BD gate stack conduction mechanism. Contrarily, at the R-state no temperature dependence is observed

on the post-R I_G. Further studies are needed to explain these temperature dependences of the post-BD and post-R gate currents.

IV. DRAIN CURRENTS DURING SWITCHING

The effect that the gate stack BD event and BD recovery at different temperatures have upon the drain transistors' electrical characteristics has been analyzed. To perform a more complete analysis, different locations of the conductive BD path along the channel were considered, which paths were determined using the method presented in [8]. Figure 5a shows the fresh and post-R I_D-V_{DS} characteristics measured in two samples with the BD path located at the source or drain. Independent of the BD path location, after the BD recovery the I_D-V_{DS} curves resemble those of a fresh device, which indicates that the device can still operate as a MOSFET but with a large reduction of the drain current [6]. Contrarily, when the characteristics are measured during the BD state the transistor characteristics are completely distorted (Figure 5b). However, the I_D-V_{DS} shape depends on the BD path location along the channel; when the BD path is located close to the drain (triangles) the drain current mainly flows between drain and gate through the BD path. As a consequence, a purely resistive behaviour in the I_D-V_{DS} characteristic is observed which should be attributed to the resistance offered by the BD path (note the zero-crossing of the drain current at V_G=V_D, i.e., when no voltage is applied to the path). When the BD path is located close to the source (circles) a very low drain current is measured (≈10pA). In this case the current through the BD path flows between the gate and source without contributing to the drain current. Furthermore, the low current measured at the drain indicates that there is no channel current contribution when the gate

stack is in the BD state. Please note that the measured behaviour does not depend on the channel width. In summary, in the BD state the transistor loses its functionality not only due to the high current through the BD path but also because the inversion layer is not created in the transistor channel. However, for both BD path locations the I_D-V_{DS} characteristic can be partially restored when the stack is switched to the R state.

The drain current has been studied at different device temperatures and biasing conditions. Figure 6 shows the post-BD drain current measured at V_D=-0.7V for several gate voltages and temperatures during the cycling for BD path locations at the drain (Fig. 6a) and source (Fig. 6b). For the case of BD at the drain, clearly the drain current increases when the gate voltage decreases (in absolute value) in the entire studied temperature range. This can be explained by the larger contribution of the BD gate current towards the drain current, because the voltage drop at the BD-path increases when the gate voltage decreases. At high temperatures the drain current is lower, due to the decrease of the BD path conductivity at high temperatures, as previously observed in Fig. 4. If the BD path is located at the source (Fig. 6b), the drain current is very small (Fig. 5b) and increases with temperature. Moreover, gate voltage dependence is only observed at the lower temperatures. For all the temperatures the drain currents are very low and, therefore, we can conclude that the inversion layer of the MOSFET is never created when the BD path is at the source and at the high-conductivity state.

Figure 7 shows the drain current (normalized to the transistor width) obtained in MOSFETs during the cycling after the BD recovery where the BD paths are located at the drain (Fig. 7a) and source (Fig. 7b). In this case, no meaningful differences are observed in the drain currents for the two BD path locations and at all temperatures (and

drain currents around 30uA-60uA are measured). Therefore, after the BD recovery the conduction through the BD path has no relevant influence on the transistor characteristics. Moreover, the inversion layer, which could not be formed at the BD state, is always partially restored when the sample switches to the R state so that the drain current is controlled by the channel current. Note that when the stack is at the R state and T is kept constant a progressive increase of drain current is observed (Fig.7), contrary to the observed behavior when the BD path is open (Fig. 6). Additional studies should be done to completely understand this dependence.

From these results it can be concluded that BD is a reversible phenomenon in the typical temperature range of the device operation in a chip, and that the MOSFET performance is partially restored when the BD path is switched off.

V. CONCLUSIONS

In this work the resistive switching phenomenon in MOSFETs with ultrathin Hf based high-k dielectrics have been studied at different temperatures. The two different conductive states of the resistive switching have been associated to the BD and BD recovery of the dielectric. The results show that at high temperature the BD recovery takes place after lower values of the injected charge to recovery, though with a larger dispersion because both the post-BD current and the time-to-recovery decrease with temperature. The dependence of the RS-related currents (gate and drain) on temperature has been analysed. At the BD state the gate current through the high-k stack decreases with temperature whereas, after BD recovery, the gate current does not depend on temperature. The drain current in MOSFETs for the dielectric BD and R states and for

different locations of the BD path along the channel (source and drain) and at several temperatures have been studied. After BD, the MOSFET loses its functionality because of the high current through the BD path (when BD is at drain) and/or the impossibility of forming the inversion layer (BD is at source). However, after BD recovery the gate current contribution to the drain current is negligible and also the inversion layer can be formed so that the MOSFET functionality is restored, though with reduced performance. This behaviour has been observed in the 25ºC – 175ºC temperature range, which leads us to conclude that BD reversibility in MOSFETs can be produced even at the high temperatures that can be reached in a chip. The results reported here represent new features of gate stack conductivity switching which could be very useful for development of models to describe the BD reversibility.

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Table 1:

Temperature [ºC]	25ºC	75ºC	125ºC	175ºC
Mean time to BD recovery [s]	584	446	335	211

Table I: Mean time to BD recovery during the SCVS as a function of temperature.

Figure Captions

Figure 1: Stress-measurement sequence designed to analyze the dielectric BD reversibility. The compliance of the measurement equipment was used to limit the current during current-limited stress (CL-RVS).

Figure 2: Gate current recorded (a) during the CL-RVS necessary to reach the BD state, and (b) during the SCVS necessary to provoke the BD recovery (R-state).

Figure 3: Statistical distributions of the Q_R measured during cycling on the same sample. The 'F' function represents the cumulative probability function of Q_R. Distributions are organized by temperature, which was increased by 50ºC every 20 cycles in the same sample.

Figure 4: The I_G evolution with cycling after BD transient (red circles) and after BD Recovery (open circles). Every 20 cycles the temperature was increased by 50ºC, starting

from 25ºC until 175ºC is reached. Blue lines indicate the mean values at each temperature.

Figure 5: Drain current versus drain voltage measured for (a) fresh and recovered devices, with BD paths located close to drain or source, and (b) after inducing the BD in the same samples.

Figure 6: Drain current measured at different temperatures in devices after BD, when the conductive path is located close to drain (a) or source (b).

Figure 7: Drain current (normalized to the transistor width) measured at different temperatures in devices after the BD recovery when the conductive path is located at the drain (a) or source (b). Similar currents are measured in both cases which stet that after recovery the BD path location has no relevant influence in the transistor electrical characteristics.