Negative Bias Temperature Instabilities induced in devices with millisecond anneal for ultra-shallow junctions

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Abstract

In this paper the NBTI degradation has been studied in pMOS transistors with ultra-thin high-k dielectric subjected to a millisecond anneal for ultra-shallow junction implantation using different laser powers. An ultrafast characterization technique has been developed with the aim of acquiring the threshold voltage (V_{th}) shift in relaxation times as short as possible once the electrical stress is removed. It has been observed that increasing the millisecond anneal temperature reduce the NBTI degradation. These results have been explained in the context of the emission and capture probability maps of the defects.

Keywords

MOSFET, BTI, annealing, threshold voltage, time-dependent variability, emission and capture times, defect passivation.

Main Text

I. INTRODUCTION

Ultra shallow junction formation in deeply scaled CMOS technologies requires the optimization and control of the implanted dopants. To achieve this objective millisecond anneal (MSA) has been shown to be a promising technique for the 32nm node and below [1,2]. On the other hand, Negative Bias Temperature Instability (NBTI), which is characterized by a progressive shift of the transistor threshold voltage (V_{th}) when high gate voltage is applied, is one of the main aging mechanisms in CMOS devices [3,4]. NBTI is associated to charge in trapping defects when a high voltage is applied to the gate of the transistor and is especially relevant at high temperatures [5]. The charge in some defects can be rapidly detrapped, leading to a partial recovery (relaxation) of the damage created by the NBTI stress [6]. The fast NBTI relaxation makes difficult the characterization of this failure mechanism, being necessary the use of special techniques to correctly evaluate the real damage produced by the NBTI stress [7]. Moreover, NBTI is strongly dependent of the fabrication process [8]. In this regard, millisecond anneal (MSA) has been demonstrated to affect NBTI aging [9]. Here we will extend the NBTI relaxation studies, from very short to medium relaxation times, using a new ultra-fast (UF) technique to more accurately characterize the recovery of the NBTI degradation.

Moreover, the results will be interpreted in the framework of the recent advances in the NBTI physics modelling.

II. SAMPLES AND THE EXPERIMENTAL SET-UP

The samples used in this work were pMOS transistors with $HfSiO/Al_2O_3$ dielectric (EOT~14-15Å [1]), TaCN as gate electrode and W/L=10µm/0.15µm. The MSA considered applying laser pulses with low (LLP), medium (MLP) and high (HLP) laser powers. The temperatures achieved during the three types of annealing are estimated to be 1100ºC, 1200ºC and 1350ºC, respectively and the duration of each anneal was around 1ms. To analyse the effect of MSA on NBTI, the transistors were electrically stressed with a constant voltage stress (CVS) sequence of 10s, 100s and 200s applied to the gate to provoke the NBTI degradation. The stress voltages (V_{stress}) ranged from -1.8V to -2.4V. During the stress sequence the drain, source and bulk terminals were grounded. After each CVS time interval, the devices were relaxed for 150s and the threshold voltage (V_{th}) was measured during the NBTI relaxation period using the ultra-fast (UF) set up developed in this work. All measurements were made at room temperature.

To acquire the NBTI relaxation, the UF measurement set-up depicted in figure 1 has been developed in order to register the device V_{th} in times as short as possible after the stress removal. The shorter the first data acquisition time, the better the accuracy prediction of the NBTI degradation. The developed circuit has been designed with the aim of avoiding the open loop operation of the operational amplifier at any moment during the stress and relaxation process. This avoids voltage ripples that could be detrimental for the measurement. The circuit presented in Fig. 1, together with an instrumentation system control, is capable of applying an electrical stress (stress mode) on the gate terminal and subsequently measuring the V_{th} of the Device Under Test, DUT, (measure mode). By means of three switches the stress and measure sequences are controlled. When the switches are in the stress position, the stress voltage is applied to the gate of the DUT with the drain, source and bulk grounded, which provokes the device degradation. In this case the current through the channel is zero because I_{bias} flows through the operational loop. When the circuit is switched to the measure mode, a low drain voltage is applied to the drain, while bulk and source are grounded. In addition, a current through the channel is forced by means of I_{bias}. If the value of I_{bias} is properly chosen, the transistor operates at $V_{gate} \sim V_{th}$. The gate voltage in the ‘measure’ mode (i.e., the device V_{th}) will be acquired by means of an oscilloscope probe and transmitted to a computer by GPIB bus to analyze the signal. All the switches are controlled by means of an instrumentation system and the ‘control’ signal.

Figure 2 shows an example of a typical oscilloscope capture of the gate voltage when the UF technique is used. The sample had a HLP annealing passivation and the stress voltage was -2.1V. The switching from ‘stress mode’ to ‘measure mode’ is produced at time equal to zero. During the stress phase, the oscilloscope registers the stress voltage applied to the gate. When the circuit operation is switched to the measure mode, the gate voltage rapidly changes from the stress voltage to the threshold voltage (V_{th}) of the transistor. Using this set-up, measurements can be done for times as small as 20µs, which allow obtaining information on the NBTI effects for very short relaxation times. The large quantity of data provided by one capture of the oscilloscope can be used to smooth the signal and get higher accuracy in the V_{th} trace. The total V_{th} shift (ΔV_{th}) induced by the NBTI degradation can be easily calculated as the difference between the

measured voltage and the V_{th} values measured prior to the stress (fresh V_{th}). As can be observed in figure 2, immediately after the stress, a shift in V_{th} has been produced due to the NBTI degradation induced during the stress. The V_{th} recovery during the relaxation can be clearly observed. Then, the set-up in figure 1 is useful to characterize the NBTI degradation at very short times after the stress and it has been used for the study of the influence of the MSA on the NBTI.

III. RESULTS

Fig. 3 shows the fresh (non-stressed) I_D-V_G characteristics in linear (left) and semilog (right) scale measured on a device subjected to LLP, MLP and HLP MSA. Clearly, a lower V_{th} is observed for MLP and HLP conditions which suggests a lower defect density when the anneal temperature increases. Fig. 4 shows the experimental NBTI relaxation traces (symbols) after stresses applied to the pMOS samples with different laser power MSA. The symbols until ~0.5ms correspond to the first fast data block captured by the oscilloscope. After that, successive acquisitions were done up to 150s of relaxation in order to measure the NBTI recovery during a larger time range (the mean value of the data captured by the oscilloscope is shown). Note that V_{th} can be acquired with the developed ultra-fast technique just around ~20µs after the electrical stress was removed. Therefore, the set-up presented in Fig. 1 allows the acquisition of ΔV_{th} at very short times, expanding the temporal experimental window to several orders of magnitude, which is crucial for accurate NBTI characterization and modelling [10]. Note that Fig. 4 suggests that the threshold voltage shift in the submillisecond range shows the same trend as in times over the second. As far as the annealing dependence is concerned, Fig. 4 indicates that increasing the laser power significantly reduces ΔV_{th} and, consequently, the NBTI degradation. Consequently the laser annealing conditions (at low, medium and high laser power) have a direct consequence on the NBTI degradation, which could be related to an annihilation of defects at high temperatures during the MSA.

Fig. 5 shows the effect of MSA on NBTI degradation when different stress voltages (-1.8V, -2.1V, -2.2V and -2.4V) were forced at the gate terminal, with the other transistor terminals grounded. The figure shows the results obtained in devices stressed during 10s(left) 100s(centre) and 200s(right). In all the cases the ΔV_{th} has been evaluated at 348µs relaxation time. Figure 5 shows that the measured ΔV_{th} has an exponential dependence on the stress voltage with an exponent around $0.56V^{-1}$ for all the MSA conditions. However, depending on the annealing conditions, different ΔV_{th} shifts will be measured, being always lower for the HLP annealing condition.

IV. NBTI MODELLING

The results above show that BTI aging is affected by the annealing conditions, suggesting, as expected, a change in the device defect distributions. In this section, a physics-based model for BTI [11] will be used in order to quantitatively evaluate the modifications and properties of the defects distributions for the different annealings.

The V_{th} increase caused by BTI can be explained by charge trapping in defects during the stress phase, which can be partially detrapped during the relaxation phase, leading to the partial V_{th} recovery [6]. In this scenario, several factors affect the BTI degradation: 1^{st}, the number of defects in the device (N); 2^{nd}, the observed V_{th} shift when the charge is trapped/detrapped in a defect (η) [12,13]; and 3^{rd}, the probability that a defect is occupied (f_{occ}). At the same time, when a stress/relaxation time sequence is applied to

the device, f_{occ} of a defect is determined by the emission time (τ_e) and the capture time (τ_c) of the considered defect [11,14] which are voltage and temperature dependent [6]. There is one more factor to be considered, that is, 4th, the probability of finding in the device a defect with given τ_e and τ_c, or, in other words, the distribution of defects in the τ_e-τ_c space ($D(\tau_e,\tau_c)$). In a device, defects with a wide distribution of τ_e and τ_c can coexist, and these characteristics times are, somehow, correlated [5]. Some works consider $D(\tau_e,\tau_c)$ as a log-normal bivariate distribution [10], which is described by the mean values, $<\tau_e>$, $<\tau_c>$, their standard deviations, $\sigma_{<\tau e>}$ and $\sigma_{<\tau c>,}$ and the correlation coefficient ρ. Then, the threshold voltage shift dependence with stress and relaxation times can be modelled according to eq. 1:

$$\Delta V_{th}(t_s,t_r) = N <\eta> \int_0^{\infty}\int_0^{\infty} D(\tau_e,\tau_c)\cdot f_{occ}(\tau_e,\tau_c;t_s,t_r)\,d\tau_e\,d\tau_c \quad (1)$$

where $<\eta>$ corresponds to the mean value of η. t_s and t_r are, respectively, the stress and relaxation times. In eq. 1 f_{occ} is the only term affected by the stress voltage and the stress and relaxation times, while the other parameters (N, $<\eta>$, $D(\tau_e,\tau_c)$) are technology dependent. A graphical interpretation of eq. 1 can be found in Fig. 6. Fig. 6a shows f_{occ} calculated for t_s=10s and t_r=100µs using the procedure in [11]. In the graph, red regions correspond to high occupancy probability, while white zones indicate a low probability that the defects are occupied. Clearly, higher occupancy probability is obtained in the region determined by $\tau_c<t_{stress}$ and $\tau_e>t_{relax}$, because a hypothetic defect located in this region will have a high probability to get occupied during the stress and a low emission probability during the relaxation phase. Fig. 6b shows an example of $D(\tau_e,\tau_c)$ with parameters $<\tau_e>=10^{-5}$s, $<\tau_c>=10^{-2}$s, $\sigma_{<\tau e>}=10^5$s, $\sigma_{<\tau c>}=10^6$s and ρ=0.6. The strong reddish area printed in the map means that the probability of finding a defect with those emission and capture times is higher. However, the faded reddish areas mean that there is a low probability of finding a defect with those specific $<\tau>$'s. The intensity of the product $f_{occ}(\tau_e,\tau_c)$ $D(\tau_e,\tau_c)$, i.e., the product to be integrated in (1) (Fig. 6c) indicates the regions that are more populated and have a high occupancy probability, being the main contributors to the BTI degradation. According to eq. 1, the total ΔV_{th} caused at the stress and relaxation conditions in Fig. 6 is proportional to the volume below the surface in Fig. 6c, being the ΔV_{th} – volume ratio equal to $N<\eta>$.

The experimental results in Fig. 4 have been reproduced using the above explained BTI model (continuous lines). To perform the fittings, f_{occ} has been calculated for the experimental stress-relaxation sequence. After that, the optimum $D(\tau_e,\tau_c)$ and $N<\eta>$ have been obtained by applying a basic minimization function algorithm. Note that it is not possible to separate N and $<\eta>$ because the large area of our devices does not permit to identify isolated defects. In Fig. 7, the resulting $D(\tau_e,\tau_c)$ for all the MSA conditions considered in Fig. 4 are plotted. The value of $N<\eta>$ is also indicated. Similar distributions are obtained for the three types of samples, however $N<\eta>$ decreases with the laser power, supporting the suggestion of annihilation of defects at high temperatures during the MSA.

The defects have a higher capture probability (lower τ_c) when the voltage increases. To describe this feature in the framework of the BTI modelling used in this work,

$D(\tau_e,\tau_c)$ has to be varied when the stress voltage changes. We have observed that ΔV_{th} at different voltages can be well reproduced by changing one of the $D(\tau_e,\tau_c)$ parameters, i.e., $<\tau_c>$, and slightly varying the correlation coefficient ρ. Fig. 8 shows the defects distribution in the τ_c-τ_e space, for samples with the HLP annealing condition stressed at different voltages. As expected, $D(\tau_e,\tau_c)$ shifts to lower τ_c values when the stress voltage increases. Figure 9 shows the dependence of $<\tau_c>$ on the stress voltage for the three MSA conditions studied. Note that $<\tau_c>$ exponentially decreases with the stress voltage, with similar slope for the three annealing conditions. Then, the voltage dependence of $D(\tau_e,\tau_c)$ is similar for all the MSA conditions, reinforcing the assumption that the number of defects decreases when the annealing temperature increases. Finally, the exponent in figure 9 is similar to that obtained for isolated defects [15], which suggests that the study presented here can be used to evaluate the average properties of those defects that cause NBTI degradation.

V. CONCLUSIONS

Because NBTI in deeply scaled CMOS technologies is strongly dependent of the fabrication process, in this work, NBTI aging has been studied in samples where Millisecond Anneal technology was used for the implantation of ultra-shallow junctions. To correctly characterize the NBTI degradation, a special set-up was designed and fabricated to measure the NBTI degradation at short times (around 20μs) after the stress removal. The results show that increasing the annealing temperature strongly reduces the NBTI degradation, which has been attributed to the annihilation of defects after the millisecond anneal application. The results have been explained in the framework of the defects capture-emission time maps. The defect distributions for devices with different annealing conditions have been extracted and their dependence with the stress voltage studied. Results show that the NBTI aging can be reduced increasing the anneal temperature mainly because of the lower defect density. However, the defects capture/emission behavior is only weakly affected by the annealing temperature. Moreover, the stress voltage dependence of the distributions is determined mainly by $<\tau_c>$. In conclusion the ultrafast set-up, combined with the modelling approach, presented here can be used to evaluate average properties of those defects that cause NBTI degradation.

Acknowledgement

This work has been partially supported by the Spanish MINECO (TEC2010-16126) (BES-2011-047449) and the Generalitat de Catalunya (2009SGR-783).

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Figure Captions

[1] Fig. 1. Ultrafast setup developed to apply a stress voltage to the gate of the MOSFET under test and to measure the threshold voltage shift when the stress is removed. A feedback loop and the switches in the 'measure' mode force a constant voltage at the gate which is approximately equal to the threshold voltage, which is acquired by means of an oscilloscope probe.

[2] Fig. 2. Oscilloscope view obtained with the set-up in figure 1. During the stress phase, V_{stress} is measured, and once the circuit is switched to the measurement mode, the V_{th} of the transistor is recorded.

[3] Fig. 3. pMOS fresh I_D-V_G curves measured in transistors with W/L=10µm/0.15µm at room temperature, after the MSA. The data is plotted in linear (left) and semilog (right) scales.

[4] Fig. 4. V_{th} shift as a function of relaxation time obtained after stresses at V_{GATE}= −2.1V measured with the UF set-up in Fig. 1. Increasing the power of the laser anneal significantly reduces the NBTI degradation.

[5] Fig. 5. ΔVth shifts as a function of voltage stress applied for different stress times on the devices subjected to different laser power annealing conditions

[6] Fig. 6. Schematic picture of the BTI modelling process. a) The defects occupancy probability map is calculated for t_{stress}=10s and t_{relax}=10^{-4}s according to the procedure explained in [11]. b) Example of the function $D(\tau_e,\tau_c)$ which indicates the distribution of defect in the devices. c) The product $f_{occ}(\tau_e,\tau_c)$ $D(\tau_e,\tau_c)$ takes into account the probability that defects are occupied and their distribution in the τ_e-τ_c space.

[7] Fig. 7. Defect distribution in the τ_c-τ_e space for the samples subjected to different MSA conditions studied. Similar distributions are obtained for the three laser powers considered. However, N<η> (related to the number of defects in the device) decreases with the annealing temperature.

[8] Fig. 8. Defect distribution in the τ_c-τ_e space for the different MSA conditions studied. Similar distributions are obtained for the three laser powers considered. However, N<η> (related to the number of defects in the device) decreases with the annealing temperature.

[9] Fig. 9. Mean capture time $<\tau_c>$ evolution as a function of the stress voltage applied at the gate terminal on the three types of MSA samples.

Figures

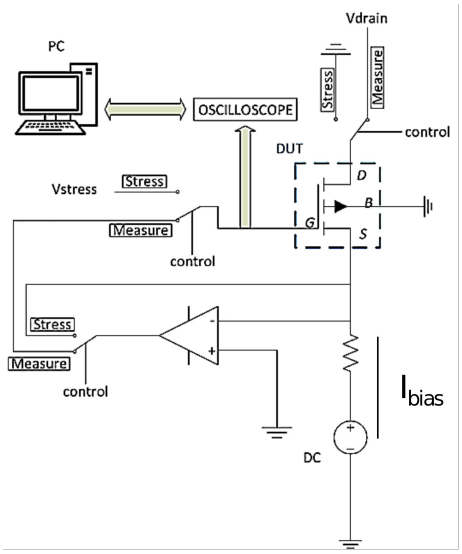

Figure 1

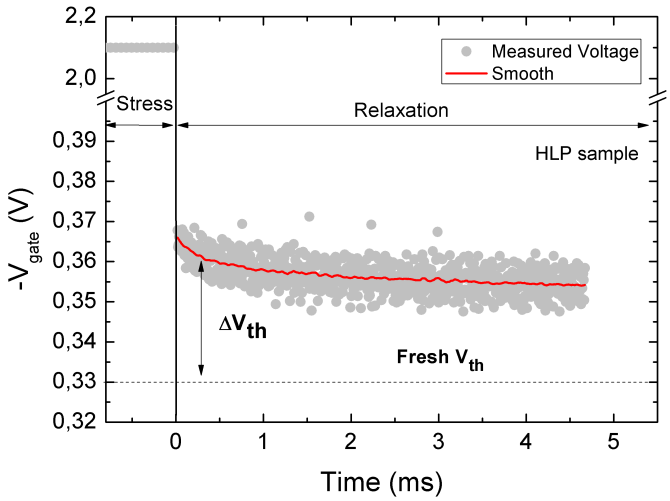

Figure 2

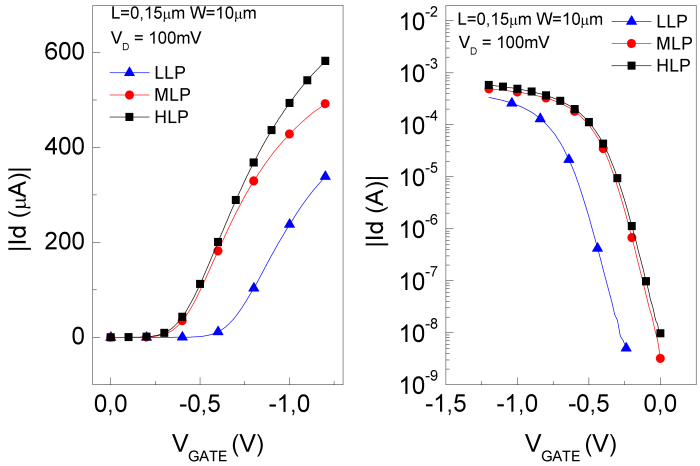

Figure 3

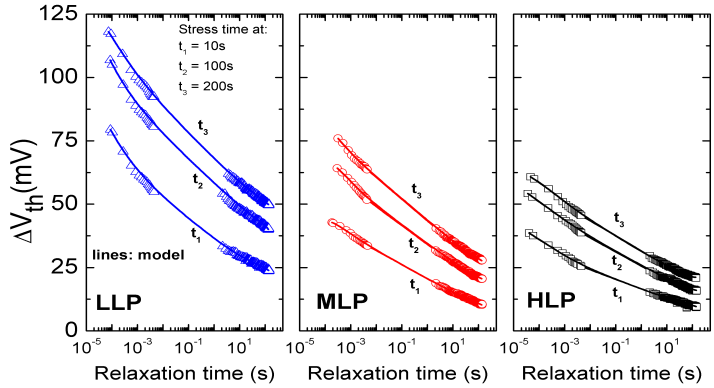

Figure 4

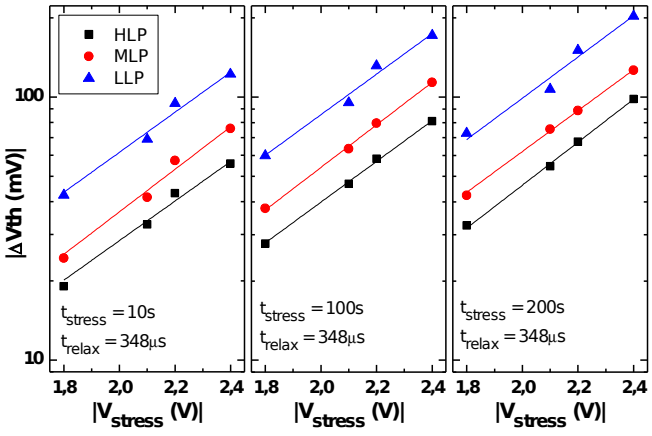

Figure 5

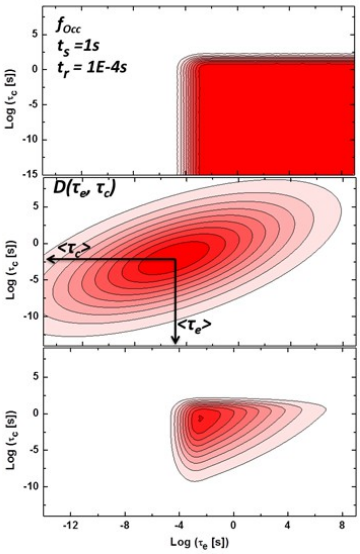

Figure 6

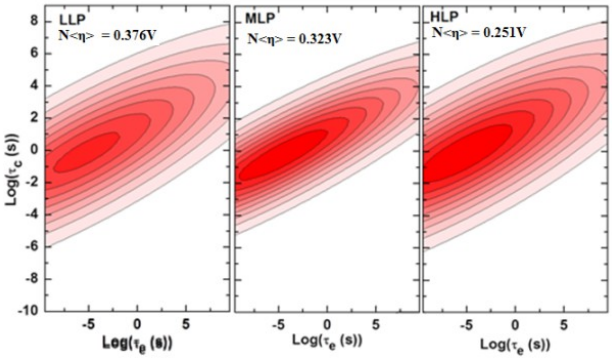

Figure 7

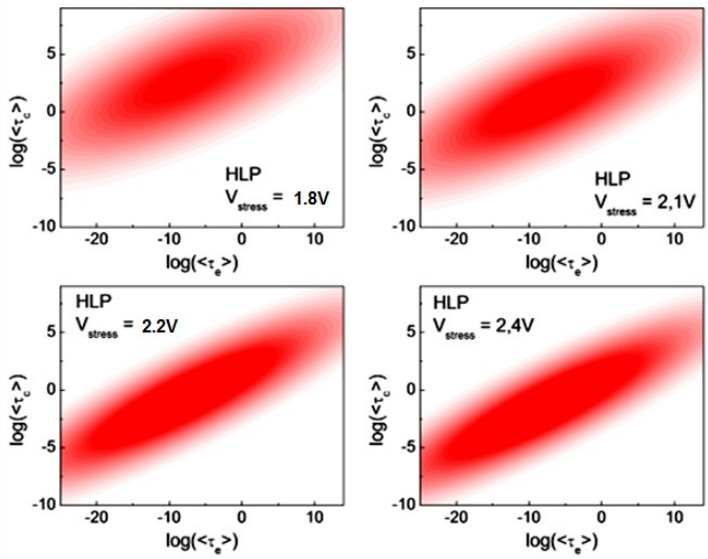

Figure 8

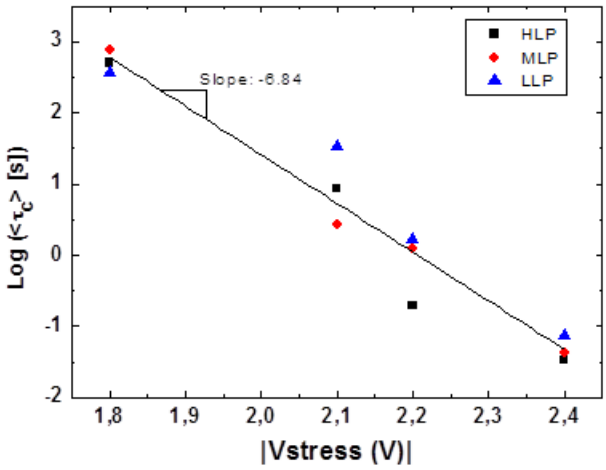

Figure 9

Equations

$$\Delta V_{th}(t_s,t_r) = N \cdot \eta \cdot \int_0^{\infty}\int_0^{\infty} D(\tau_e,\tau_c)\cdot f_{occ}(\tau_e,\tau_c;t_s,t_r)\,d\tau_e\,d\tau_c$$

Eq. 1