Analysis of Set and Reset mechanisms in Ni/HfO_2-based RRAM with fast ramped voltages

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Abstract

The resistive switching phenomenon is analyzed using a purposely developed setup which allows fast ramped voltages and measurements in the time domain. Taking advantage of these capabilities, the Set and Reset processes in Ni/HfO_2 structures have been studied under a large range of voltage ramp speeds. The results obtained show that Set and Reset voltages increase with voltage ramp speed. The use of time domain measurements has allowed concluding that a critical energy is needed to trigger the Set and Reset processes, independently of the biasing conditions.

Keywords: Resistive switching random access memory (RRAM), metal-insulator-semiconductor (MIS), fast ramped voltages, time domain measurements.

1. Introduction[*]

The large efforts devoted to the investigation of Resistive Switching (RS) based memories (RRAMs) is justified by their promising electrical properties [1–3] and scaling ability, so that they could become the future non-volatile memories (NVM) [4–6]. In particular, the RS phenomenon allows changing the conduction of the dielectric material of a MIM or MIS structure between two resistance states, namely low resistance state (LRS) and high resistance state (HRS).

The Set process corresponds to the change from HRS to LRS. It is worth mentioning that during this process a current limit has to be stablished to avoid the complete degradation of the dielectric and therefore of the whole MIS or MIM structure. The HRS to LRS switching is described by the formation of a conductive filament through the dielectric, allowing the current flow. For unipolar switching, which is the case that will be studied in this work, the filament formation is governed by the temperature and field-induced generation of defects [7]. On the contrary, the Reset process leads the device from LRS to HRS. In this case, the previously formed filament is partially broken, blocking the current flow. In the case of Ni-HfO_2-based structures, this mechanism is controlled by thermally enhanced diffusion of Ni atoms induced by local Joule heating in the conductive filament [8,9]. Among other aspects, understanding the dynamics of Set and Reset is crucial to achieve a correct performance of the RRAM devices. In this work, by taking advantage of a setup specifically designed for the RS characterization, the Set and Reset processes are analyzed when fast voltage ramps with different speeds are used. The I-V characteristics, the Set and Reset voltages and the energies associated to both processes are analyzed.

2. Samples and experimental setup

The devices used in this work are MIS structures with Ni/HfO_2/Si stack. The samples were fabricated on (100) n-type CZ silicon wafers with resistivity

between 0.007Ωcm and 0.013Ωcm [10]. After standard wafer cleaning, a wet thermal oxidation process was done at 1100ºC leading to a 200nm-thick SiO_2 layer. This field oxide was patterned by photolithography and wet etching. Prior to the high-k deposition, a cleaning in H_2O_2/H_2SO_4 and a dip in HF(5%) were performed. Subsequently, 20nm-thick HfO_2 layers were grown by atomic layer deposition (ALD) using tetrakis(Dimethylamido)-hafnium (TDMAH) and H_2O as precursors, and N_2 as carrier and purge gas. The deposition temperature was 225ºC. The top metal electrode, consisting of a 200nm-thick Ni layer, was deposited by magnetron sputtering. The resulting structures are square cells of $5x5\mu m^2$.

Fig 1 shows a picture of the circuit developed for the RS characterization (top) and the block diagram of the whole setup (bottom). The circuit consists of two main modules. The first one fixes the current limit that has to be applied to control the Set process, namely the Current Limit Control Unit (CLCU). This module would not be necessary in case that, for example, a serial transistor is included together with the MIS or MIM structure [11] (which would control the current), so that it could be inhibited. The second module is a logarithmic current-voltage converter (Log-IVC), which allows measuring both Set and Reset processes in very short times when connected to an oscilloscope. Moreover, the logarithmic conversion permits to register the current in a window ranging from 100nA to 10mA, without losing relevant information in the low current range as would be the case if linear conversion was used. Then, in this setup, a voltage is applied to one of the terminals of the device under test (DUT), whereas the CLCU is connected to the other to control the maximum current through the DUT; the CLCU is only activated during the Set process, as explained above. A buffer is also connected to this electrode in order to measure the actual voltage drop across the DUT. Then, current through the DUT is logarithmically converted to voltage and acquired by an oscilloscope. The use of the oscilloscope allows increasing the measurement time resolution by taking advantage of its large sampling rate (50000 Samples/s in our case), when compared to the approximately 200 Samples/s of a Semiconductor Parameter Analyzer (SPA) [12].

Traditionally, voltage ramps are applied to the DUT to switch its state, using a SPA. However, in this work, we will use a pulse generator to apply the required voltages. This will allow us the study of the Set and Reset processes in a much larger voltage ramp speed (VRS) range than the one provided by a SPA. Taking advantage of the positive slope of a square pulse, by varying its rise time it is possible to achieve VRS ranging from 35V/s up to 1143V/s, improving in several orders of magnitude the ~0.2V/s larger VRS provided by the SPA. As an example, the maximum VRS was achieved by choosing a pulse amplitude of 8V and a rise time of 7ms, leading to a VRS~1143V/s. The SPA will also be used to cover the low VRS range.

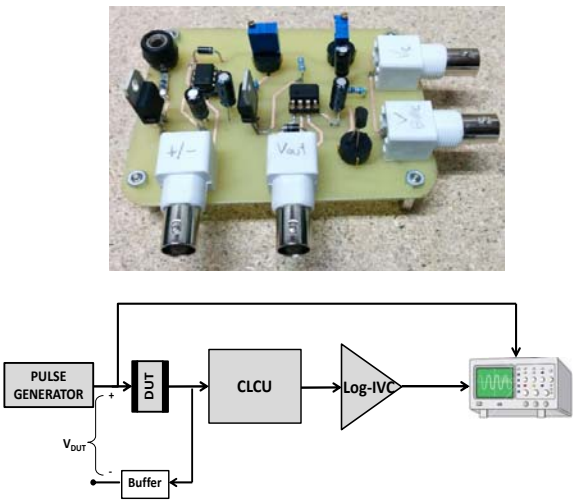

Fig 1: (top) Picture of the circuit designed to characterize the RS phenomenon. (Bottom) Block diagram of the setup. The CLCU will only be required when a current-limiting transistor is not integrated in the memory cell.

3. Results

Using the setup in Fig 1, Set and Reset were sequentially induced on the same DUT at different voltage ramp speeds. Previously, the initial electroforming was performed with an SPA. In Fig 2 both Set and Reset processes are plotted as a function of time. Using the developed setup, complete information on the applied voltage pulse and the registered current, measured by means of the oscilloscope, can be simultaneously obtained in the time domain. Note that the simultaneous

measurement allows reconstructing the standard I-V characteristics, to facilitate RS analysis if necessary.

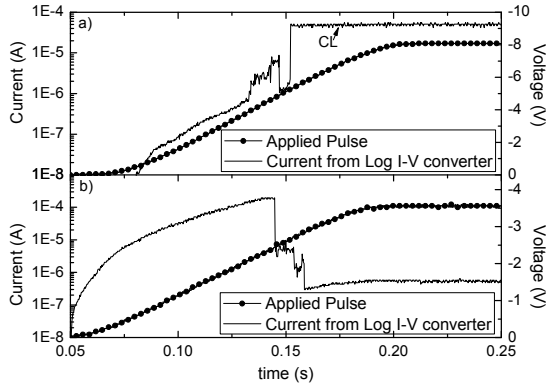

Fig 2: Applied voltage ramps and current registered during a Set (a) and a Reset (b) process using the setup in Fig. 1. The CLCU is configured to limit the current at ~80μA during the Set. In this case a VRS of 80V/s for Set and VRS of 35V/s for Reset have been used.

Fig 3 shows several I-V characteristics of the Set and Reset events for different values of VRS. For comparison, additional measurements performed with an SPA, are shown. From the figure it becomes clear that V_{Set} and V_{Reset} increase with the VRS, suggesting a relevant influence of this magnitude on the deceleration of defect generation and diffusion processes.

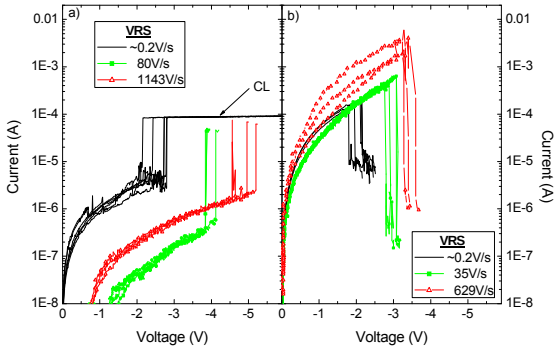

Fig 3: Set (a) and Reset (b) for different VRS. The x axis shows the actual DUT voltage drop. Measurements with a typical SPA (which allows lower ramp speeds than those available with the developed setup) are included for comparison.

This is confirmed in Fig 4, where the mean values of the V_{Set} and V_{Reset} are plotted for the full range of studied VRS. Clearly, V_{Set} and V_{Reset} exponentially increase with VRS, which is consistent with thermally activated Set [7] and Reset [8] mechanisms; the faster the voltage ramp, the higher the voltage required to form or dissolve the conductive filament. These results are in agreement with those in [13], where a deeper analysis was performed in the Reset case taking into account the temperature dependence on the VRS. The strong dependence of voltages on the VRS suggests the existence of a critical energy required to trigger the corresponding process. To corroborate this hypothesis, the energies required for the observation of the Set (ε_{Set}) and Reset (ε_{Reset}) events have been calculated. This can be done from the voltage and current time evolutions registered with the setup (Fig 2), firstly, calculating the power as their product and, next, the energy, by integrating the previous power along time.

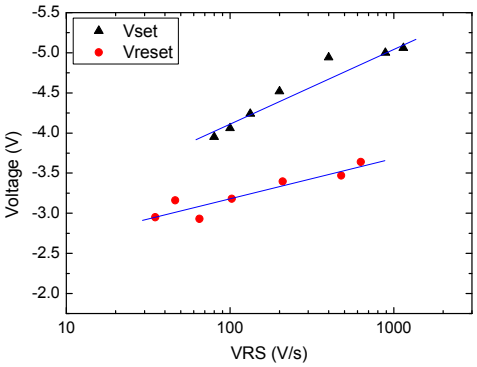

Fig 4: V_{Set} (triangles) and V_{Reset} (circles) as a function of VRS.

Fig 5 shows examples of the power evolution as a function of time during the LRS/HRS, calculated (from traces like those in Fig 2) until the Reset/Set process occurs. In the plot, the LRS power (empty red triangles) is larger than the HRS power (solid black squares) which is consistent with the fact that at LRS more current is passing through the device compared to the current flowing at HRS, provoking the rupture of the conductive filament due to local Joule heating [8].

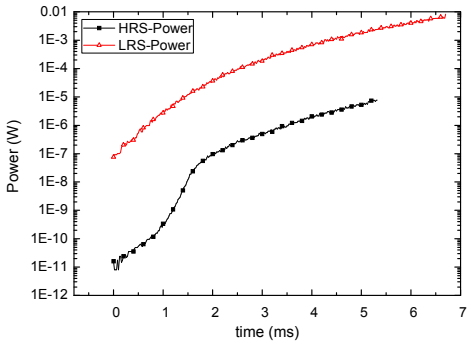

Fig 5: Example of the power at LRS (red triangles) and at HRS (black circles) when VRS=629V/s and VRS=1143V/s respectively. Power during LRS is greater than that during HRS.

Then, the power evolution is integrated along time, to calculate the corresponding energies, for the different VRS applied. In Fig 6, the mean values of Set and Reset energies calculated for the whole range of VRS are plotted as a function of the VRS. Note that no dependence of the energies with VRS is observed. This result suggests that the energy supplied to the DUT controls the Set and Reset processes. Therefore, ε_{Set} and ε_{Reset} are two critical parameters that determine when the Set or the Reset events will occur, independently of the biasing conditions used to trigger them.

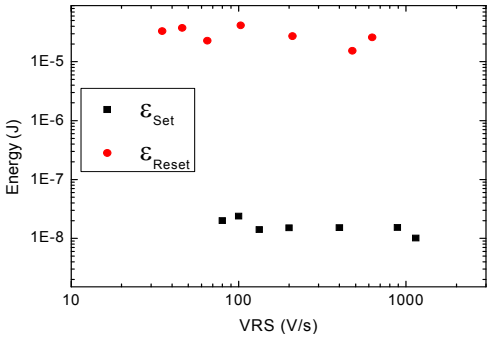

Fig 6: Energy required to trigger the Set and Reset processes as a function of VRS. Both energies remain constant as the voltage ramp speed increases indicating ε_{Set} and ε_{Reset} are critical parameters in the RS phenomenon.

4. Conclusions

An in-house system has been developed to investigate the Resistive Switching (RS) phenomenon in the time domain (with a large time resolution). Using this setup, the Set and Reset processes have been studied in Ni/HfO_2 based RRAM structures, by applying voltage ramps with a wide range of speeds. The results show that the Set and Reset voltages increase with the voltage ramp speed. However, the energies employed to trigger the processes are independent of the biasing conditions, suggesting that this is an intrinsic parameter of the RS mechanism.

Acknowledgements

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