Amorphous silicon mediates a high yield in GaAs nanowire arrays on Si.

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ABSTRACT. GaAs nanowire arrays on silicon offer great perspectives in the optoelectronics and solar cell industry. To fulfil this potential, gold-free growth in predetermined positions should be achieved. Ga-assisted growth of GaAs nanowires in the form of array has been shown to be challenging and difficult to reproduce. In this work we provide some of the key elements for obtaining a high yield of GaAs nanowires on patterned Si in a reproducible way. By modifying the surface properties of the nanoscale areas exposed to growth with the addition of an amorphous silicon intermediate layer between the crystalline substrate and the oxide mask, the size and the contact angle of the Ga droplet are suitably modified, leading to a high yield of vertical nanowire. This work opens new perspectives for the rational and reproducible growth of GaAs nanowire arrays on silicon.

Semiconductor nanowires (NWs) have been the subject of extensive investigations in recent years, motivated in part by the unique physical properties provided by their essentially one-dimensional geometry. These novel properties, as well as new material combinations that can only be achieved with NWs[1,2,3], offer a large number of potentially useful applications in a broad range of electronic, optoelectronic and energy harvesting devices[4,5,6,7,8,9,10]. A particularly useful property is that their small diameter allows their growth on lattice-mismatched substrates[11,12,13]. A natural consequence is that NWs enable the integration of highly functional III-V compounds with silicon-based technologies[14,15,16,17]. This represents a unique opportunity to combine the advantages of III-V materials such as direct band gap and high mobility with Si, which is extensively used in microelectronics industry[18,19].

In the past, regular arrays of NWs have been achieved by patterning a substrate with gold nanoparticles[20,21,22]; such a configuration demonstrated the rational use of NWs, showing their potential integration in mass-production applications. These pioneering works rely on the use of the gold droplets for the nucleation and growth of the NWs through the Vapour-Liquid-Solid process (VLS). However, gold is a non-desired impurity in silicon technology, so other methods have been investigated for the growth of NWs on silicon substrates[23,24,25]. Ga-assisted growth is a successful example showing how this precious metal can be avoided for the growth of III-V NWs on III-V and on Si substrates.[26] Following this method, nanoscale gallium droplets collect arsenic from the gas phase. Subsequent supersaturation leads to the precipitation of GaAs underneath. The Ga droplet should be refilled continuously to ensure a sustainable growth. Applying this method, arrays of GaAs NWs have been obtained on patterned GaAs substrates[27], while fabrication of GaAs NWs on a patterned Si surface has shown to be by far more challenging. One of the main challenges has been the reproducibility in obtaining high yield of vertical GaAs NWs. Key elements such as gallium pre-deposition, thickness and composition of the growth mask have shown to be important parameters for a successful growth[28,29]. Still, successful growths of GaAs NW arrays by the Ga-assisted method are rare in literature[30,31,32].

In this work we bring new elements of analysis for understanding how a high yield can be obtained for the growth of Ga-assisted GaAs arrays on silicon. We have found that the microstructure of the Si wafer, in particular the interface between the Si and the SiO_2 growth mask, is decisive for achieving highly controlled vertical GaAs NWs. Progress in the deterministic GaAs NW growth at selected positions on a Si substrate is the first step towards the rational fabrication of advanced devices on the silicon platform.

We synthesized GaAs NWs by the Ga assisted method using a DCA P600 molecular beam epitaxy (MBE) machine. 4 in. Si(111) wafers have been patterned with arrays of nanoscale holes following standard nanofabrication methods[28,32,33]. First, a 20 nm thick SiO_2 layer has been grown by thermal oxidation on the silicon wafers as growth mask. The holes were defined by electron-beam lithography and wet chemical etching based on 7:1 buffered hydrofluoric acid (BHF) solution (see Supporting Information for further details). The wafers were subsequently diced into 35 × 35 mm^2 square chips for the MBE sample holder. Prior to growth, the substrates were heated to 770 °C for 30 min to remove any possible surface contaminants. In the following we will refer to this process step as *degassing*. The growth was carried out at a nominal Ga growth rate of 1 Å/s, As_4 partial pressure of 2 x 10^{-6} Torr, at a substrate temperature of 630 °C, and with 7 rpm rotation. In some of the growth runs, Ga was pre-deposited to facilitate the formation of Ga droplets. This has been accomplished by keeping the Ga shutter open since the ramp up of the substrate temperature for the degassing step. In the following we specify whether or not such pre-deposition has been performed. The morphology of the samples was characterized by scanning electron microscopy (SEM) and by transmission electron microscopy (TEM). TEM cross-sections were prepared by using a Focus Ion Beam (FIB).

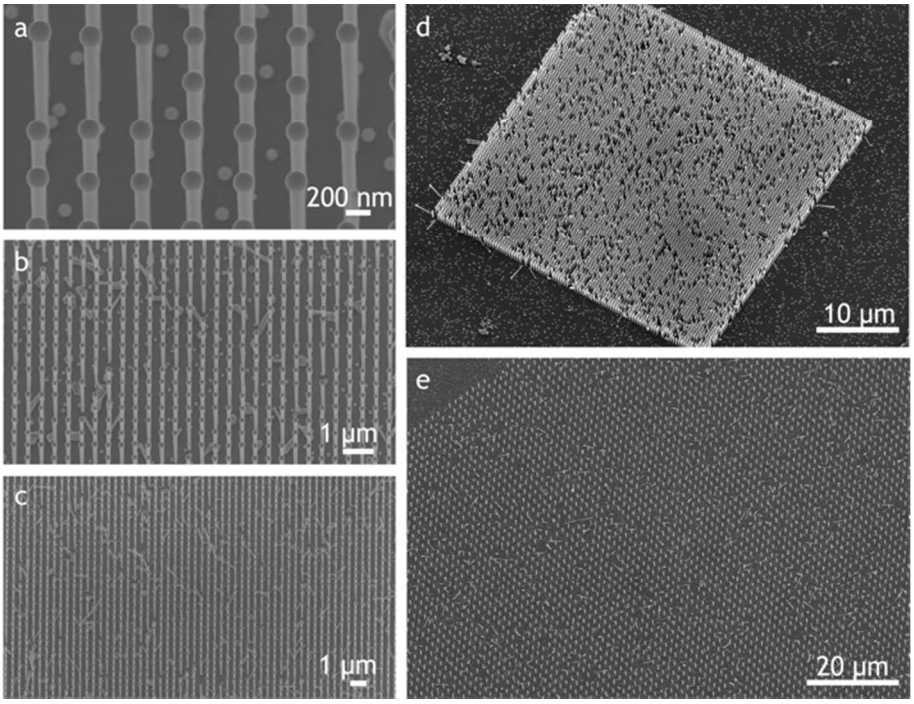

Figure 1. Scanning electron microscopy (SEM) images of GaAs nanowires grown on patterned Si(111) substrates at 630 °C, at a nominal Ga growth rate of 1 Å/s and under an As_4 partial pressure of 2 x 10^{-6} Torr. (a-c) are 20° tilted images and (d-e) are tilted views with additional in-plane rotation. The yield of vertical nanowires is 80%. The hole diameter size is 90 nm for all the images. The interhole distance is 400 nm in (a-d) and 1600 nm in (e).

SEM micrographs of successful GaAs NWs arrays grown on a Si(111) substrate are shown in Figure 1. Figure 1a-d show tilted views of the NWs grown in patterns with a nominal hole diameter of 90 nm and an inter-hole distance of 400 nm at different magnification and with additional in plane rotation (d). Figure 1e shows the results for a larger inter-hole distance (1600 nm). The NWs are uniform in length and diameter. They present a slightly inverse tapering and a Ga droplet at their tip. The yield of vertical NWs - defined as number of openings nucleating vertical NWs divided by the total number of openings in the array - is 80%. The yield is independent from the inter-hole distance of the array. The majority of holes not leading to the

formation of vertical NWs correspond to a failure in nanowire nucleation, while only few consist of tilted NWs. This could be due to an incomplete definition of the holes by the e-beam lithography. An optimization of the pattern definition could in principle lead to an improved yield of vertical wires.

As found by other groups[29,34], the gallium pre-deposition step has a strong influence on the yield of vertical NWs. Figure 2 (top) shows representative SEM images of the growth results obtained with and without the Ga pre-deposition, keeping all the other growth parameters unvaried. The two substrates originated from the same wafer, which we refer as *Wafer 1*. As we can see in the picture, omitting the Ga pre-deposition step leads to an extremely low yield of vertical wires and a high density of non-vertical wires and parasitic growth. An identical set of growths, with and without the Ga pre-deposition, has been performed on a similar Si wafer of a different batch. We refer to these two samples as *Wafer 2*. Fig. 2 (bottom) shows the results of the growths. In this case, irrespective of the Ga pre-deposition, the yield of vertical wires is very low. Instead, many tilted wires and parasitic growth are found on the substrates.

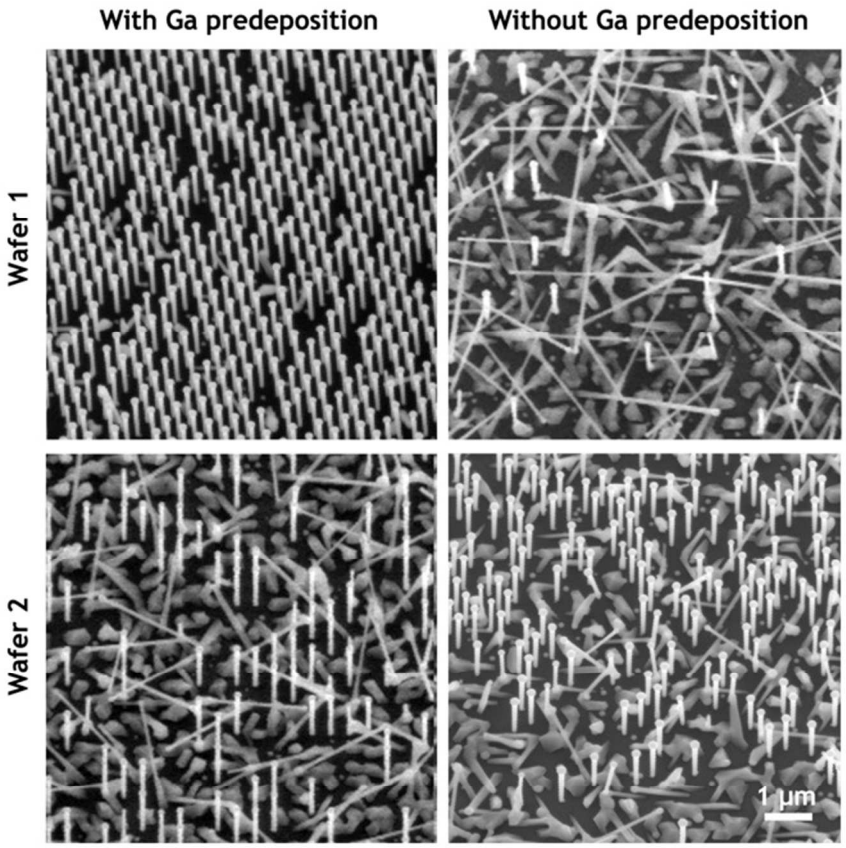

Figure 2. Tilted SEM micrographs of GaAs NWs grown in arrays defined on two different 4 in. wafers (Wafer 1 and Wafer 2) with and without the pre-deposition of Ga droplets. (Top) For the growth on Wafer 1, the yield of vertical wires strongly depends on the Ga pre-deposition. (Bottom) For the growth on Wafer 2, the yield of vertical nanowires is very low in both cases. For all the images the interhole distance is 400 nm and the hole diameter size is 90 nm.

The discrepancy between the results obtained on the two wafers was unexpected, since *Wafer 1* and *2* had been subject to identical sample preparation and growth protocols. This prompted us to investigate the characteristics of what were supposed to be identical substrates in detail. To this purpose, lamellas containing cross-sections of the substrates were prepared by focus ion beam (FIB).

We start by analysing the structure of the Si chip in a region outside the pattern. Figure 3 displays cross sectional high angle annular dark field (HAADF) images of representative samples of *Wafer 1* and *Wafer 2*, taken at the interfaces between Si and the thermal SiO_2, and the corresponding energy-dispersive X-ray spectroscopy (EDX) maps. The same analyses have been performed on four chips, two of *Wafer 1* and two of *Wafer 2*. Two samples correspond to remaining wafer pieces which had not been loaded in the MBE reactor, i.e. they have been analysed just after the sample preparation; the other two have been analysed at the end of the growth process and correspond to the samples depicted in Figure 2.

We start by considering the pieces not loaded in the MBE (Figure 3a-b). Surprisingly, the sample from *Wafer 1* shows an unexpected amorphous layer between the crystalline silicon and the SiO_2. This 13 nm thick layer consists of amorphous silicon, as confirmed by the lack of oxygen in the EDX analysis. The interface between amorphous silicon and crystalline silicon is relatively rough. Conversely, the piece from *Wafer 2* shows the thermal oxide layer directly on top of the monocrystalline silicon, as one would expect from the sample preparation. The SiO_2 layer of the chip from *Wafer 1* has been found to be rather non uniform, with thickness ranging from 10 to 20 nm, unlike for *Wafer 2* sample, although an identical dry oxidation has been performed on the wafers. The analysis of the chips after growth is shown in Figure 3c-d. In this case, for both samples only thermal oxide is found on the crystalline silicon. Since the crystallization of amorphous silicon starts at temperatures higher than 500°C, we think that it has crystallized during the heating of the substrate in the growth chamber[35,36]. Our Si provider suggested that the amorphous layer was generated by the mechanical treatments such as slicing and lapping and by an insufficiently long chemical mechanical polishing (CMP) step at the end

of the substrate preparation. We believe indeed that the large thickness of the layer of amorphous silicon layer prevented its full crystallization during the thermal oxidation.

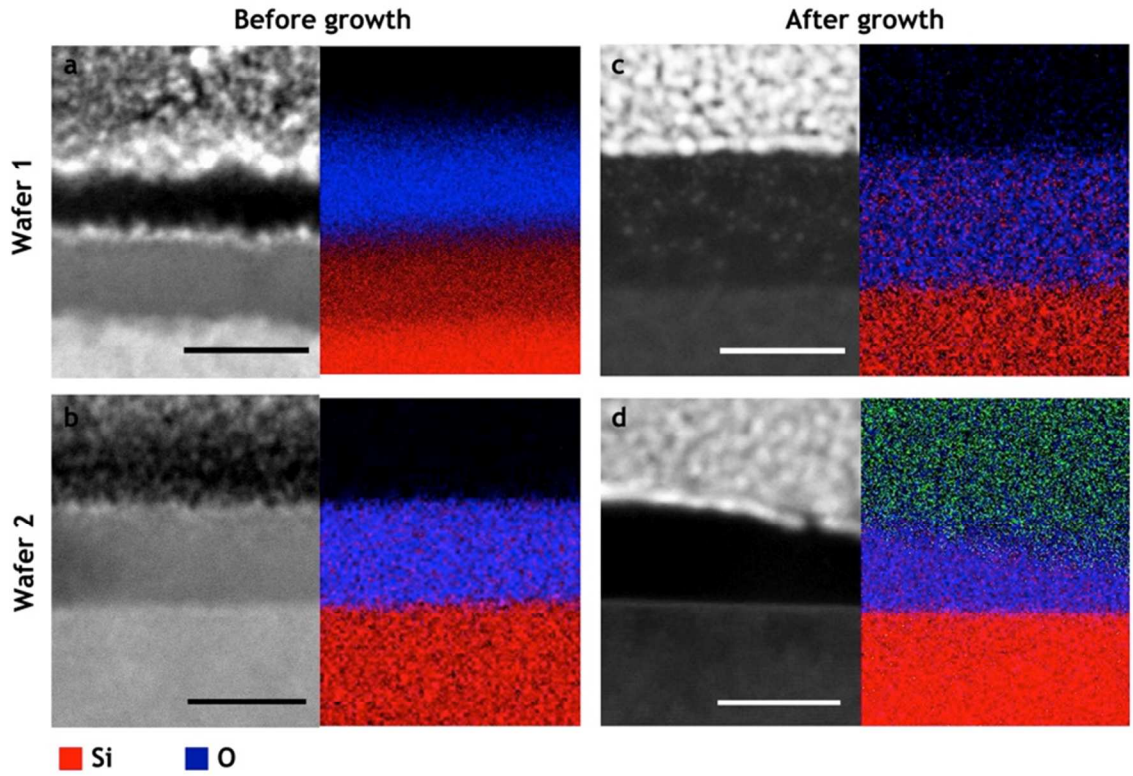

Figure 3. HAADF images of representative samples of Wafer 1 and Wafer 2, studied before and after growth, and corresponding EDX results, with the Si map in red and the O map in blue. The analysis is performed at the interface between the silicon substrate and the mask oxide. The sample from Wafer 1 shows an unexpected layer of a-Si that crystallizes after growth. The sample from Wafer 2 shows uniquely a thermal oxide layer grown directly on the crystalline silicon substrate. The scale bar is 20 nm.

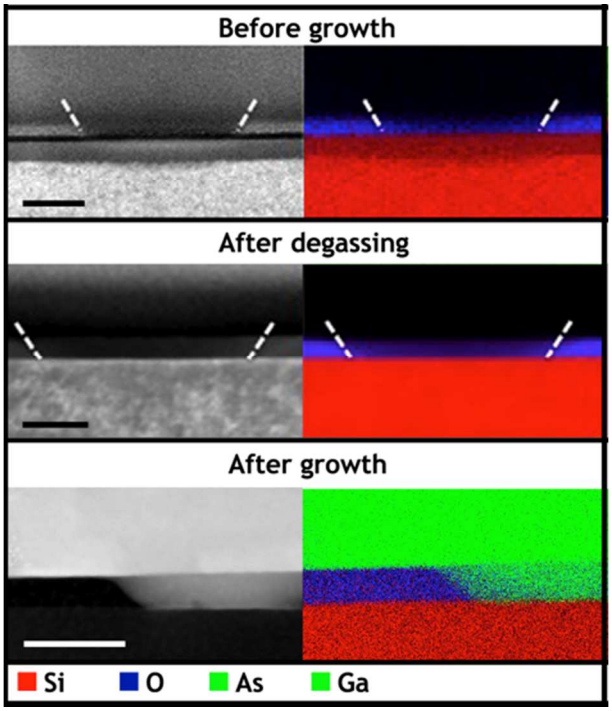

Figure 4. (Top) HAADF image of a nanoscale hole where the SiO_2, the amorphous Si and the crystalline Si can be distinguished and the corresponding EDX map. (Center) HAADF and EDX analysis of the hole degassed in the MBE reactor. The amorphous silicon layer is crystallized. (Bottom) HAADF and EDX analysis performed after the growth. A GaAs NW nucleates in the hole, grows vertically and also radially once higher than the hole. The scale bar is 50 nm.

We turn now the attention to a patterned region of the silicon chip: cross-sectional HAADF images of nanoscale holes from *Wafer 1* with the corresponding EDX maps are shown in Figure 4. The analysis has been performed prior to growth (Figure 4 top), after the degassing step in the MBE chamber (Figure 4 center) and after the growth (Figure 4 bottom). Here we also observe the presence of an amorphous silicon layer below the SiO_2 prior to degassing or growth. The amorphous layer, which is also observed at the position of the holes, is completely crystallized

after the degassing and growth steps. After crystallization, the silicon surface at the bottom of the hole appears completely flat, as shown in Figure 4 (bottom).

We thus conclude that the presence of a layer of amorphous silicon seems to be a necessary but not sufficient condition to guarantee a high yield of vertical wires, and that the addition of the Ga pre-deposition is also required. We remind here that in our case the Ga shutter is opened at the very beginning of the growth process and thus during the degassing step. During this time, the temperature of the Ga cell is ramping up to a achieve a nominal Ga growth rate of 1 Å/s, and the substrate temperature is ramped up from 200°C up to 770°C at a rate of 50°C/s for the degassing step. Therefore, the amorphous layer is expected to crystallize in a relatively short time once the substrate approaches the degassing temperature[36]. The Ga pre-deposition, however, already starts at lower substrate temperatures, when the amorphous layer has not yet crystallized. We believe that the Ga droplets are formed on the amorphous silicon at the bottom of the holes before it crystallizes. When the Ga pre-deposition is not performed during the heating of the substrate, or when the amorphous layer is not present, the Ga droplets form directly on the crystalline silicon of the substrate.

Crystalline and amorphous silicon possess different surface energies. As a consequence, wetting of Ga should also present a different nature. Knowing that the characteristics of the Ga droplets affect the yield of vertical NWs[37,38], we looked at their shape and contact angle on amorphous and crystalline silicon. A thin amorphous silicon layer was deposited by means of Plasma-Enhanced Chemical Vapour Deposition (PECVD) on a Si(111) wafer. The substrates were exposed to BHF wet etching to ensure their surfaces were free of oxide; both samples have been heated to 770°C for the degassing step with the increasing Ga deposition during the ramp up, simulating the initial step of our growth process.

SEM micrographs of the Ga droplets obtained on the two kinds of surfaces are shown in Figure 5. The Ga droplets deposited on what initially was amorphous silicon have a contact angle of 84±4°; the ones deposited on crystalline silicon have a contact angle of 52±3°. The Ga droplets deposited directly on crystalline silicon are also significantly larger than the ones observed on amorphous silicon. Both, the droplet size and contact angle, could favour vertical nanowire growth in the case of the originally amorphous silicon substrate. Contact angles smaller than 90° render nucleation at the triple-phase line especially difficult[39,40]. Additionally, we envisage in patterned substrates that when the sizes of the holes and the droplet are similar, the lateral walls affect the extension and position of the droplet. It also suppresses the existence of the triple-phase line at the interface with the silicon substrate. If the triple-phase line occurs on the SiO_2, the loss of epitaxial relation with the substrate results in random orientation of the nanowires. Although this study has been performed on unpatterned substrates, we believe that it highlights important aspects of the initial stages of growth and how to obtain high yields of vertical wires.

We conclude that the size and the contact angle of the Ga droplets as well as their interaction with the substrate play a fundamental role in the successful growth of vertical GaAs NW arrays. Our results suggest some possible modifications to the nanofabrication methods usually employed for nanoscale holes. In particular is should be advantageous to change the wetting properties at the open surface of the holes. Recent ~~unpublished~~ results show that there is an optimal contact angle for obtaining high yield of vertical wires, which can be obtained by a careful control of the native oxide[40]. Finally, if amorphous silicon should be used at the interface between the substrate and the SiO_2 mask, it is necessary to investigate the required layer thickness, as the amorphous silicon layer will party crystallize during the thermal oxidation

process. Alternatively, if the process should be compatible with thin amorphous silicon layers, the growth mask material should be reconsidered.

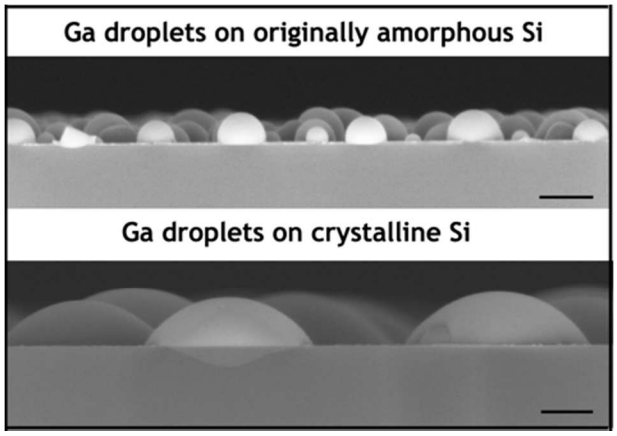

Figure 5. Cross sectional SEM images of Ga droplets deposited on originally amorphous silicon (top) and on crystalline silicon (bottom). The droplets have different sizes and contact angles depending on the surface. The scale bar is 200 nm.

In conclusion, we have provided new elements for the achievement of a high yield of vertical GaAs NWs on a patterned Si substrate. A Ga pre-deposition step prepares the Ga droplets for nanowire growth. The nature of the surface during this pre-deposition is key for the obtaining the contact angle and position of the triple-phase line. We have obtained ideal conditions by using an oxidized Si substrate containing an amorphous layer at the interface with the crystalline substrate. Other treatments such as the creation of an appropriate native oxide layer may lead to a similar effect.

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Author Contributions

ERA, GT, DR, HAP and FM contributed to the growth. ERA, JVP, GT and ADM fabricated the samples. JA, MdlM and SCB performed HAADF STEM and EDX analysis. ERA made the figures and the artwork. ERA and A.F.iM. wrote the manuscript in collaboration with all the authors. A.F.iM. supervised the project. All authors have given approval to the final version of the manuscript.

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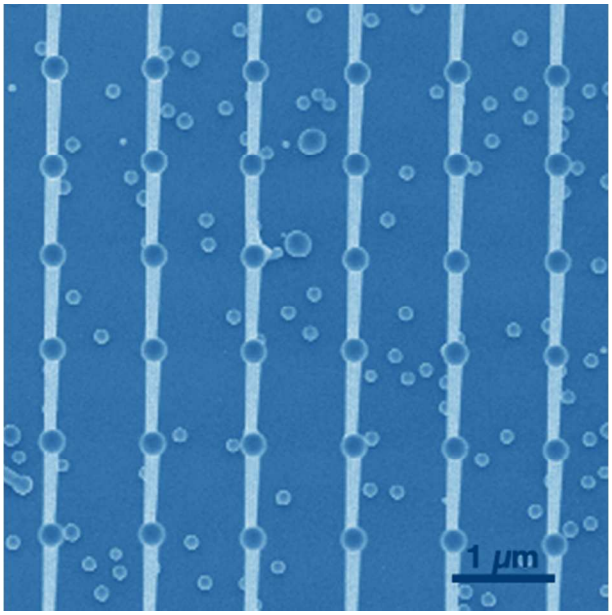

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