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3C-SiC Transistor With Ohmic Contacts Defined at Room Temperature

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***Abstract*— Among all SiC polytypes, only 3C-SiC has a cubic structure and can be hetero-epitaxial grown on large area Si substrate, thus providing an alternative choice for fabricating cheap wide bandgap power devices. Here, we present a low resistivity (~3 × $10^{-5}\Omega \cdot cm^2$) ohmic contact formed by directly depositing a Ti/Ni metal stack on n-type 3C-SiC without any extra annealing. For the first time, 3C-SiC lateral MOSFETs with as-deposited ohmic contacts were fabricated, and it turned out not only the ohmic contact is free from any interface voids, but also a higher field-effect mobility value (~80 $cm^2/V \cdot s$) was achieved compared with the annealed devices.**

***Index Terms*— 3C-SiC, channel mobility, MOSFET, ohmic contact, reliability.**

I. Introduction

WIDE band gap (WBG) semiconductors are considered as the materials for next generation electronics, particularly in the harsh environment and power electronics area. It is generally known that forming Ohmic contact to WBG semiconductors require not only a highly doped surface region, but also a relative high temperature (around 1000 °C) post-metallisation annealing (PMA) step. The PMA step generates an intermediate semiconductor layer (silicide or carbide) with narrower bandgap to reduce the Schottky barrier height (SBH) as well as creating more free carriers at the contact interface [1]. This additional step increases the fabrication thermal budget and complicates the WBG semiconductor applications in technologies which are sensitive to heat treatments, such as high-k, organic semiconductors, semiconductor heterojunctions etc. In this letter, we demonstrate how 3C-SiC MOSFETs fabrication can benefit from the as-deposited Ohmic contacts, with reliability and electrical performance both improved compared with a conventional PMA process.

The most studied metals for n-type 3C-SiC Ohmic contacts are Al [2]–[4], Ti [3]–[5] and Ni [2], [4], [6], [7], and the resultant ρ_c values covered a huge range from 10^{-7} to $10^{-1}\Omega$.cm^2. Room temperature Ti and Al contacts were reported on highly doped (3×10^{20} cm^{-3}) n-type 3C-SiC back in 1995 [3], although with a considerable resistivity spread of over $6\times10^{-5}\Omega$.cm^2. The literature shows that Al contacts generally have the lowest ρ_c value, which can be explained by the negligible SBH between Al and 3C-SiC (~0 eV) compared with Ti (0.4 eV) and Ni (0.55 eV) [4]. However, both Al and Ti easily get oxidised in air and Al has a melting point below 600 °C. On the other hand, Ni has a slow oxidation rate at room temperature and very high melting point. Although reacting with SiC above 500 °C, the silicide products help to reduce the interface SBH, leading to a lower ρ_c value. As a result, Ni has been the mostly used contact metal for n-type SiC and is applied for the study here.

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II. Device Fabrication

The material used in this work was a 10 μm thick unintentionally doped ($<1\times10^{16}$cm^{-3}) 3C-SiC film epitaxial grown on a 4-inch Si(100) substrate by NOVASiC. Nitrogen was implanted for creating high impurity concentration regions. A post-implantation annealing (PIA) at 1375 °C (Si melting point 1412 °C [8]) for 1 hour was carried out to activate the dopants, no surface capping layer was used. The samples were then all solvent cleaned, followed by a standard RCA cleaning procedure. Conventional transmission line method (TLM) structures with 1 μm mesa were patterned using photolithography and ICP etcher. 100 nm Ni was deposited as the contact metal in an e-beam evaporator at a low pressure of 2×10^{-7}Torr with a thin Ti interlayer (20 nm) to improve the contact adhesion. Lateral n-channel MOSFETs were fabricated using a double implantation scheme, P base (~1×10^{18} cm^{-3}, Al) for channel and N+ (~5×10^{20} cm^{-3}, N) for source/drain. The same PIA process used before was applied to activate both dopants. Prior to gate oxidation, the MOSFET samples went through an extra piranha clean (H_2SO_4:H_2O_2 =3:1). The gate oxide was thermally grown at 1300 °C (O_2 1 L/min), after that source/drain contacts were fabricated with as-deposited Ti/Ni contacts. For comparison purposes, devices with a PMA step (1 min at 1000 °C) were also fabricated. 500 nm Al was deposited on the channel region to form the gate contact. The final MOSFET has a channel length of 150 μm and width of 290 μm.

III. Results and Discussions

A. Non-Annealed Ohmic Contacts to 3C-SiC

Ohmic behaviour was obtained for the as-deposited Ti/Ni contacts on the 5×10^{20} cm^{-3} implanted 3C-SiC films.

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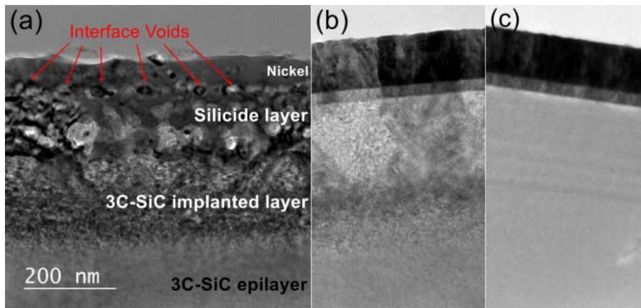

Fig. 1. TEM cross section views of the fabricated contact interfaces, (a) 5×10^{20} cm^{-3} after 1 min 1000 °C PMA, (b) 5×10^{20} cm^{-3} as-deposited, and (c) 5×10^{19} cm^{3} as-deposited.

The room temperature average ρ_c of $\sim3\times10^{-5}\Omega$.cm^2 is higher than the annealed one ($\sim9\times10^{-6}\Omega$.cm^2), but still low enough for power device fabrications. Here the average is taken from 4 TLM structures fabricated on each sample with little spread (as shown later in Fig. 2b) and performed using standard cleanroom deposition technology, which is an improvement from [3]. The voids (labelled in Fig. 1a) are silicon vacancies formed by severe silicon diffusion into nickel, known as Kirkendall effect [9]. Whereas they do not affect much the contact electrical performance [10], they were known to degrade the contact reliability [11]. From Fig. 1b and 1c, it can be seen that without the SiC-Ni reaction, the contact interface is much more abrupt and the interface voids are not present. Fig. 1b shows that the 5×10^{20}cm^{-3} implantation significantly damaged the 3C-SiC top layer. This would only occur in the Ohmic contact region and should not be a concern for most device fabrications, yet it is worth trying lowering the implantation dose and see if the Ohmic behaviour can be preserved. The same fabrication procedure (without PMA) was carried out on a 5×10^{19} cm^{-3} implanted sample, and again Ohmic behaviour was obtained, whereas $\rho_c$now increased to $\sim7\times10^{-4}\Omega$.cm^2. Further reducing the implantation level to $\sim1\times10^{19}$ cm^{-3} led to a rectifying contact, which became Ohmic after the PMA.

Metallic contacts were known to be formed when metal was deposited onto a semiconductor surface with high density dislocations, which can then shunt the space-charge layer and make field emission the dominant mechanism [12], [13] regardless of the semiconductor doping levels. Considering the 3C-SiC layer used in this study was grown on Si thus contains a large amount of defects, they may have helped towards a lower contact resistance. However, the 'metal shunts' requires the dissolution and recrystallization of semiconductor in metal, namely additional heat treatment [14]. We believe the as-deposited Ohmic contacts were obtained more likely by the formation of an impurity band caused by the excessive doping. In our previous study [15], the activation energy E_a of nitrogen for 1×10^{19}cm^{-3} implanted sample is approaching zero (15 meV). It is reasonable to assume that E_a becomes zero for 5×10^{19}cm^{-3} and 5×10^{20}cm^{-3} samples and they behave as degenerated semiconductors [16]. The increasing sheet resistance with temperature in Fig. 2a also favours this idea.

All the Ohmic contacts show very low temperature dependence from 25 °C up to 225 °C as shown in Fig. 2b.

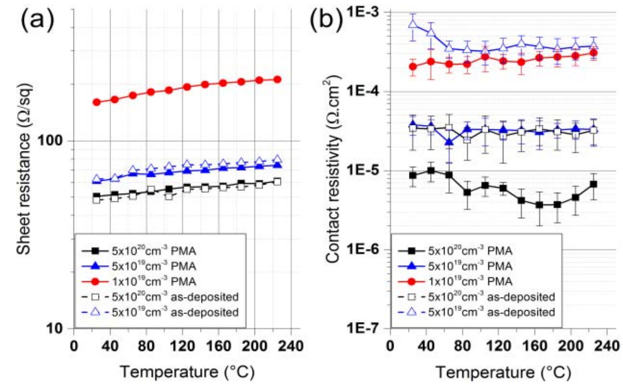

Fig. 2. Temperature dependence of (a) sheet resitance and (b) contact resistivity extracted from the TLMs.

As-deposited contacts on the 5×10^{20}cm^{-3} and 5×10^{19}cm^{-3} implanted samples readily behave as temperature independent, which means the PMA (similarly "metal shunts") did not play a big role in this. Also, the 1×10^{19}cm^{-3} doped sample has as-deposited rectifying behaviour, therefore not degenerated by the implantation process, whereas after PMA the ρ_c is also thermally stable, namely ruling out the degeneracy being the main cause. With the 3C-SiC electron effective mass of conductivity 0.32m_0 [17], dielectric constant 9.72 [18] known, the characteristic energy E_{00}/kT for the non-degenerated 1×10^{19} cm^{-3} doped 3C-SiC/metal interface is calculated [19] to be $\approx$ 1.3, which means the contact interface should be dominated by thermionic-field emission, and the ρ_c value should decrease considerably with increasing temperature. This is, however, conflicting with the Fig. 2b curves, which, if anything, appear more field-emission dominated. It was recently reported [20] that the metal/semiconductor interface band bending can be caused by dopant-induced dipole field between the interface and the dopant site. We then believe the thermal stable ρ_c is due to the Schottky barrier elimination caused by the interface band bending.

B. 3C-SiC MOSFETs Without Ohmic Contact Annealing

Apart from the improved contact interface which will lead to higher reliability, as-deposited Ohmic contacts may also benefit device fabrications where annealing can degrade other key features such as MOS and Schottky contacts [3]. To confirm this, lateral MOSFETs were fabricated as described in section II. All devices have typical forward features with well observed gate effects shown in Fig. 3a. Device without a PMA step clearly demonstrates higher forward current under all gate biases. Since the annealed contacts have lower resistance, the resultant higher total on-resistance of PMA processed devices must come from the channel.

The device transfer curve ($I_{ds}^{0.5}$ versus V_g) is shown in Fig. 3b and the leakage current observed in device off state ($Vg<-2$ V) should be caused by the stacking faults, which were identified as the main origin of leakage currents in 3C-SiC devices and can be greatly reduced by latest advanced growth techniques [21], [22]. The threshold voltages V_{th} extracted from Fig. 3b are ~-0.5V and ~2.5V for as-deposited and PMA processed devices, respectively.

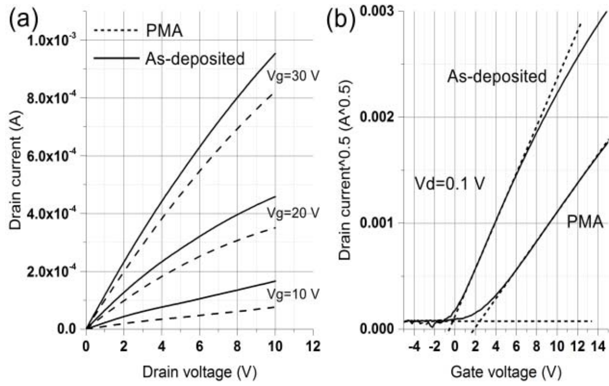

Fig. 3. (a) Forward conducting curves and (b) transfer curves ($I_{ds}^{0.5}$vs V_{gs}) for as-deposited and PMA processed MOSFET devices.

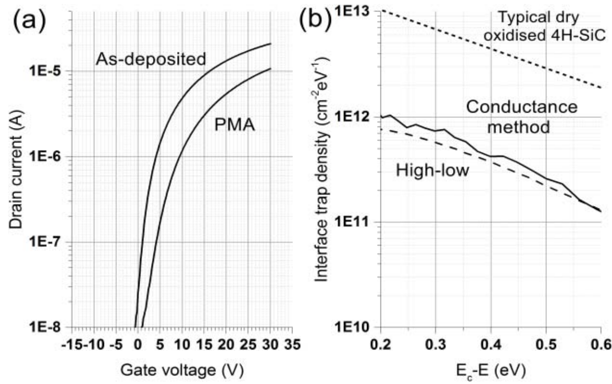

Fig. 4. (a) Subthreshould characteristics (Vd=0.1 V) of MOSFETs fabricated with as-deposited and PMA ohmic contacts and (b) D_{it} of capacitors fabricated on n-type 3C-SiC epilayer with same gate oxidaiotn as MOSFET.

The commonly observed [21], [23], [24] negative V_{th} of 3C-SiC MOS devices can be explained by the carbon-cluster interface traps model [25], which describes that due to the smaller band gap, only donor-like interface states (carbon clusters/dangling bonds) are present at the 3C-SiC/SiO_2 interface. Consequently, as-grown dry oxidized 3C-SiC MOS interface is positively charged and demonstrates a negative V_{th} [26], which can be shifted to positive if wet gate oxidation/post-oxidation annealing is applied [27] since wet oxidation is known to induce negative charges near the SiC/SiO_2 interface [28], [29]. Accordingly, the positive V_{th} shift of the PMA processed device observed in Fig. 3b should be caused by an additional build-up of negative charges at/near the MOS interface rather than a reduction of the donor-like interface states, since otherwise it would have improved the device conduction performance. These facts agree well with the devices subthreshold features shown in Fig. 4a. The subthreshold swing S estimated from drain current of 10^{-8} to 10^{-7} A are $\sim$1.7 V/dec and $\sim$3.3 V/dec for as-deposited and PMA processed devices, respectively. This is much higher than the ideal value ($\sim$0.06 V/dec for a MOSFET) and is caused by the unoptimised device parameters (i.e. oxide thickness $\sim$92 nm and channel doping $\sim 1\times10^{18}$ cm^{-3}), yet a comparison shows that an, almost 50% reduction of the subthreshold swing can be achieved by using as-deposited Ohmic contacts. The interface trap densities D_{it} can be estimated from S [30] with the

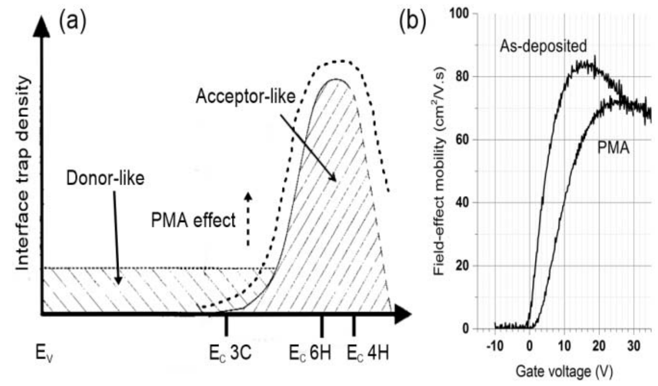

Fig. 5. (a) Schematic diagram of the inteface traps distribution for various SiC polytypes and (b) field-effect mobility of farbricated MOSFETs.

oxide thickness 92 nm known. For the weak inversion region, C_b was assumed to be zero, which caused the overestimation of D_{it}, and the values are determined as $\sim 6.6\times10^{12}$ cm^{-2}eV^{-1} for as-deposited devices and $\sim 1.3\times10^{13}$ cm^{-2}eV^{-1} for PMA devices. The 10^{13} order D_{it} values were previously reported for dry oxidised 3C-SiC MOS capacitors [26], [31]. Here lateral MOS capacitors were also fabricated following the same gate oxidation process as MOSFETs and D_{it} is found to be below 1×10^{12} cm^{-2}eV^{-1} close to the conduction band as seen in Fig. 4b, determined by both high-low and conductance methods. This is one magnitude lower than the values [32], [33] for 4H-SiC without further post oxidation annealing. The lower D_{it} value for devices with as-deposited Ohmic contacts confirms the PMA step leads to additional interface traps (schematic diagram shown in Fig. 5a) as previously reported for Si MOS devices, which was mostly explained by the mechanical stress induced at the MOS interface by the rapid temperature change and thermal expansion coefficients difference [34]–[36]. The channel field-effect mobility are calculated from the MOSFET trans-conductance and shown in Fig. 5b. Clearly the extra PMA step results in a lower peak channel mobility value ($\sim$70 cm^2/V.s) than the as-deposited case ($\sim$80 cm^2/V.s).

In power MOSFET designs, p-body and source are shorted by sharing the contact. Alloyed Ni is commonly used for both in 4H-SiC power devices [37], [38], similarity we believe the as-deposited Ti/Ni bilayer proposed here can also be integrated. The low thermal budget of the process demonstrated in this work opens new doors to the application of SiC transistors with other low temperature technologies, including high k dielectrics atomic layer deposited (e.g. Al_2O_3 or HfO_2) with relative low temperature of growth, ferroelectric polymers a classical example being polyvinylidene fluoride, organic semiconductors such as polythiophenes that can become conducting owing to their conjugated π-orbitals, fullerenes or carbon nanotubes, organic trihalide perovskites, and classic heterojunction or wafer bonded devices.

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