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Low-Temperature Growth of Axial Si/Ge Nanowire Heterostructures Enabled by Trisilane

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ABSTRACT: Axial Si/Ge heterostructure nanowires, despite their promise in applications ranging from electronics to thermal transport, remain notoriously difficult to synthesize. Here, we grow axial Si/Ge heterostructures at low temperature using a Au catalyst with a combination of trisilane and digermane. This approach yields, as determined with detailed electron microscopy characterization, arrays of epitaxial Si/Ge nanowires with excellent morphologies and purely axial composition profiles. Our data indicates that heterostructure formation can occur via either the vapor-liquid-solid (VLS) or vapor-solid-solid (VSS) mechanisms. These findings highlight the importance of precursor chemistry on semiconductor nanowire synthesis and open the door to Si/Ge nanowires with programmable quantum domains.

Control of composition at the nanoscale is central to the construction and operation of devices ranging from field effect transistors to solar cells.[1-2] It is also critical for advanced materials where the arrangement of nanoscale constituent elements gives rise to exotic properties.[3-5] The vapor-liquid-solid (VLS) mechanism, which permits the encoding of different materials and/or compositions along the length of semiconductor nanowires, provides one route to programmable compositional heterogeneity.[6-9] Group III-V nanowires, due to the low solubility of group V atoms in the catalyst droplet and the wide parameter space offered by the use of two precursors (i.e., for delivering group III and V atoms), currently offer the best control of axial heterostructure. Axially embedded quantum dots can be fabricated with heights ranging from one to several bilayers.[10-11]

Axial heterostructure formation remains challenging for group IV nanowires.[12] Yet, the promise of these heterostructures in applications such as transistors[13-15] for large-area integrated circuits and thermoelectrics[16-18], where low cost, low toxicity, and thermal stability are paramount, continues to motivate work in this area. To date, the large majority of axial Si/Ge heterostructure nanowire syntheses yield non-ideal structural motifs including diameter changes,[19-20] sidewall deposition,[9, 21] kinking,[8, 22-23] and/or crystallographic defects.[22] Si/Ge heterostructure nanowires without these unwanted structural motifs are possible, but with growth rates usually too rapid to encode highly confined structures.[24-25] In many cases, co-flow of a second precursor, such as HCl, is also necessary to improve sidewall morphology.[26-27] This approach, however, requires careful control of growth conditions to prevent surface roughening from halogen-induced surface atom removal (e.g., as SiX_2 or GeX_2 where X = Cl or Br).[28-30] A notable exception to the above challenges is vapor-solid-solid (VSS) growth with an alloyed catalyst (e.g., Au/Al, Au/Ag), which is able to produce sub-5 nm Ge domains along the length of Si nanowires.[31-32]

Here, we demonstrate arrays of axial Si/Ge heterostructure nanowires with excellent sidewall morphologies and purely axial composition profiles. We use the precursors trisilane (Si_3H_8) and digermane (Ge_2H_6) for Si and Ge segment growth, respectively, with a conventional Au catalyst. Trisilane is highly reactive, enabling Si homoepitaxy as low as 300 °C.[33] This precursor choice is motivated by the reduced H_2 desorption rate on both Si[34-35] and Ge[36-37] surfaces at these temperatures. The nanowire sidewalls are expected to remain largely hydrogen-passivated during Si/Ge heterostructure formation, and limit the catalyst perturbations that can lead to poor morphologies, kinking, and defects. This approach also offers growth rates slow enough for quantum dot and/or superlattice fabrication.

METHODS. All nanowires are synthesized in a custom-built ultra-high vacuum (UHV) chamber with a base pressure of 3×10^{-10} Torr (McAllister Technical Services). A description of the chamber and substrate preparation methods are included in prior studies.[38-39] Briefly, substrates are cut into rectangles (6 mm × 24 mm) from a double-side polished Ge(111) wafer (MTI Corp., CZ, 500 μm, 42-64 Ω-cm). Each substrate is repeatedly oxidized in 3 wt% H_2O_2 (JT Baker, 30 wt%, ACS grade), etched with 9 wt% HCl (JT Baker, CMOS grade), cleaned with dionized water, and dried with N_2 gas. The substrate is then immersed in a 1:2:20 NH_4OH (Sigma-Aldrich, 28-30 wt%, ACS grade):H_2O_2:H_2O solution, rinsed with dionized water, and dried with N2 gas. Upon insertion into the UHV chamber, the substrate is heated to 485 °C to desorb the chemical oxide from the wet chemical treatment, followed by epitaxial Ge film deposition at 305 °C with a Ge_2H_6 (Air

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Liquide, 20% in He) partial pressure of 2×10^{-5} Torr. Finally, a thin layer of Au (< 0.5 nm) is deposited onto the substrate at room temperature via thermal evaporation (SVT Associates). The substrate temperature is monitored throughout the nanowire growth by a calibrated infrared pyrometer (Mikron) focused on the backside of the substrate.

Nanowire growth begins with the same procedure utilized in a recent study.[37] Briefly, Ge_2H_6 at a partial pressure of 1×10^{-4} Torr is introduced to the chamber with the substrate at room temperature. The substrate is then heated to 485 °C at a rate of 10 °C/s, held for 30 s, and cooled to 305 °C at a rate of 3 °C/s. A short Ge nanowire "stub" results from growth at these conditions for 5 min. While maintaining the Ge_2H_6 partial pressure, the substrate temperature is lowered to 290 °C and the remainder of the Ge segment is grown over the course of 30 min. Si segment growth is initiated by flowing Si_3H_8 followed by termination of Ge_2H_6 flow. The Si segment is elongated at either 290, 310, or 330 °C with a Si_3H_8 (Air Liquide, 99.99%) partial pressure of 1×10^{-4} Torr for 30 min. For Ge/Si/Ge heterostructures growth, Ge_2H_6 is re-introduced at a partial pressure of 1×10^{-4} Torr prior to termination of Si_3H_8 flow. All segments of Ge/Si/Ge nanowires are synthesized at 290 °C. Growth is terminated by rapidly reducing substrate temperature, after which all precursors are evacuated from the chamber.

Nanowire structure is analyzed with a Hitachi SU-8230 scanning electron microscopy (SEM) and a FEI Tecnai F20 transmission electron microscope (TEM). For TEM measurements, nanowires are transferred to carbon-coated grids (Ted Pella) by a direct mechanical transfer method.[40] High resolution TEM (HRTEM) images are obtained with a 0.19 nm point-to-point resolution at 200 keV. For the compositional maps and profiles, we combine scanning TEM (STEM) with electron energy loss spectroscopy (EELS) in the same FEI Tecnai F20. An embedded Gatan image filter is used for EELS analyses. EELS can provide atomic-level spatial resolution for sufficiently thin samples.[41] For nanowires with diameters similar to those studied here, typical signal broadening at heterointerfaces is less than 2 nm. Heterointerfacial strain is analyzed by the geometric phase analysis (GPA) method.[42] The GPA algorithm performs an analysis based on the amplitude and phase of the lattice fringes as a function of position in the HRTEM images at different Bragg reflection angles. A cosine type mask with the radius previously optimized is employed around the (1 -1 -1) growth plane for all nanowires.

RESULTS & DISCUSSION. Figures 1a and 1b show representative SEM images of Si/Ge nanowire arrays where the Si segment is grown at 290 and 330 °C, respectively. Si segment growth at 310 °C yields a similar morphology (Supporting Information, Figure S1). Nanowire morphology and cross-array uniformity is excellent (> 98% verticality) for all temperatures (Supporting Information, Figure S2). Nanowires exhibit an epitaxial orientation relative to the Ge(111) substrate, indicating their growth is in the <111> direction. As anticipated for a Si/Ge heterostructure, the images in the Figure 1a and 1b insets show a bright segment (Ge) below a dark (Si) segment. The heterostructure forms properly in almost every nanowire. The growth rate of the initial Ge segment is ~10.6 nm/min, as expected for growth at 290 °C.[39] The Si segment growth rate is far lower at ~0.45, 0.96, and 1.64 nm/min for 290, 310, and 330 °C, respectively.

Detailed structural analysis confirms the single-crystallinity and growth direction of the Si/Ge heterostructure nanowires. Figure 2a shows a representative bright field TEM image of the near-catalyst region of a Si/Ge heterostructure nanowire with Si segment growth at 290 °C. Lattice fringes are clearly visible, demonstrating that the nanowire remains single-crystalline across the Si/Ge heterointerface. Figures 2b,c and 2d,e show high resolution TEM (HRTEM) images along the [1-12] zone axis and associated Fast Fourier Transform (FFT) for the nominally Si (blue box) and Ge (red box) segments, respectively. Both segments grow along the <111> direction.
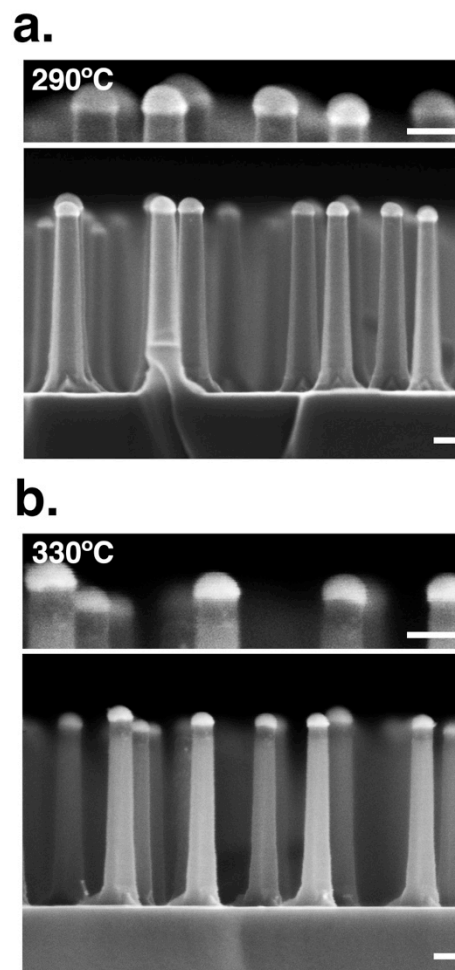

Figure 1. Representative cross-sectional SEM images of Si/Ge heterostructure nanowires where the Si segment is grown at (a) 290 °C and (b) 330 °C for 30 minutes. Scale bars, 50 nm.

Electron energy loss spectroscopy (EELS) measurements confirm the chemical identity of the Si and Ge segments. Figure 3a shows a representative high angle annular dark field STEM (HAADF-STEM) image of a nanowire containing Si/Ge nanowires with the Si segment grown at 290 °C. A contrast change near the catalyst is observed similar to that seen in Figure 1. As would be expected for hydrogen-passivated sidewalls,[43] gold is only observed in the catalyst region. EELS maps of Si (blue) and Ge (red) are also shown in Figure 3a and definitively confirm the presence of Si and Ge segments. The top of each map is the liquid-solid interface.

The Si/Ge heterointerface is compositionally graded along the axial direction, as seen in Figure 3b, for all temperatures

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studied here. A transition width of approximately 20 and 35 nm is observed for Si segment growth at 290 and 330 °C, respectively, and is considerably less than the nanowire diameter.[24-25] We discuss the observed compositional grading in more detail below. In addition, the absence of Si on the sidewall of the Ge -segment (Supporting Information, Figure S3) confirms that the heterostructure exhibits a purely axial composition profile. This observation provides additional support that the sidewall is well passivated.
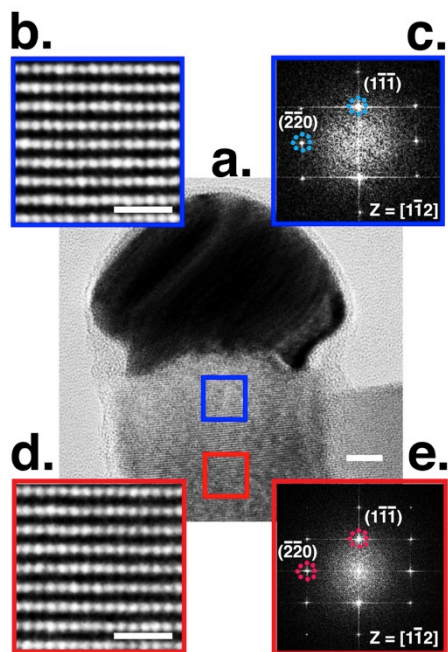

Figure 2. HRTEM of the Si/Ge heterointerface. (a) HRTEM image of a nanowire with the Si and Ge segments grown at 290 °C. Scale bar, 5 nm. (b) High resolution TEM image of the Si segment. Scale bar, 1 nm. (c) FFT of the image in (b) showing growth along the <111> direction. (d) High resolution TEM image of the Ge segment. Scale bar, 1 nm. (e) FFT of the image in (d) showing growth along the <111> direction.

We quantify heterointerfacial strain, as shown in Figure 4, by combining HRTEM with geometric phase analysis (GPA). A transition region (green) between the Ge (red) and Si (blue) regions is clearly observed in the GPA maps. This transition is consistent with the axial compositional grading seen in the EELS data (Figure 3) and is analogous to recent reports for axial III-V heterostructures.[44-45] The lattice mismatch is calculated to be -3.7% and -3.9% for Si segment growth at 290 and 330 °C, respectively, which is close to that expected for an ideally relaxed bulk Si/Ge heterointerface (approximately - 4.0%). We attribute the larger deviation from ideality for Si segment growth at 290 °C (-3.7 vs. -4.0%) to the length of the Si segment, which is shorter and thus remains more strained than the Si segment grown at 330 °C (-3.9 vs. -4.0%).
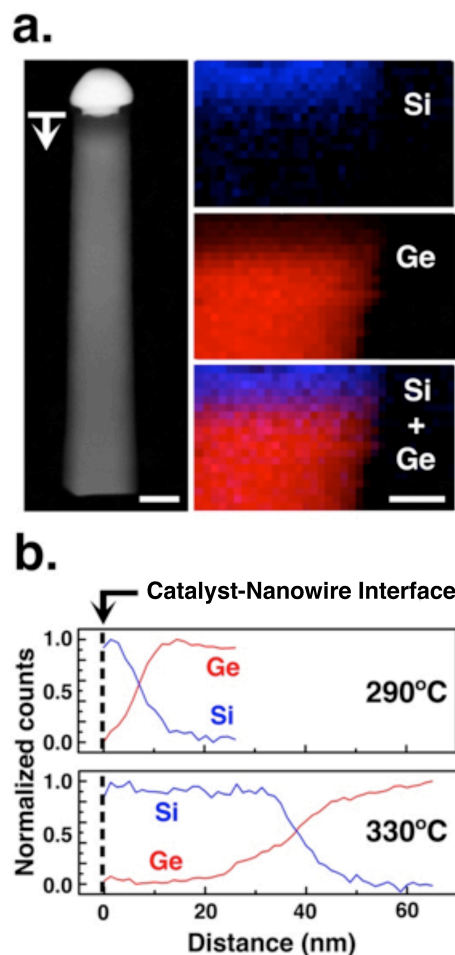

Figure 3. Compositional analysis of the Si/Ge heterointerface. (a) Representative HAADF STEM image of a Si/Ge heterostructure nanowire grown entirely at 290 °C. Scale bar, 30 nm. White line denotes the liquid-solid interface. EELS maps of Si, Ge, and composite Si + Ge are also shown. Scale bar, 10 nm. (b) Axial EELS composition profiles starting at the catalyst-nanowire interface and crossing the Si/Ge heterointerface for nanowires with the Si segment grown at 290 and 330 °C.

Nanowires containing Ge/Si/Ge heterostructures are also synthesized as shown in Figure 5. All segments are grown at 290 °C for 30 min. A HAADF STEM image and the corresponding EELS composition map is displayed Figure 5a. A distinct Si segment is visible between two Ge segments, which confirms that Si crystallization is occurring under growth conditions. The HRTEM image in Figure 5b shows that the nanowire remains single-crystalline across both heterostructures. The EELS composition profile in Figure 5c, similar to Figure 3b, shows how the initially grown Si/Ge heterointerface exhibits a graded composition. Interestingly, the subsequently grown heterointerface is more abrupt.

Our data show that the use of a Si_3H_8 and Ge_2H_6 chemistry solves many, but not all, of the challenges of conventional hydrides for Si/Ge heterostructure formation. Foremost, the near-unity fraction of nanowires containing Si/Ge heterostructures without kinks or defects (Figures 1, S1, S2), as well as the absence of radial composition grading (Figure S3), supports the presence of a robust, likely hydrogen, sidewall passivation. Additional studies are required to definitively
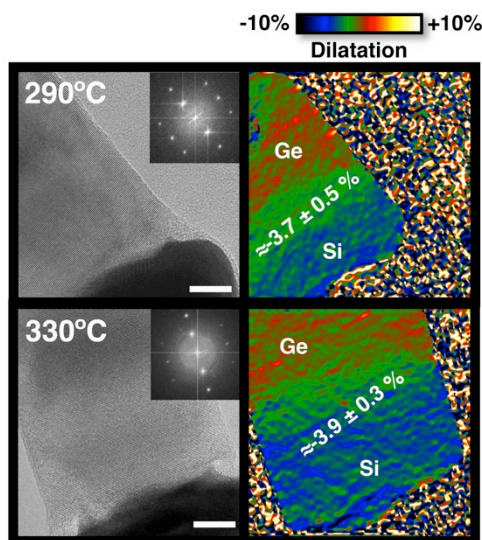
Figure 4. Strain analysis of the Si/Ge heterointerface. HAADF STEM images of representative Si/Ge heterostructure nanowires with the Si segment grown at 290 °C (left, top) and 330 °C (left, bottom). Scale bars, 10 nm. Dilatation maps after applying GPA to the (1 -1 -1) Si and Ge growth planes for Si segment growth at 290 °C (right, top) and 330 °C (right, bottom). The GPA color scale ranges from -10 to +10 % lattice expansion.

identify the catalyst's phase during Ge to Si and Si to Ge transitions, but the present data provides important clues. The slow growth rate of the second Ge segment, especially relative to the first Ge segment (i.e., ~0.5 vs. ~10 nm/min), indicates that the catalyst solidified during or prior to the Si to Ge transition.[49] The low solubility of semiconductor atoms in solid catalysts also results in more abrupt heterointerfaces,[32] as seen here for the Si to Ge transition. The larger composition grading observed for the Ge to Si transition, however, suggests that the catalyst was still liquid at that point during growth. Graded composition profiles are commonly observed for axial heterointerfaces synthesized with the VLS mechanism and attributed to the so-called "reservoir effect".[46-47] While not as widely studied as Ge nanowire growth via the VLS growth mechanism below the bulk eutectic temperature,[39, 48-49] Si nanowires have also been reported to grow via this mode.[50] The presence of a liquid catalyst droplet for Si nanowire growth below the bulk eutectic temperature is supported by prior studies of Ge nanowire growth by us[43] and others.[49] In particular, we recently showed that hydrogen-passivated sidewalls maintain Au/Ge catalysts in a metastable liquid state below the bulk eutectic temperature.[43] A similar situation is likely present for low temperature Si segment growth with Si_3H_8. Adsorbed hydrogen atoms prevent catalyst atoms from accessing the sidewall and, in doing so, prevent the Au/Si catalyst from solidifying. The same mechanism can explain why the catalyst appears to solidify upon reintroducing Ge_2H_6. The presence of Ge atoms in the trijunction region increases the hydrogen atom desorption rate (as H_2) enough to permit atomic transport to the sidewall and identification of a low barrier site for nucleation (i.e., catalyst solidification).
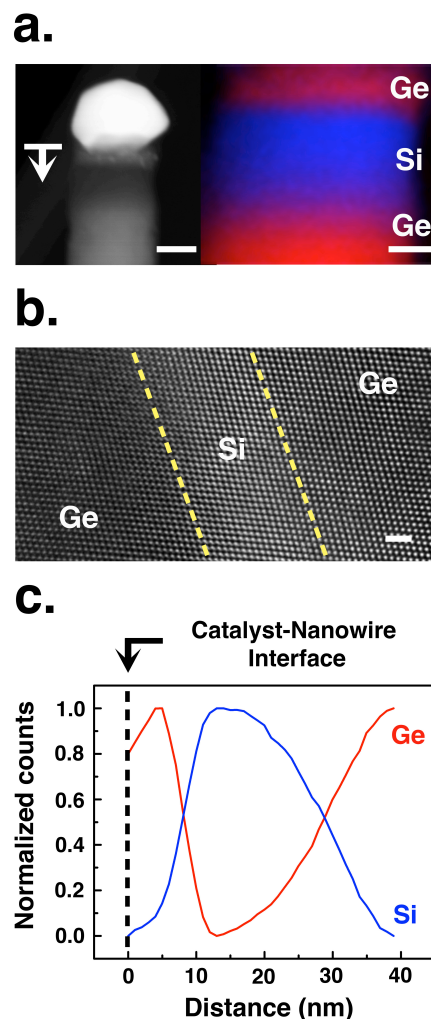

Figure 5. Compositional analysis of the Ge/Si/Ge heterointerface. (a) Representative HAADF STEM image of a Ge/Si/Ge heterostructure nanowire grown entirely at 290 °C. Scale bar, 20 nm. White line denotes the liquid-solid interface. A composite EELS map of Si (blue) and Ge (red) is also shown. Scale bar, 10 nm. (b) HRTEM image of the Ge-Si-Ge region along the [1-12] zone axis. Scale bar, 1.5 nm. (c) Axial EELS composition profiles starting at the catalyst-nanowire interface and crossing both Si/Ge heterointerfaces.

Identification of a root cause for the temperature-dependent transition width seen in Figure 3 is still under investigation, but is likely of kinetic origin. Since the solubility of semiconductor atoms in the catalyst droplet changes only a few percent over the temperature range studied here, thermodynamics cannot fully explain the ~50% change in transition width over 40 °C.[49] Recent work has shown that a backward reaction pathway can transfer atoms from the liquid catalyst to the gas phase,[51-52] an effect that is particularly pronounced in crystallization-limited situations. The smaller transition width observed here at lower temperature (Figure 3) is consistent with this pathway. When crystallization is limiting, as is likely under the low temperature conditions studied here, catalyst composition will be dominated by atomic delivery/removal at the catalyst-vapor interface. In this situation, as observed here, conditions that increase the stability of gas phase product species (e.g., GeH_x), including a reduced temperature, would fa-

vor atomic removal from the catalyst and result in a more abrupt heterointerface.

CONCLUSION. We demonstrate the low temperature growth of axial Si/Ge heterostructures with a combination of Si_3H_8 and Ge_2H_6. Our approach prevents the catalyst perturbations that result in poor morphologies, kinks, and defects. A robust sidewall passivation is likely responsible for these observations, but additional work is required to demonstrate this directly. Our experiments show that precursor design is a powerful method to control bottom-up nanowire growth, and enable nanostructures that were previous challenging or off-limits.

ASSOCIATED CONTENT

Supporting Information

Additional figures of cross-sectional SEM images of nanowire arrays and radial EELS composition profiles, as referenced in the main text. The Supporting Information is available free of charge on the ACS Publications website.

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Author Contributions

HYH grew the nanowires and collected the SEM data. HYH and MAF jointly analyzed the data and wrote the manuscript. JA and MdlM collected and analyzed the TEM data. All authors approved the final version.

Notes
The authors declare no competing financial interest.

ABBREVIATIONS

VLS, vapor-liquid-solid; VSS, vapor-solid-solid; Si_3H_8, trisilane; Ge_2H_6, digermane; UHV, ultra-high vacuum; SEM, scanning electron microscopy; TEM, transmission electron microscope; HRTEM, High resolution TEM; STEM, scanning TEM; FFT, Fast Fourier Transform; HAADF STEM, high angle annular dark field STEM; GPA, geometric phase analysis; EELS, Electron energy loss spectroscopy.

REFERENCES

(1) Cui, Y.; Zhong, Z.; Wang, D.; Wang, W. U.; Lieber, C. M. High performance silicon nanowire field effect transistors. *Nano Lett.* **2003,** *3*, 149-152.

(2) Garnett, E.; Yang, P. Light trapping in silicon nanowire solar cells. *Nano Lett.* **2010,** *10*, 1082-1087.

(3) Carnevale, S. D.; Yang, J.; Phillips, P. J.; Mills, M. J.; Myers, R. C. Three-dimensional GaN/AlN nanowire heterostructures by separating nucleation and growth processes. *Nano Lett.* **2011,** *11*, 866-871.

(4) Gudiksen, M. S.; Lauhon, L. J.; Wang, J.; Smith, D. C.; Lieber, C. M. Growth of nanowire superlattice structures for nanoscale photonics and electronics. *Nature* **2002,** *415*, 617-620.

(5) Ye, X.; Chen, J.; Diroll, B. T.; Murray, C. B. Tunable plasmonic coupling in self-assembled binary nanocrystal superlattices studied by correlated optical microspectrophotometry and electron microscopy. *Nano Lett.* **2013,** *13*, 1291-1297.

(6) Hyun, J. K.; Zhang, S. X.; Lauhon, L. J. Nanowire heterostructures. *Annu. Rev. Mater. Res.* **2013,** *43*, 451-479.

(7) Johansson, J.; Dick, K. A. Recent advances in semiconductor nanowire heterostructures. *CrystEngComm* **2011,** *13*, 7175-7184.

(8) Ben-Ishai, M.; Patolsky, F. From crystalline germanium-silicon axial heterostructures to silicon nanowire-nanotubes. *Nano Lett.* **2012,** *12*, 1121-1128.

(9) Mouchet, C.; Latu-Romain, L.; Cayron, C.; Rouviere, E.; Celle, C.; Simonato, J. P. Growth of one-dimensional Si/SiGe heterostructures by thermal CVD. *Nanotechnology* **2008,** *19*, 335603.

(10) Priante, G.; Patriarche, G.; Oehler, F.; Glas, F.; Harmand, J. C. Abrupt GaP/GaAs interfaces in self-catalyzed nanowires. *Nano Lett.* **2015,** *15*, 6036-6041.

(11) Vainorius, N.; Lehmann, S.; Jacobsson, D.; Samuelson, L.; Dick, K. A.; Pistol, M. E. Confinement in thickness-controlled GaAs polytype nanodots. *Nano Lett.* **2015,** *15*, 2652-2656.

(12) Amato, M.; Palummo, M.; Rurali, R.; Ossicini, S. Silicon-germanium nanowires: chemistry and physics in play, from basic principles to advanced applications. *Chem. Rev.* **2014,** *114*, 1371-1412.

(13) Huang, Y.; Duan, X.; Cui, Y.; Lauhon, L. J.; Kim, K. H.; Lieber, C. M. Logic gates and computation from assembled nanowire building blocks. *Science* **2001,** *294*, 1313-1317.

(14) Le, S. T.; Jannaty, P.; Luo, X.; Zaslavsky, A.; Perea, D. E.; Dayeh, S. A.; Picraux, S. T. Axial SiGe heteronanowire tunneling field-effect transistors. *Nano Lett.* **2012,** *12*, 5850-5855.

(15) Björk, M. T.; Ohlsson, B. J.; Thelander, C.; Persson, A. I.; Deppert, K.; Wallenberg, L. R.; Samuelson, L. Nanowire resonant tunneling diodes. *Appl. Phys. Lett.* **2002,** *81*, 4458-4460.

(16) Amato, M.; Palummo, M.; Ossicini, S.; Rurali, R. SiGe nanowires for thermoelectrics applications. In Nanoscale Thermoelectrics, Lecture Notes *in Nanoscale Science and*

Technology, Wang, X.; Wang, Z. M., Eds. Springer International Publishing: Switzerland, 2014; Vol. 16, pp 497-515.

(17) Li, D.; Wu, Y.; Fan, R.; Yang, P.; Majumdar, A. Thermal conductivity of Si/SiGe superlattice nanowires. *Appl. Phys. Lett.* **2003,** *83*, 3186-3188.

(18) Hu, M.; Poulikakos, D. Si/Ge superlattice nanowires with ultralow thermal conductivity. *Nano Lett.* **2012,** *12*, 5487-5494.

(19) Geaney, H.; Mullane, E.; Ramasse, Q. M.; Ryan, K. M. Atomically abrupt silicon-germanium axial heterostructure nanowires synthesized in a solvent vapor growth system. *Nano Lett.* **2013,** *13*, 1675-1680.

(20) Li, C. B.; Usami, K.; Mizuta, H.; Oda, S. Growth of Ge–Si nanowire heterostructures via chemical vapor deposition. *Thin Solid Films* **2011,** *519*, 4174-4176.

(21) Eisenhawer, B.; Sivakov, V.; Berger, A.; Christiansen, S. Growth of axial SiGe heterostructures in nanowires using pulsed laser deposition. *Nanotechnology* **2011,** *22* (30), 305604.

(22) Dayeh, S. A.; Wang, J.; Li, N.; Huang, J. Y.; Gin, A. V.; Picraux, S. T. Growth, defect formation, and morphology control of germanium-silicon semiconductor nanowire heterostructures. *Nano Lett.* **2011,** *11*, 4200-4206.

(23) Flynn, G.; Ramasse, Q. M.; Ryan, K. M. Solvent vapor growth of axial heterostructure nanowires with multiple alternating segments of silicon and germanium. *Nano Lett.* **2016,** *16*, 374-380.

(24) Clark, T. E.; Nimmatoori, P.; Lew, K. K.; Pan, L.; Redwing, J. M.; Dickey, E. C. Diameter dependent growth rate and interfacial abruptness in vapor-liquid-solid Si/Si$_{1-x}$Ge$_x$ heterostructure nanowires. *Nano Lett.* **2008,** *8*, 1246-1252.

(25) Wu, Y.; Fan, R.; Yang, P. Block-by-Block Growth of single-crystalline Si/SiGe superlattice nanowires. *Nano Lett.* **2002,** *2*, 83-86.

(26) Chang, H. Y.; Tsybeskov, L.; Sharma, S.; Kamins, T. I.; Wu, X.; Lockwood, D. J. Photoluminescence and Raman scattering in axial Si/Ge nanowire heterojunctions. *Appl. Phys. Lett.* **2009,** *95*, 133120.

(27) Wang, X.; Tsybeskov, L.; Kamins, T. I.; Wu, X.; Lockwood, D. J. Structural and optical properties of axial silicon-germanium nanowire heterojunctions. *J. Appl. Phys.* **2015,** *118*, 234301.

(28) D'Evelyn, M. P.; Yang, Y. L.; Cohen, S. M. Adsorption, desorption, and decomposition of HCl and HBr on Ge(100): Competitive pairing and near-first-order desorption kinetics. *J. Chem. Phys.* **1994,** *101*, 2463-2475.

(29) Jackman, R. B.; Ebert, H.; Foord, J. S. Reaction mechanisms for the photon-enhanced etching of Semiconductors - an investigation of the UV-stimulated interaction of chlorine with Si(100). *Surf. Sci.* **1986,** *176*, 183-192.

(30) Jackman, R. B.; Price, R. J.; Foord, J. S. Semiconductor surface etching by halogens - Fundamental steps. *Appl. Surf. Sci.* **1989,** *36*, 296-312.

(31) Chou, Y. C.; Wen, C. Y.; Reuter, M. C.; Su, D.; Stach, E. A.; Ross, F. M. Controlling the growth of Si/Ge nanowires and heterojunctions using silver-gold alloy catalysts. *ACS nano* **2012,** *6*, 6407-6415.

(32) Wen, C. Y.; Reuter, M. C.; Bruley, J.; Tersoff, J.; Kodambaka, S.; Stach, E. A.; Ross, F. M. Formation of composi-

tionally abrupt axial heterojunctions in silicon-germanium nanowires. *Science* **2009,** *326*, 1247-1250.

(33) Kumata, K.; Itoh, U.; Toyoshima, Y.; Tanaka, N.; Anzai, H.; Matsuda, A. Photochemical vapor deposition of hydrogenated amorphous silicon films from disilane and trisilane using a low pressure mercury lamp. *Appl. Phys. Lett.* **1986,** *48*, 1380-1382.

(34) Kim, H.; Spila, T.; Greene, J. E. Si(113) hydrogen desorption kinetics: a temperature programmed desorption study. *Surf. Sci.* **2001,** *490*, L602-L608.

(35) Oura, K.; Lifshits, V. G.; Saranin, A. A.; Zotov, A. V.; Katayama, M. Hydrogen interaction with clean and modified silicon surfaces. *Surf. Sci. Rep.* **1999,** *35*, 1-69.

(36) Kim, H.; Vailionis, A.; Cahill, D. G.; Greene, J. E. Ge(011)-c(8×10) surface structure and hydrogen desorption pathways: a temperature-programmed desorption and scanning tunneling microscopy study. *Surf. Sci.* **2000,** *457*, 337-344.

(37) Lee, J. Y.; Maeng, J. Y.; Kim, A.; Cho, Y. E.; Kim, S. Kinetics of H$_2$ (D$_2$) desorption from a Ge(100)-2×1:H (D) surface studied using scanning tunneling microscopy and temperature programmed desorption. *J. Chem. Phys.* **2003,** *118*, 1929-1936.

(38) Shin, N.; Filler, M. A. Controlling silicon nanowire growth direction via surface chemistry. *Nano Lett.* **2012,** *12*, 2865-2870.

(39) Sivaram, S. V.; Shin, N.; Chou, L. W.; Filler, M. A. Direct observation of transient surface species during Ge nanowire growth and their influence on growth stability. *J. Am. Chem. Soc.* **2015,** *137*, 9861-9869.

(40) Fontcuberta i Morral, A.; Arbiol, J.; Prades, J. D.; Cirera, A.; Morante, J. R. Synthesis of silicon nanowires with wurtzite crystalline structure by using standard chemical vapor deposition. *Adv. Mater.* **2007,** *19*, 1347-1351.

(41) Arbiol, J.; Estrade, S.; Prades, J. D.; Cirera, A.; Furtmayr, F.; Stark, C.; Laufer, A.; Stutzmann, M.; Eickhoff, M.; Gass, M. H.; Bleloch, A. L.; Peiro, F.; Morante, J. R. Triple-twin domains in Mg doped GaN wurtzite nanowires: structural and electronic properties of this zinc-blende-like stacking. *Nanotechnology* **2009,** *20*, 145704.

(42) Hÿtch, M. J.; Snoeck, E.; Kilaas, R. Quantitative measurement of displacement and strain fields from HREM micrographs. *Ultramicroscopy* **1998,** *74*, 131-146.

(43) Sivaram, S. V.; Hui, H. Y.; de la Mata, M.; Arbiol, J.; Filler, M. A. Surface hydrogen enables subeutectic vapor-liquid-solid semiconductor nanowire growth. *Nano Lett.* **2016,** *16*, 6717-6723.

(44) de la Mata, M.; Leturcq, R.; Plissard, S. R.; Rolland, C.; Magen, C.; Arbiol, J.; Caroff, P. Twin-Induced InSb nanosails: A convenient high mobility quantum system. *Nano Lett.* **2016,** *16*, 825-833.

(45) de la Mata, M.; Magen, C.; Caroff, P.; Arbiol, J. Atomic scale strain relaxation in axial semiconductor III-V nanowire heterostructures. *Nano Lett.* **2014,** *14*, 6614-6620.

(46) Dick, K. A.; Bolinsson, J.; Borg, B. M.; Johansson, J. Controlling the abruptness of axial heterojunctions in III-V nanowires: beyond the reservoir effect. *Nano Lett.* **2012,** *12*, 3200-3206.

(47) Li, N.; Tan, T. Y.; Gösele, U. Transition region width of nanowire hetero- and pn-junctions grown using vapor–liquid–solid processes. *Appl. Phys. A* **2008,** *90*, 591-596.

(48) Dayeh, S. A.; Picraux, S. T. Direct observation of nanoscale size effects in Ge semiconductor nanowire growth. *Nano Lett.* **2010,** *10*, 4032-4039.

(49) Kodambaka, S.; Tersoff, J.; Reuter, M. C.; Ross, F. M. Germanium nanowire growth below the eutectic temperature. *Science* **2007,** *316*, 729-732.

(50) Westwater, J.; Gosain, D. P.; Tomiya, S.; Usui, S.; Ruda, H. Growth of silicon nanowires via gold/silane vapor-liquid-solid reaction. *J. Vac. Sci. Technol. B* **1997,** *15*, 554-557.

(51) Hui, H. Y.; Filler, M. A. Solid-liquid-vapor etching of semiconductor nanowires. *Nano Lett.* **2015,** *15*, 6939-6945.

(52) Pinion, C. W.; Nenon, D. P.; Christesen, J. D.; Cahoon, J. F. Identifying crystallization- and incorporation-limited regimes during vapor-liquid-solid growth of Si nanowires. *ACS Nano* **2014,** *8*, 6081-6088.

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