High-Temperature Electrical and Thermal Aging Performance and Application Considerations for SiC Power DMOSFETs

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***Abstract*—The temperature dependence and stability of three different commercially-available unpackaged SiC DMOSFETs have been measured. On-state resistances increased to 6 or 7 times their room temperature values at 350 °C. Threshold voltages almost doubled after tens of minutes of positive gate voltage stressing at 300 °C, but approached their original values again after only one or two minutes of negative gate bias stressing. Fortunately, the change in drain current due to these threshold instabilities was almost negligible. However, the threshold approaches zero volts at high temperatures after a high temperature negative gate bias stress. The zero gate bias leakage is low until the threshold voltage reduces to approximately 150 mV, where-after the leakage increases exponentially. Thermal aging tests demonstrated a sudden change from linear to nonlinear output characteristics after 24–100 h air storage at 300 °C and after 570–1000 h in N2 atmosphere. We attribute this to nickel oxide growth on the drain contact metallization which forms a heterojunction p-n diode with the SiC substrate. It was determined that these state-of-the-art SiC MOSFET devices may be operated in real applications at temperatures far exceeding their rated operating temperatures.**

***IndexTerms*—Aging,insulatedgatebipolartransistors(IGBTs), oxygen, power MOSFETs, temperature measurement.**

I. INTRODUCTION

SILICON carbide power MOSFET devices have now been commercially-available for more than six years. Full SiC power modules incorporating SiC Schottky barrier diodes and SiC MOSFETs were also made available shortly after. Other types of SiC power devices such as bipolar junction transistor and JFET have also been commercialized but, in general, have seen less commercial success and, in some cases, discontinued. One of the perceived main advantages of the SiC devices is their potential to operate at much higher temperatures than silicon power devices such as IGBTs. In fact, SiC devices are intrinsically capable of operating at very high temperatures and are actually manufactured using very high melting temperature materials. Their performance and reliability of commerciallyavailable devices under such conditions is, therefore, of interest but there have been relatively few independent studies done on this to date. In this paper, the first two generations of SiC MOSFET devices have been evaluated to obtain their electrical and thermo-mechanical performances at temperatures up to 350 °C. The target application for this is a high-performance hybrid electric vehicle inverter whose junction temperature is allowed to increase up toa peak of approximately 300 °Cfor occasionalshortdistances,suchthatthespaceandweight consuming cooling system does not have to be scaled up to meet this occasional demand. Although 350 °C is approximately 200 °C above the rated operating temperatures of current SiC MOSFET devices, initial static measurements showed good performance up to 350 °C, beyond which device failures were noted.

The materials used in the manufacture of these devices are well known, and known to be capable of being operated well above the rated device temperatures—the only question is how long. To illustrate this point, an SiC PiN diode made from a similar material set has already demonstrated very good electrical performance up to 900 °C, at least for the duration of the measurements [1]. The purpose of this present work was to evaluate the readiness of the commercially-available devices for hightemperature applications and, in particular, to determine how they degrade and how long they last.

Neudeck *et al*. have reviewed the possible roles for SiC devicesandconcludedthattheywouldbeunlikelytofindmuchuse until they are able to operate at ambient temperatures exceeding 300°Candthatthelimitationforlong-termhigh-temperaturereliability is the metal–semiconductor ohmic contact [2]. Thermal cycling above such temperatures would also make the long-term hermeticsealingofthepackaging achallenge; therefore, thereal test for these devices is the long-term operation in air. For these reasons, and because there are no long-term reliable die on substrate encapsulation materials available for such high temperatures, high temperature aging tests have also been carried out on bare die in air in this work, as well as in an inert atmosphere. The impact of the oxygen penetration on the rate of degradation of the electrical characteristics of these SiC MOSFETs has been obtained so that the remaining lifetime of the devices can be incorporated into a whole system lifetime model.

The reliability of the ohmic contacts at high temperatures has received a great deal of attention, both in air and inert atmospheres. For example, the degradation mechanisms of contacts of semiconductors in general, including at high

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temperatures, were summarized to be due to diffusion and subsequent formation of solid solutions or compounds [3]. The interdiffusion can increase the contact resistance by orders of magnitude, and compound formation can induce coefficient of thermal expansion mismatch, brittleness, and open circuits. The degradation mechanisms of ohmic contacts for SiC at high temperatures were shown by [4], and can be summarized as voiding due to dissimilar diffusion rates of adjacent metal layers. In the case of operation in air or oxygen containing environments, various metal stack and ceramic oxygen diffusion barriers have been demonstrated on top of the ohmic contacts to have high performance at extremely high temperatures from 450 °C to 750 °C [5]–[10]. It is not known whether such features have been incorporated into commercially-available devices, as such detail is generally retained as commercial secrets by the device manufacturers.

A number of other authors have already demonstrated the performance of SiC devices at high temperatures. SiC JFETs capable of operating for thousands of hours at 500 °C have been demonstrated [11]. Commercially-available versions of so-called SiC junction transistors have also been shown to operate well up to 500 °C [12] and have demonstrated current gains higher than 60 at 350 °C, roughly half of their room temperature gain [13]. For SiC DMOSFETs, the temperature dependence of drain–source current, mobility, channel resistance, and threshold voltage (V_T) up to 300 °C was comprehensively demonstrated by [14]. The threshold voltage was shown to have a negative temperature dependence. The high-temperature performance of SiC JFETs and DMOSFETs up to 300 °C has also been partially studied by [15], where it was shown that transconductance of SiC DMOSFETs increases with temperature while the threshold voltage decreases with temperature. This has the effect of reducing the channel resistance and counteracting the positive temperature dependence of the drift region resistance to keep the overall on-state resistance ($R_{DS,ON}$) relatively temperature insensitive. Their results demonstrated a two-fold increase in $R_{ON,SP}$ from room temperature to 300 °C. It was also suggested that the SiC JFET is more suitable for high-temperature operation due to its lower drain–source leakage at high temperatures, and because there is no channel resistance.

One of the perceived main negative issues of SiC DMOSFET devices is the threshold voltage drift under positive and negative gate bias temperature stress conditions (simultaneous high gate bias and high temperature for long time periods). This was anticipated to have been solved in second-generation devices. However, this has already been shown not to be the case for temperatures above their rated maximum operating temperatures [16], [17]. It was shown that the V_T shift is still significant for plastic packaged devices when operated at 225 °C, especially for an extreme constant negative gate voltage of –20 V, which is significantly below the normal –5 V limit of today's commercially-available devices. It was suggested that the negative bias causes a greater shift because holes are more susceptible to oxide trapping than electrons. This trapping is known to be an extremely fast process, as has been demonstrated by [18]. The temperature dependence of interface trapping and temperature on V_T has also been illustrated mathematically and used to demonstrate its sensitivity to the P-well doping concentration for practical values of V_T around +2 V [19]. Most importantly, the possibility of the device becoming normally on at high temperatures was also discerned. Kaplar *et al*. have demonstrated the positive benefit of using a constant negative gate bias at up to 250 °C, by showing that it decreases the drain–source leakage current significantly [17], but only at the expense of increased negative threshold voltage drift. The impact of switched gate bias temperature stressing (BTS), as opposed to constant gate bias, was also demonstrated by Kaplar *et al*. to emulate the real application conditions. An initial and significant V_T drift of between –150 and –350 mV was demonstrated after the first 30 min of operation (with no intermediate measurements), followed by a slow drift of approximately 1–2 mV/h. Tanimoto and Ohashi, one of the only other authors to study the effects of physical degradation of SiC MOSFET devices, demonstrated electrical failure of the devices due to gate dielectric erosion and disconnection of the ohmic contacts after 32 h at 500 °C [20].

In almost all of the previous works highlighted, the authors demonstrated the performance of a single and mostly proprietary device under a limited set of conditions and, in some cases, had a direct affiliation with the device manufacturer. In this paper, two different widely available SiC DMOSFET devices from the current second generation and one device from the first generation, for comparison, are evaluated independently for their high-temperature performance and thermo-mechanical reliability. These new results complement the existing results and are presented in a way that demonstrates the state of the art, rather than to identify which manufacturer has the best product. These results will also serve as a benchmark for a future evaluation of the third-generation devices that are now just becoming available.

II. Experimental Procedure

More than 100 SiC DMOSFET die of three types from different manufacturers have been used for these tests. Approximately 20 of each type have undergone electrical testing, mainly to determine the temperature dependence up to 350 °C of the most important device parameters including their output characteristics, threshold voltage drift, drain current leakage, and reverse breakdown voltages. Approximately 15 of each type have undergone thermal aging in air or inert atmospheres and some have been subjected to temperature cycling tests. The three MOSFET types were all rated at 1.2 kV, approximately 30 A continuous drain current at room temperature and with a surface area in the order of 10–15 mm^2.

A. High-Temperature Electrical Measurements

A heated probe station was designed and manufactured to evaluate the electrical performance of the devices, as shown in Fig. 1. The devices, in bare die form, were tested individually by placing the drain terminal side down in the polished stainless steel container. This container was lowered onto the hotplate for testing, with voltage isolation to the heater provided by a thin aluminum nitride disk. The gate and source terminals were probed by specially designed high temperature capable tungsten

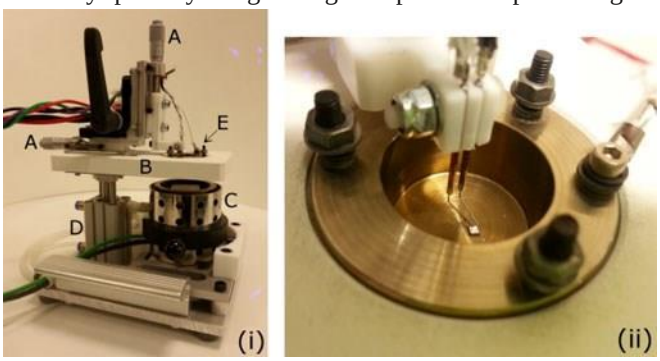

Fig. 1. (i) High temperature probe station developed for this work including probe positioners (A), ceramic sample holder (B), hotplate (C), sample lift (D), and sample holder (E). (ii) Magnified view of die sample holder with bespoke high-temperature probes.

rhenium S-bend probes that had good elasticity to facilitate the application of pressure to the die topside aluminum metallization. For high temperature reverse breakdown tests, a dielectric fluid capable of being heated to 300 °C for periods of a few minutes was poured into the container. The electrical measurements were conducted using a Tektronix 371B curve tracer and the measured characteristics were saved as images and spreadsheet files. Calibration exercises were first carried out to determine the safe electrical limits for single-shot and sweep measurements using the curve tracer, to avoid device damage and significant self-heating up to the maximum temperature. In general, this meant limiting the maximum drain current to around 5 A. A new die was used for every high-temperature test, to eliminate the possibility of additional measurements being influenced by thestressescausedbypreviushigh-temperaturemeasurements.
More than 50 die were tested for their high-temperature electrical performance in total. Differential on-state resistance measurementsweretakenfromtheslopeoftheoutputcharacteristic s as measured by the curve tracer. Gate threshold voltage measurements were conducted on the curve tracer by connecting the gate and drain terminals ($V_{DS} = V_{GS}$), setting the gate–drain voltage limit and then performing a single-shot pulsed measurement. The threshold voltage was read from the resulting plot of $V_{DS} = V_{GS}$ versus current at 20 μA. This current was chosen to be well above the threshold voltage knee, and low enough to prevent a positive threshold voltage shift *during* the measurement, and during additional measurements. The curve tracer was connected to the heated die probe station for all of these measurements. Gate BTS was performed by connecting the heated probe station to a laboratory power supply with the drain and source terminals connected together. The zero volt and drain–source connections were exchanged to apply the negative gate bias stress.

B. High-Temperature Storage Tests

Approximately 50 new die have also been used for these aging tests. Aging in air was carried out by placing the die on a laboratory ceramic hotplate, drain side down, for a fixed period of time up to 100 h storage time. For the aging in inert atmosphere, the die were placed on a thin aluminum oxide sheet

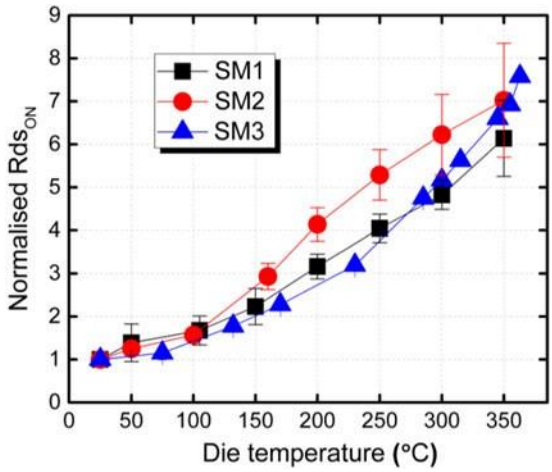

Fig. 2. Normalized temperature dependence of on-state resistance $R_{ds,ON}$ measured for two different SiC MOSFET power device types at V_{gs} = 20 V. The error bars indicate the spread of measured values for different die.

in a tube furnace with an N_2 gas flow rate of approximately 1.4slmfor1000hstorageintotal.Inallcases,thesetsofdevices were periodically removed, cooled quickly in air by placing them on a large block of polished aluminum, and then were electrically tested using the curve tracer. Typically, the output characteristics and threshold voltage were recorded in this case, before returning them to the high-temperature environment to continue the aging tests.

III. Results

A. On-State Resistance Measurements

In order to facilitate the calculation of conduction losses and scale the cooling system performance up to the high temperatures of interest in this work, the drain to source on-state resistance $R_{DS,ON}$ of the devices has been measured up to 350 °C. This temperature was chosen as the limit for testing because the failure rate appeared to increase quickly above this temperature. The results of the $R_{DS,ON}$ measurements are shown in Fig. 2, normalized to their room temperature starting values, which were all between approximately 80 and 100 mΩ. These values are close to the manufacturer data sheet values up to their 150 °C ratings, increasing to approximately two times their room temperature values, but increasing more rapidly with temperature thereafter. This is expected to be because the ratio

of channel to drift resistance has been optimized to be close to the maximum rated operating temperature of the devices, which are all 150 °C, and above which the channel resistance is decreasing slightly slower than the drift resistance is increasing. It can be seen that, for the SiC MOSFETs under test, $R_{DS,ON}$ has increased to 6 or 7 ± 1 times their room temperature values at 350 °C. The error bars also show the large spread of values for different die of the same type.

B. High Temperature Instability of Threshold Voltage

During electrical testing at the high temperatures, instability of the gate threshold voltage (V_T) was noted for some of the devices; V_T was increasing *while* carrying out the higher temperature electrical measurements. Fig. 3 illustrates this variation for a small number of slow heating and cooling cycles of the probe station hot plate while carrying out pulsed *I–V* measurements using the curve tracer. These results clearly illustrate significant instability for one device type, and good stability for the other from a different manufacturer for this single-shot pulsed measurement scenario. The resulting V_T instability shown for the SM1 device type is due to the combination of temperature dependence and drift due to the curve tracer pulsed gate bias temperature stress. For the SM2 device, the temperature dependence is similar, but the V_T instability is negligible. Gate bias switching tests have been carried out by a previous author who suggested that constant gate bias conditions, used by other researchers and in this work, are not realistic and under realistic switching conditions the V_T drift will be negligible [21]. However, the results shown in Fig. 3 and those of other authors [16], [17] prove that the drift *can* be affected by switched operation, especially above the device's rated temperatures, but it will always be a strong function of the switching frequency and duty ratio. A previous study on older SiC MOSFET devices used a ramped gate bias turn-on and demonstrated V_T instability even at room temperature, and which increased when the gate voltage was ramped up more quickly [22]. However, the constant bias conditions give a good measure of device V_T stability and have, therefore, been used for the remainder of the present work.

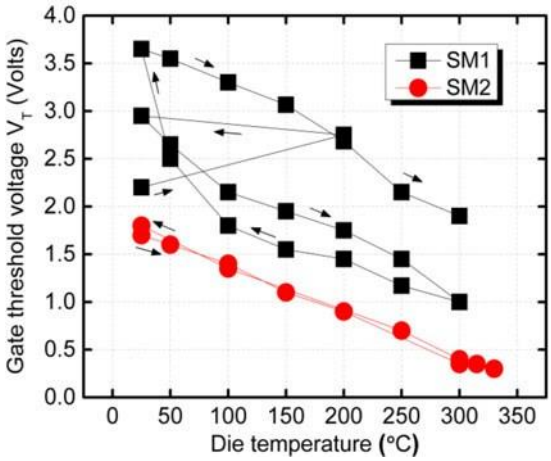

Fig. 3. Measured threshold voltage V_T versus die (top) surface temperature for two different SiC MOSFET types and for a small number of hotplate heating and cooling cycles. The arrows indicate the order of single-shot pulsed measurements during temperature cycling.

1) Instability Due to Bias Temperature Stressing: Gate BTS was carried out to quantify the extent of the observed threshold voltage drifts at 300 °C by applying +20 V gate bias voltage for 30 min followed by –5 V gate bias for 30 min. These values are the maximum gate–source voltages for the devices under test. The measured results shown plotted in Fig. 4 show a near twofold threshold voltage increase for the positive gate bias pBTS tests for two of the three SiC MOSFET types. These two SiC MOSFET devices, labeled SM1 and SM3, are first- and secondgeneration devices from the same manufacturer, which indicates that no significant improvement in the threshold voltage instability has been achieved by that manufacturer.

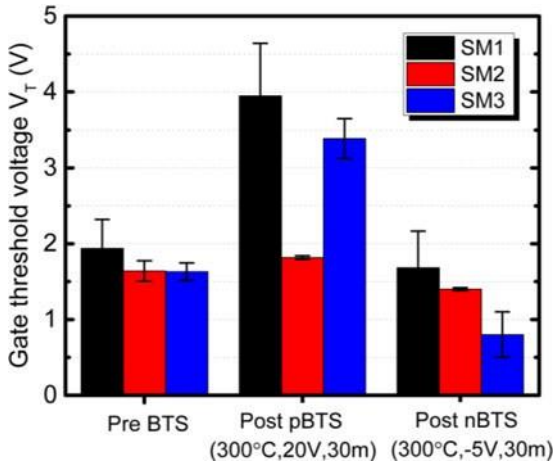

Fig. 4. SiC MOSFET threshold voltage V_T measured for the three different device types before and after BTS testing for 30 min at 300 °C, and for +20 and –5 V gate biases. All V_T measurements were taken at room temperature and for a drain current of 20 μA.

The results also indicate that, within the same time period, this increase, or V_T drift, can be completely corrected by the negative gate bias nBTS stress. Interestingly, the V_T drift due to pBTS was almost negligible for the SM2 device type, which is a second-generation device from a different manufacturer. This suggests that the SM2 devices have a much lower density of near interface traps (NITs) and/or oxide traps than the other two devices, most probably due to its specific SiO_2 growth conditions. In general, a relatively low spread of measured values was found for all device types for the initial room temperature V_T measurements and a larger spread was found for the devices following the high-temperature BTS tests. This indicates a strong material variation in the thermally generated density of NITs or oxide traps from die to die.

2) Temperature Dependence: The temperature dependence of threshold voltage for the three device types is also shown in Fig. 5, for the worst case situation where the

threshold voltages have been permanently reduced by the high temperature negative gate bias nBTS tests. The shift will be permanent unless a positivebiasorafurtherperiodofnegativebiasisappliedlaterat anelevatedtemperature.Itcanbeseenfromtheseresultsthatthe threshold voltages all have a negative temperature dependence, which approaches zero volts at relatively low temperatures for two device types but not until almost 350 °C for the SM2-type device. This is partly due to the fact that the SM2 device has a lower V_T temperature dependence of approximately 4mV/° C than the other two device types whose temperature dependence is approximately 8mV/° C, and partly because the SM2 devices have less drift at constant negative bias and, therefore, had the highest room temperature V_T values at the start of these tests. These V_T temperature dependencies were found to be identical for any other V_T starting values.

3) TimeDependence:

Thetimeandtemperaturedependence of V_T drift due to both maximum positive gate bias and minimum negative gate bias has also been obtained for one device type, as shown in Fig. 6. In this case, the temperature and maximum positive gate bias were applied and V_T was measured for different periods up to a total of 2 h, after which the maximum negative gate bias of –5 V was applied. All measurements were taken after cooling down to room temperature, and every measurement point is taken from a separate new device that has not been previously stressed (this removes the possibility of new measurements being influenced by previous measurements). The results clearly demonstrate the time dependence of the V_T drift which increases relatively slowly before rolling off to a maximum for the constant positive gate bias temperature stress. However, the V_T drift decreases extremely rapidly for the negative gate bias temperature stress, with V_T returning to its starting value or lower in one or two minutes. This negative bias V_T drift is also referred to by some authors as *negative bias temperature instability* (NBTI). At low temperatures, the V_T drift is low, almost negligible. However, as the temperature is increased the threshold shifts higher, but the time dependence of the V_T drift appears to be relatively independent of temperature for both the positive and negative gate bias. This situation is illustrated better in Fig. 7 where the maximum V_T drift and time to reach 90% of the maximum are plotted against temperature. It can be seen from this that the maximum drift increases significantly as the device is heated, but slows down sharply and rolls off at 250 °C. These results also demonstrate that it takes longer to reach 90% of the maximum V_T drift value as the temperature of the device is increased, and has a near linear temperature dependence. This temperature dependence is approximately 280ms K^{-1}, or, can be stated as a heating rate (β) of approximately 15K s^{-1}. It is worth noting that these test conditions are the worst case situations for these devices, using the maximum rated positive and negative gate voltages. Although it would be desirable to use the maximum possible positive gate voltage to extract maximum current from each device, it might be possible for some lower noise applications to use a value for the negative gate bias closer to zero volts. The benefits in terms of NBTI, which of course would result in a

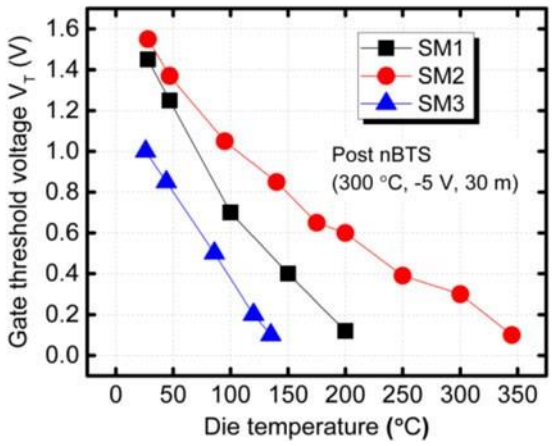

Fig. 5. Post nBTS temperature dependence of threshold voltage V_T following the 30 min –5 V nBTS test period at 300 °C. These results illustrate the situation that could occur if V_T drifts too far in a negative direction; the devices may enter a normally-on state.

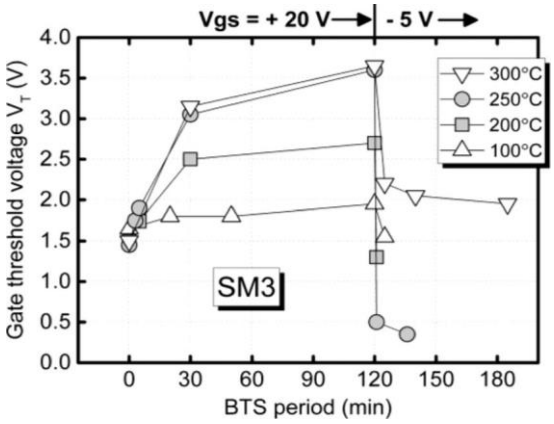

Fig. 6. Time dependence of threshold voltage V_T drift under constant bias BTS test conditions for SM3-type devices. A positive gate bias was applied for up to 2 h followed by negative bias for up to 45 min. Measurements were taken after cooling to room temperature.

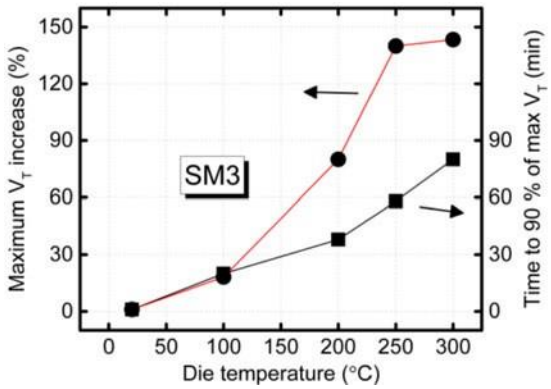

Fig. 7. Temperature dependence of *maximum* threshold voltage V_T drift and time to reach 90% of this maximum under constant bias BTS test conditions for the SM3-type devices.

lower V_T drift, have recently been demonstrated by another author for a proprietary SiC DMOSFET where the drift was demonstrated to be approximately four times less for a –1 V gate bias than for a –5 V bias over a 1000 s period [23].

4) Impact on Drain Current: It is important to know how much the stresses that cause these threshold voltage drifts effect the drain current (I_d) up to high temperatures so that the devices can be derated sufficiently in the real application. The output characteristics have been measured for the three device types before and after the 30 min BTS stress tests at 300 °C, and up to approximately 6 A. As can be seen from the representative resultsshowninFig.8,thechange incurrentisalmostnegligible for this current range, despite the quite high threshold voltage shifts reported in Fig. 4. The measured V_T values for the results shown pre-BTS, after pBTS, and after nBTS tests, respectively, for these specific die were SM1: 1.75, 4.1, 1.1; SM2: 1.5, 1.85, 1.4; SM3: 1.6, 2.25, 0.95 V. However, this negligible change in drain current after BTS tests was found for all die tested.

5) Drain–Source Leakage Current: The drain-to-source leakage current and its temperature dependence are shown in Fig. 9 for all three device types along with the associated threshold voltage measurements for each measurement temperature. It

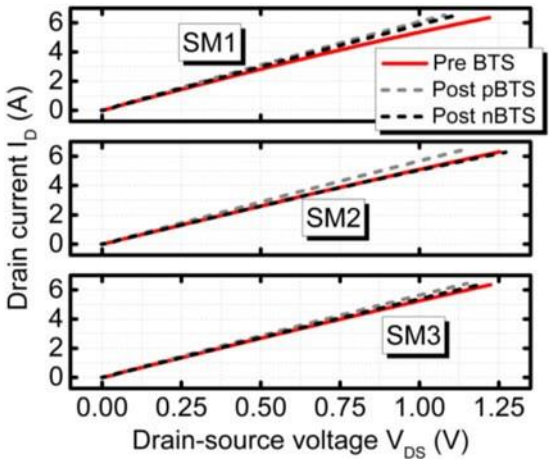

Fig. 8. Representative measured output characteristics for the three different SiC MOSFET types before and after the +20 V pBTS and –5 V nBTS constant gate bias stress tests at 300 °C for 30 min. Measurements were taken at room temperature and V_{gs} = +20 V.

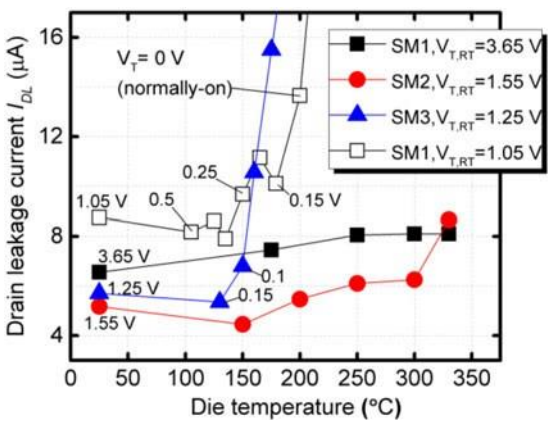

Fig. 9. Measured drain–source leakage currents versus die temperature for three different SiC MOSFET types, measured at V_{ds} = 10 V, V_{gs} = 0 V. The associated room temperature threshold voltage values ($V_{T,RT}$) are also shown. The leakage levels are heavily dependent on $V_{T,RT}$ and increase exponentially when V_T 150 mV approximately.

can be seen from these measurements that the leakage current is very low, in the order of 4–8 μA, for the entire measured temperature range of almost 350 °C in some cases. It is clear from these results that there is a very strong dependence of leakage current on the room temperature value of the threshold voltage V_T. For example, an SM1-type device with high V_T value of 3.65 V displays low leakage up to almost 350 °C. However, an SM1 device type with an extremely low V_T of 1.05 V shows an exponential increase at temperatures higher than approximately 125 °C. This is happening because V_T is already low and approaches zero volts at a relatively modest temperature due to its strong negative temperature dependence. The same situation exists for the SM3 device type results. It appears from these results that the leakage begins to increase exponentially if V_T is reduced to below approximately 150 mV within the operating temperature range. In general, these results demonstrate that this occurs for devices with high drift such as the SM1 and SM3 devices, even when their room temperature V_T values are relatively high, or devices with low V_T drift such as the SM2 devices even with their low room temperature V_T values.

C. Output Characteristics Before and After Aging

Aging experiments were carried out by placing a number of dieinhigh-temperaturestorageat300 °CinbothairandinertN$_2$ atmospheres. The air storage experiments were carried out by heating the die, placed drain side down, on a ceramic hotplate. The temperature of the hotplate cycled slowly up and down by no more than ±5 °C, presumably as a result of its thermostatic control. The inert atmosphere storage tests were carried out using a laboratory tube furnace. The precise temperature and temperature variation inside the tube furnace are unknown, but are expected to be small enough to neglect.

1) Air Atmosphere Aging: The air atmosphere aging simulates the situation where the device packaging hermetic seal has failed and oxygen has begun to infiltrate and, presumably, degrade the semiconductor device die [2]. Fig. 10(a)–(e) shows the measured output characteristics for the three device types before and after aging in air at 300 °C. It can be seen from (a) that the SM1-type device characteristic was severely degraded after 40 h and in (b) that the SM2 device characteristic was degraded after 70 h (but not 40 h). In both these cases, the output characteristics have become nonlinear for low values of V_{DS}, but are generally still quite linear above the knee position of the new characteristic for higher V_{DS} values. In fact, for the SM1 device, it appears as if the slopes have simply shifted to the right after the high-temperature aging in air. Closer scrutiny, however, indicates a 64% increase in $R_{DS,ON}$ from approximately 82 mΩ before aging to 134 mΩ after aging

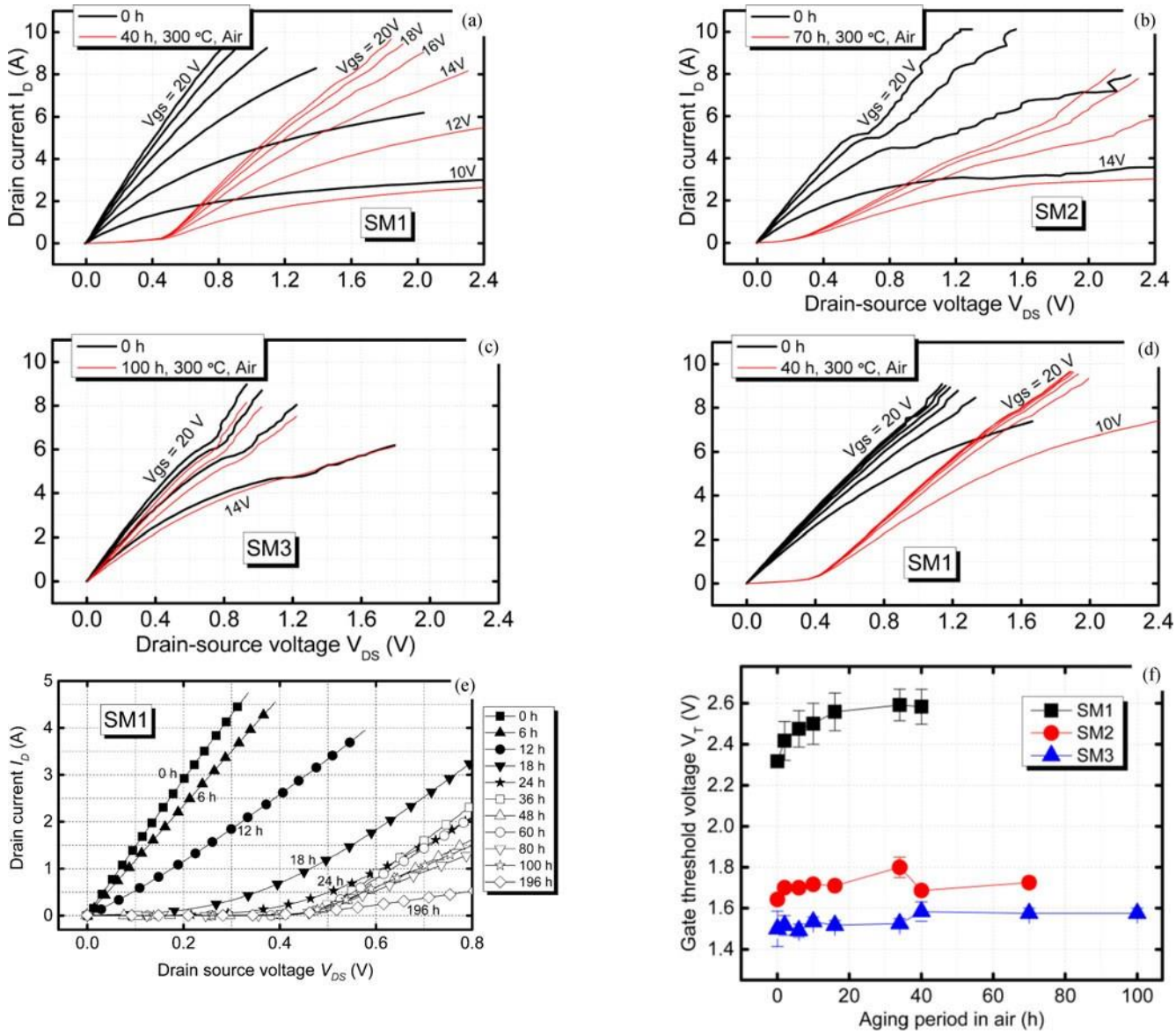

Fig. 10. (a–d) Measured linear region output characteristics for the three different SiC MOSFET types before after aging in air for storage periods up to 100 h at 300 °C. V_{gs} was increased in 2 V steps up to +20 V and all measurements were taken at room temperature except (d) which was measured at 150 °C in order to illustrate the temperature dependence before and after aging. These measurements were taken after 0, 40, 70 h for SM2 and SM3 die only and 100 h for the SM3 die only. (e) Aging time period dependence of the output characteristics for up to 196 h to illustrate the change versus aging time a long time after the rectifying output becomes evident. (f) Threshold voltage shifts due to aging in air at 300 °C for up to 100 h. In this case, single-shot measurements were taken carefully to limit the possibility of further measurement pulses influencing the results.

for the 20 V gate bias. The SM2 device suffered an even greater $R_{DS,ON}$ increase of 125%. However, the output characteristics for the SM3type device shown in (c) are still completely linear even after 100 h of storage in air, and with a comparably smaller $R_{DS,ON}$ increase of 21% (from 96 to115 mΩ). The measurements shown in Fig. 10(a) and (b) were all conducted at room temperature. The same SM1 device was also measured at 150 °C, before and after air storage, as shown in Fig. 10(d); in this case, the on-state resistance has increased by 70% (from 121 to 207 mΩ). The transconductance (g_m) has also increased at this elevated measurement temperature, particularly at the lower gate voltages. We attribute this g_m increase to the approximately 1 V reduction in threshold voltage at 150 °C which, according to the standard transconductance equation for a power DMOSFET, would give a 10% increase in g_m for V_{gs} = 10V but only a 5% increase at V_{gs} = 20V. These results also indicate that the knee voltage for the nonlinear response of device type SM1 has decreased from approximately 400 mV at room temperature to 250 mV when measured at 150 °C, comparing (a) to (c) and projecting along the resistance slopes to the *x*-axis intersects. The roomtemperatureknee value for the SM2 device is even lower at approximately 220 mV. Fig. 10(e) plots the temperature dependence of the air storage aging process for the SM1 device type for 6 h measurement intervals. These results confirm that the transformation from a linear to nonlinear output characteristic *does* occur quite suddenly; in this case after between 12 and 18 h

approximately, and the transformation appears to be complete after approximately 40 h. There is also a gradual increase in the on-state resistance from 0 to 200 h, which seems to be independent of the occurrence of the nonlinear characteristic. Fig. 10(f) shows the measured threshold voltage versus air storage aging period for all three device types. The only significant shift was found for the SM1 device type. Further work is required to determine whether this shift is due to the aging process, or is simply an accumulation of trapped charges due to the multiple periodic measurements.

2) Temperature Cycling in Air: A number of SM1-type die were also temperature cycled in a thermal cycling chamber with air atmosphere. It was found that these die had the same electrical characteristics before and after 1000 temperature cycles from 0 to 350 °C, with no nonlinearity. In this case, the thermal cycling profile spends approximately 5 min per cycle *above* 300 °C, for a total of 83 h, and 15 min per cycle below 300 °C. This situation is curious because all of the devices aged in air at a constant temperature of *exactly* 300 °C showed the nonlinear output characteristics after less than 40 continuous hours. The reasons for these differences are under investigation. However, it appears from these results that the cumulative time period above 300 °C is *not* equivalent to a continuous period.

3) N_2 Atmosphere Aging: The results for our inert atmosphere aging at 300 °C are shown in Fig. 11 for the three device types. In these cases, the SM1-type device aged in N_2 showed a slightly nonlinear characteristic at the 1000 h measurement point, but not after 570 h (no measurements were taken inbetween). In contrast to the air storage results where the SM1 devices degraded before the SM2 devices (after 40 h and 70 h, respectively), the inert storage results showed the opposite order; the SM2 device type had the nonlinear output characteristic at the 570 h measurement point. Unfortunately, this SM2 device was not functional after 1000 h for reasons unknown. In common with the air-aged die, the SM3 device type produced the normal MOSFET linear output characteristic after 1000 h in N_2 storage. The appearance of the nonlinear responses, even in this inert N_2 atmosphere, but only after approximately ten times the durations for devices stored in air, strongly suggests that the N_2 atmosphere did contain some small amount of oxygen. The actual levels of oxygen in this laboratory tube furnace are currently under investigation.

4) Validation of Nonlinear Output Characteristic Theory: Our assumption about the possible presence of a (p-type) nickel oxide adjacent to the n-type SiC substrate has been validated by milling trenches in the drain contact at various positions on the die surface using a focused ion beam (FIB) system, an example of which is shown in Fig. 12(a). The associated SEM image of the drain contact metallization stack on the sidewall and energy dispersive X-ray elemental analysis revealed the formation of a continuous layer of nickel oxide on top of the nickel diffusion barrier, under the surface of the silver back metallization as shown in Fig. 12(b).

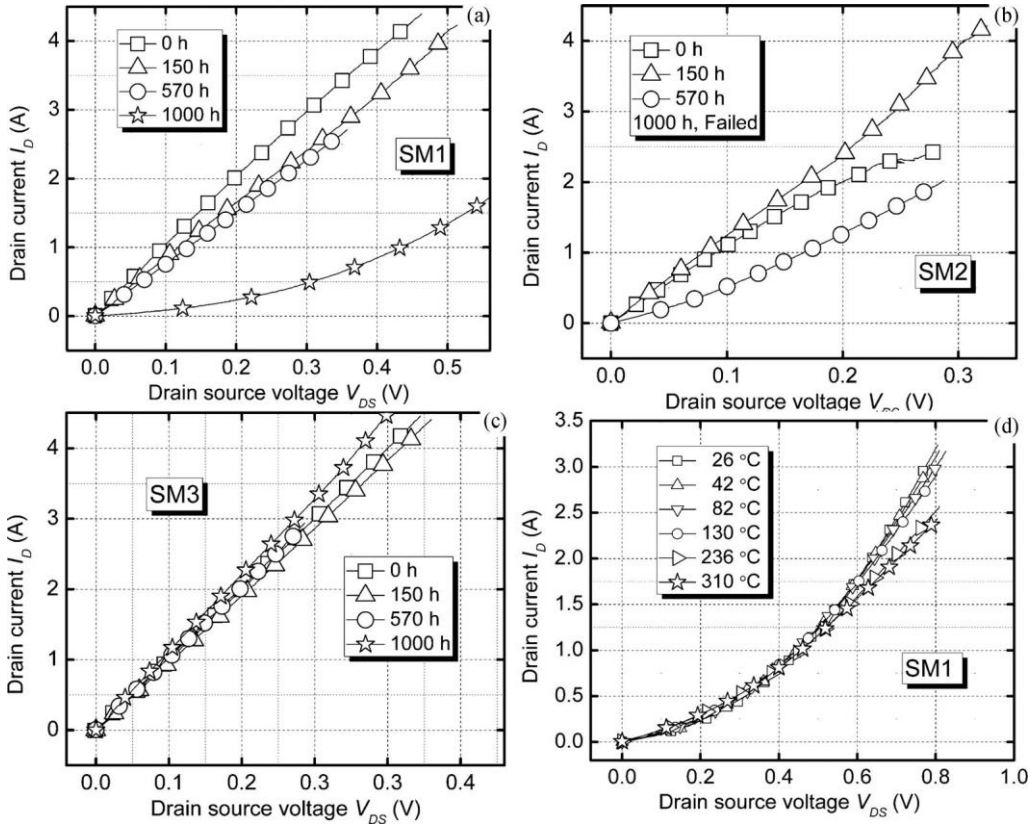

Fig. 11. (a–c) Measured linear region output characteristics versus inert N_2 atmosphere storage period at 300 °C for the three different SiC MOSFET device types. All measurements were taken at room temperature and for a gate voltage of +20 V. (d) Temperature dependence of output characteristics for the SM1 die after storage in N_2 atmosphere for 1000 h at 300 °C.

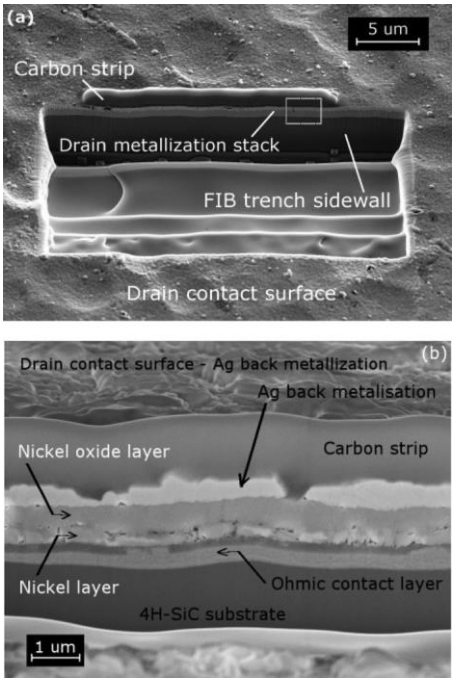

Fig. 12. (a) Tilted surface SEM image of one of a number of FIB trenches milled in the drain side of the SM2 die after heating for 1000 h in N_2. (b) Cross section SEM image of drain contact metallization stack taken from the FIB trench sidewall, indicating the formation of a nickel oxide layer under the silver.

IV. Discussion

The operation of these SiC MOSFETs up to at least 300 °C has beenshowntobefeasibleinthiswork,evenforextendedperiods inair.However,wehavedemonstratedthatthehigh-temperature environment produces high levels of on-state resistance and V_T instability that will have to be considered carefully in the system design of a real high-temperature power converter. We have also introduced a new issue in this work; the time-dependent thermal aging of these SiC MOSFET devices when oxygen is present at high temperatures, such as might be the case if the packaging hermetic seal eventually fails.

A. Consequences and Management of V_T Instability

It is likely that the next generations of devices will still have the problem of gate threshold voltage instability (or drift) to some degree, at least when operated at very high temperatures, and for both positive and negative gate bias. It would be difficult and expensive to monitor and correct the threshold voltage drift in a real system, mostly because the device turn-ON and OFF times are so fast (in the order of tens of nanoseconds). Both a positive and negative high temperature bias stress would be needed to correct the drift if V_T were to be monitored. The question then arises about how and if it can be managed for real high-temperature applications, or not.

1) Positive BTS Instability Solution: We have demonstrated the V_T instability for positive gate bias, including for a switched bias, and shown that the V_T increase can be significant at high operating temperatures. However, we have also demonstrated that, despite this large shift, the impact on the drain current appears to be almost negligible, and the amount of V_T drift is limited and dependent on the highest operating temperature. In our opinion then, this positive shift, although undesirable, can be easily tolerated and compensated for if thought necessary as part of the current derating strategy for the whole system.

2) Negative BTS Instability Solution: The constant negative gate bias presents a particular problem; we have demonstrated thatalargenegativegatebiasproduceslargeandextremelyrapid negative drifts of the threshold voltage when operated at high temperatures. These drifts are cumulative but have been shown in this work to be limited in magnitude and can be counteracted by a high temperature positive gate bias stress. However, such large negative shifts, when coupled with the negative temperature dependence of the threshold voltage, make the possibility of the threshold voltage approaching zero volts, or potentially much lower, a realistic possibility even at modest temperatures is demonstrated in Fig. 5. The most likely scenario where large negativethresholdvoltagedriftscouldoccurinarealapplication isifaconverteroperationisstoppedtemporarilywhileoperating atveryhightemperatures,andhaltingtheswitchingoperationby holding all the SiC MOSFET devices off with a high, e.g., maximum negative gate bias. When switching operation resumes and the device junction temperatures rise again, the device threshold voltages will decrease even further due their negative temperature coefficients. It is feasible that, for some SiC MOSFET device products, the drift might be so high under high-temperature conditions that the threshold voltage may reduce down as far as the gate turn-OFF voltage itself. In this case, the devices would enter a normally-on state, which would have disastrous consequences for the converter and its application. Alternatively, as demonstrated in Fig. 9, it might reduce low enough to cause high drain leakage currents to flow. Although the current leakage was shown to be very low over the full temperature range in the off state, and for high starting values of threshold voltage, as the threshold reduces below approximately 150 mV, the leakage increases exponentially and the power dissipation would increase accordingly. As was mentioned earlier, using a lower negative gate voltage, closer to zero volts, significantly reduces negative threshold voltage drift. Using a zero gate voltage would eliminate drift from occurring in a real application completely, and so eliminate the risks of high leakage currents or devices becoming normally-ON. Implementing a zero or small negative gate voltage to eliminate or substantially reduce drift appears to be a sensible strategy then. However, some devices have inherently low threshold voltages at room temperature, e.g., 1.5–2.0 V and their temperature dependence can reduce these values close to zero or less, even if the stress-induced drift can be eliminated completely. Such devices may suffer from false turn-ON in circuits and systems where cross-talk or other noise is present and a negative gate bias may have to be mandated to

compensate for temperature dependence and stress-induced drifts in such noise scenarios.

Ultimately, this threshold instability or drift feature might becomealimitingfactorfortheveryhigh-temperatureoperationof someSiC MOSFET devices andmustbereduced asfaraspossible infuturedevices. Itappears that thebest way tomanage thisdrift in very high-temperature applications for the time being is to either entirely eliminate negative drift by using a zero-volt gate bias or at least minimizing it by using the lowest negative gate voltage that provides sufficient noise margin. Selecting devices that have inherently higher threshold voltages, e.g., 3.0–4.0 V, lowertemperaturedependenceofthresholdvoltageandlowdrift will also reduce the risks highlighted in this section.

3) Consequences for Paralleling of Devices: The paralleling of devices to share current and account for the current reductions at high temperatures may also present an issue. It will almost always be the power module designer's goal to distribute heat losses as evenly as possible between die in order to more effectively share current. However, in practice, there will always be a complex interaction of contributions from slight steady-state and large transient temperature variations as well as from characteristic differences from die to die such as $R_{DS,ON}$, V_T, and transconductance. V_T drift must also play a part in this, and should be considered during the design phase for high-temperature applications. In the worse-case situation, the threshold voltages of different die working in parallel and sharing current may drift far apart such that a few die with a low V_T may take the full transient current, with possibly disastrous consequences. However, it seems feasible that such a transient heating situation might help balance the threshold voltages between paralleled devices. Further work is needed to determine how V_T drift might affect current sharing in these situations.

B. Consequences and Management of High $R_{DS,ON}$

Low on-state resistance is one of the main selling points for allkindsofpowerdevicesandthereisalwaysacontinuouseffort by manufacturers to reduce it. For example, recent significant reductions of around 50% of the drift resistance have been made by wafer thinning for both SiC and Si power devices.

Although the room temperature values of the on-state losses of the SiC MOSFETs are low, we have demonstrated in Fig. 2 that they are extremely high at high temperatures. In order to manage thehigh$R_{DS,ON}$,thedevicesmustbederatedorparalleledinthe usual manner to meet the overall current demand at the highest desireddevicejunctiontemperature.Thedesignermusttakeinto account the switching losses, ambient temperature, packaging thermal resistance, and cooling system performance, and verify that the system will not overheat and devices will not suffer from thermal runaway under any real thermal or electrical load conditions. When derating, any small current reductions from potential positive V_T drift may also be taken into account. These high temperatures will ultimately be the driving force for their V_T instabilities; therefore, any future reductions in $R_{DS,ON}$ will be beneficial in this respect too. Depending on the packaging and cooling performance, the steep positive temperature coefficient of $R_{DS,ON}$ may make it necessary to limit the durations of high-temperature operation in some applications, and where practical. Future devices must reduce this temperature dependence of $R_{DS,ON}$ as far as possible to limit the need for current derating in high-temperature applications. Fortunately, the positive temperature coefficient of $R_{DS,ON}$ demonstrated all the way up to 350 °C in Fig. 2 ensures good current sharing when paralleling these devices in high current converters.

When operating at high temperatures, large heat transients may be a particular issue, because of the temperature dependence of the on-state resistances. We have demonstrated in our previous simulation and validation work that, with these same high on-state resistances and temperature dependencies, the thermal transients in a high power automotive inverter drive application are both extremely high and fast, with thermal transients as high as 200 °C in 15 s occurring [24], [25]. Accumulation of heat due to successive high magnitude heat transients must be avoided. Therefore, it is of extreme importance that the thermal path to the heat-sinking be as low as achievable, without any bottlenecks in the packaging that could lead to overheating. Inparticular,thehighestthermalconductivitydieattachsolution possible should be implemented. For example, this might necessitate implementing a high silver solids content sinter paste or solid core die attach on a thick copper heat-spreader. Thermal grease, or any other high thermal resistance alternatives must be kept far away from the die. For example, it might not be appropriate to use a baseplate-free design where a DCB-type substrate is mounted directly on top of a cold plate or other heatsink with a grease layer, because the grease layer would present a high thermal resistance bottleneck close to the die.

C. Thermal Aging and Associated On-State Losses

We have demonstrated a thermo-mechanical aging feature of the devices which eventually leads to the sudden appearance

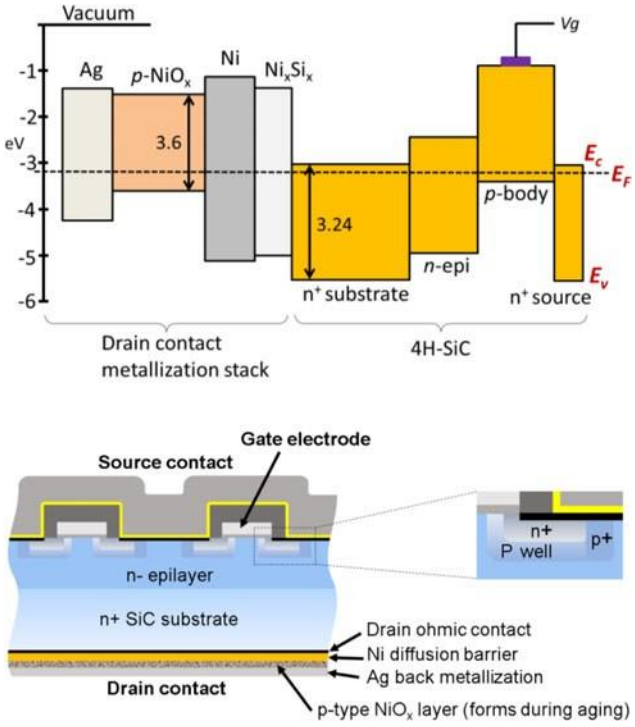

Fig. 13. Band energy alignment diagram and associated simplified SiC D-MOSFET device structure, indicating the position of the NiO_x layer that appeared on the back of the drain contact metallization stack.

of a rectifying type response in the output characteristic after tens of hours of high-temperature exposure to air, or many hundreds of hours in a lower oxygen atmosphere. Such an exposure to air might occur in a real application if there was a breach of hermetic sealing, which would be a real possibility for power module packaging operating in high-temperature thermal-cycled applications.

1) Nonlinear Response Theory: This nonlinear or rectifying type output characteristic has been demonstrated before for nickel silicide based 4H–SiC ohmic contacts aged in air for 150 h at 400 °C [6]. In that case, the author attributed this to degradation of the ohmic contact itself. However, we present an alternative theory here, based around the formation of the NiO_x layer presented earlier: this rectifying behavior seems to be equivalent to that of a diode in series with the drain–source current. It also emulates the output characteristics of an Si IGBT, which has the same basic structure as a DMOSFET but uses a p+ substrate. Our diode theory then appears to be plausible, since the nickel oxide is a well-known p-type semiconductor. The device cross section and associated band diagram are shown in Fig. 13. It can be seen from this that the material layers in between the p-type NiO_x and n-type SiC substrate layers are metals, or metal-like, and, therefore, act like highly doped n-type semiconductors. We, therefore, propose that the SiC MOSFET devices effectively have a heterojunction diode in series with their drain contacts and this causes the nonlinear output characteristic after a period of aging in an oxygen-containing atmosphere.

2) Additional Time Delayed V_{DS0} On-State Losses: This IGBT-like rectifying response will impose an additional conduction loss in the same way as for an IGBT's V_{CE0} built-in potential parameter, in addition to the normal temperature dependent MOSFET on-state losses. The total conduction losses for this new situation are shown as follows:

$$P_{\text{cond}} = \int_{T0}^{T2} I^2 \cdot R_{\text{DS,ON}} + \int_{T0}^{T2} I \cdot V_{\text{DS0}} \qquad (1)$$

where V_{DS0} is the built-in potential value of V_{DS} at the knee in the nonlinear curves shown for these SiC MOSFETs in Figs. 10 and 11, and is equivalent to the IGBT's V_{CE0} parameter. As can be seen from this equation, the $I^2.R_{DS,ON}$ losses occur for the entire operation from time $T0$ to $T2$. However, the new losses due to the built-in potential only occur from time $T1$, after the output characteristics become nonlinear.

3) Feasibility of Operating in Air or Low-Oxygen Environments: Asthisisarelativelyslowthermalagingprocess and only results in increased on-state losses, and not outright failure, the good performance of these SiC MOSFET devices at very high temperatures opens up the possibility of operating the devices in air. Low vacuum or inert gas sealed atmospheres with inherently low but nonzero oxygen levels might also be considered as alternatives to hermetic sealing or high temperature capable silicone gels or other alternative encapsulates. However, when operating in such atmospheres, care must be taken to ensure that high leakage or breakdown at the edges of the device occurs at the working temperature of choice, and under real switching transients with real loads. When tested in air for reverse breakdown, we have seen arcing at the edges of some SiC MOSFET types at less than their rated breakdown voltages, while this was not found for other types even slightly above their breakdown voltages. This presumably is because some manufacturers have designed their device terminations to reduce the electric field close to the edge of the die more than others, and/or have used different passivation materials with different insulation strengths.

4) Influence of Die Attach on Aging: We have attributed the sudden appearance of the nonlinear response to correlate with the occurrence of a continuous layer of nickel oxide (previously shorted out) after long periods of oxygen exposure at high temperature. In these tests, the die were simply placed drain-side down on a hotplate, and were not bonded to the surface. In real applications, the die will be bonded to a substrate with a die attach material. We, therefore, expect the diffusion of oxygen to be delayed by the die attach material and to occur first at the outer edges of the die. In a porous die attach microstructure, such as silver sintered bonds, there may be fast paths for oxygen diffusion, particularly if the microstructure has coarsened due to either high temperature cycling stresses [25] or high temperature storage stresses [26]. As mentioned in Section I, much work has been done by other authors to evaluate oxygen barriers between the ohmic contact(s) and the final metallization layer, whether it be aluminum on the source

contact side for wire bonding or silver on the drain side for soldering. However, it is not known currently whether the devices being evaluated in the present work have been fabricated with such features. In either case, our results suggest that these devices would benefit from the implementation of a higher performance oxygen barrier to enable them to survive for longer in an oxygen containing environment than we have demonstrated in this work.

5) LifetimeofDieComparedtoPackaging: Itispossiblethat thedevicepackagingmayfailinotherwaysbeforethisdegraded output characteristic occurs for the devices, particularly in thermal cycled applications where the thermo-mechanical stresses can be extremely high. For example, earlier in this work, we reported that the SiC MOSFET die survived 1000 temperature cycles from 0 °C to 350 °C. However, in our previous works, we have demonstrated much shorter lifetimes under the same temperature cycling conditions for various candidate high temperature capable die attach materials and DCB-type substrates [27], [28]. In the future, as the requirement for a high temperatureoperating capability becomes more widespread, and the SiC power devices are made available at higher temperature ratings, it is highly likely that the packaging materials will be improved accordingly.

V. Summary and Outlook

We have demonstrated the feasibility of operating these commercially-available second-generation SiC DMOSFET devices at temperatures well above their rated temperatures, even as high as 350 °C. The devices showed excellent forward and reverse characteristics up to this temperature. However, the R_{DS} on-state losses are extremely high at high temperatures and, when added to switching losses, will have to be managed by current derating, dimensioning the cooling system, and/or limiting the periods of high-temperature operation. The threshold voltages are also unstable at high temperatures and drift significantly from their nominal values. Some amount of drift is likely to feature in the next generations of devices, at least at very high temperatures and gate potentials. For the devices under test in this work, the positive drift appears to cause only minor current reductions and can be compensated for in the system design. There appears to be a risk that the significant negative drift demonstrated in this work could potentially allow the threshold voltage to reduce as far as the gate turn-OFF bias, and cause some devices to enter a normally-on state at very high operating temperatures. Recommendations were made to mitigate this risk. Exposure to oxygen at high temperatures has been shown to eventually cause a sudden increase in on-state losses due to the degradation of the drain contact metallization. The additional heat generated will then place an addition burden on the cooling system and power module packaging. When practical, these additional losses can be accounted for in the system design.

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