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Heteroepitaxial beta-Ga_2O_3 on 4H-SiC for an FET with Reduced Self Heating

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***Abstract*—A method to improve thermal management of β-Ga_2O_3 FETs is demonstrated here via simulation of epitaxial growth on a 4H-SiC substrate. Using a recently published device as a model, the reduction achieved in self-heating allows the device to be driven at higher gate voltages and increases the overall performance. For the same operating parameters an 18% increase in peak drain current and 15% reduction in lattice temperature is observed. Device dimensions may be substantially reduced without detriment to performance and normally off operation may be achieved.**

***Index Terms*—FET, Gallium Oxide, Molecular Beam Epitaxy, Normally-Off, Self-Heating, Silicon Carbide, Threshold Voltage**

I. INTRODUCTION

Wide band-gap semiconductor materials commonly thought of for use in power electronic devices include silicon carbide (SiC) [1-2], gallium nitride (GaN) [3] and diamond. SiC has shown the greatest potential to date in replacing silicon for DC power applications, indeed 4H-SiC diodes and MOSFETs are today commercially available. Diamond has been touted as the ideal material for high power electronics due to its large thermal conductivity, high breakdown field and high bulk carrier mobility. It has the potential to compete with both SiC for high voltage DC applications and GaN for RF power applications [4-6]. However despite recent advances, doping and substrate cost remains an issue [7-8].

In contrast, beta-Gallium Oxide (β-Ga_2O_3) could offer an alternative to 4H-SiC for power applications. Its key intrinsic material properties are competitive with diamond e.g. a band-gap of 4.8 eV and high breakdown field 8 $MVcm^{-1}$ [9-10]. Large scale growth is also far less challenging and possible at a fraction of the cost [11].

Despite the material structure being first investigated in the 1960s [12] it is only much more recently this material has been suggested for application in power electronic devices. Indeed, Ga_2O_3 thin-films have been successfully employed for a variety of applications including a window layer for solar cells and a transparent conductive oxide [13-15]. This holds promise for a larger degree of integration compared with traditional wide band-gap semiconductors e.g. into display screens or transparent electronics [16].

In recent years basic FET devices have been demonstrated [17-20], although p-type doping (which is notoriously difficult in wide band-gap semiconductors) is still a practical challenge. The best oxide solution is yet to be settled upon with work to date mainly focusing on Al_2O_3, although in theory SiO_2 provides a greater band off-set and hence reduced gate leakage [21-22].

In this paper a SILVACO Atlas non-isothermal model for β-Ga_2O_3 demonstrated in a recent paper is employed to recreate a device demonstrated by Higashiwaki *et al* [23, 18]. The low thermal conductivity of β-Ga_2O_3 (~0.2 $Wcm^{-1}K^{-1}$) [10] can be regarded as perhaps the most severe drawback for very high voltage applications. We demonstrate via simulation the advantages of engineering a thin film of β-Ga_2O_3 onto a good thermal conductor such as SiC (~5 $Wcm^{-1}K^{-1}$) to increase the thermal performance of β-Ga_2O_3 FETs.

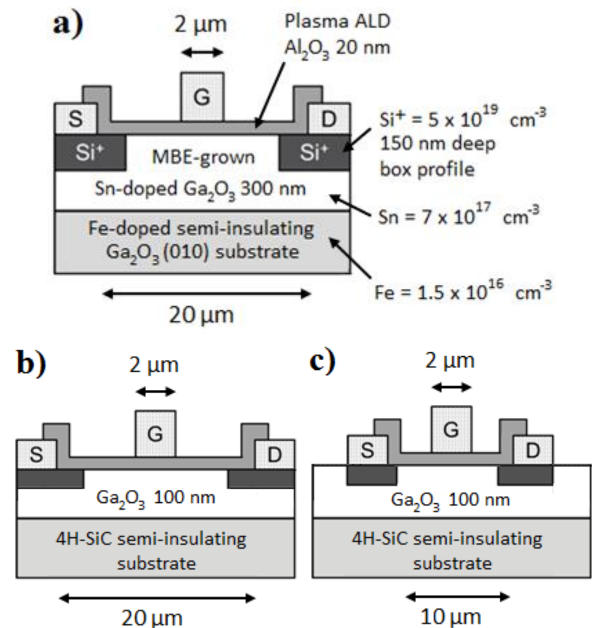

Fig. 1. Schematic showing the structure and doping of a) original MOSFET device based on β-Ga_2O_3 [18] and b) & c) adaptations made in this paper

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II. Simulation

Fig. 1 shows a cross-section of the FET modelled here. The semi-insulating β-Ga_2O_3 substrate material is detailed in the original paper as having a doping of 1.5 x 10^{16} cm^{-3}, while the dopant in the Molecular Beam Epitaxy (MBE) layer is 7 x 10^{17} cm^{-3} with half considered activated. The Si ohmic dopant is 5 x 10^{19} cm^{-3} with 3 x 10^{19} cm^{-3} activated. A 20 nm Al_2O_3 Atomic Layer Deposited (ALD) oxide layer covers the device with a source-drain spacing of 20 µm and gate length 2 µm. This device (Fig. 1a) suffers from self-heating effects due to the relatively poor thermal conductivity of β-Ga_2O_3 which reduces the saturated drain current value. One way to mitigate this is to use a substrate with a high thermal conductivity such as 4H-SiC. A recent study has shown the positive impact this can have even on Si based devices [24]. The lattice match of β-Ga_2O_3 to 4H-SiC is close at 3.04Å compared to 3.07Å respectively, allowing for low defect density materials to be grown and interfaces to be formed between β-Ga_2O_3 and 4H-SiC by growth methods such as MBE used in this instance.

A simple constant thermal conductivity and low-field mobility model was used for this study with main parameters summarised in Table 1.

TABLE I
SIMULATION PARAMETERS

Material	Parameter	Value
β-Ga2O3	Bandgap Energy	4.8 eV
	Thermal Conductivity	0.13 $Wcm^{-1}K^{-1}$
	Effective Mass	0.28 m_0
	Local Conduction Band Density of States	3.72 x 10^{18} cm^{-3}
	Epitaxial Layer Mobility	118 $cm^2V^{-1}s^{-1}$
	Epitaxial Layer Dopant Concentration	7 x 10^{17} cm^{-3} (3.5 x 10^{17} cm^{-3} activated)
	Substrate Mobility	20 $cm^2V^{-1}s^{-1}$
	Substrate Dopant Concentration	1.5 x 10^{16} cm^{-3}
4H-SiC	Bandgap Energy	3.23 eV
	Thermal Conductivity	3.7 $Wcm^{-1}K^{-1}$
	Effective Mass	0.41 m_0
	Local Conduction Band Density of Stateas	5 x 10^{18} cm^{-3}
	Substrate Mobility	460 $cm^2V^{-1}s^{-1}$
	Substrate Dopant Concentration	1.5 x 10^{16} cm^{-3}

β-Ga2O3 parameters taken from [12 & 25] whereas standard SILVACO parameters are used in the case of the 4H-SiC substrate

As many β-Ga2O3 parameters are not fully established yet care is needed to not pick unrealistic values. Electron effective mass is taken to be 0.28 m_o giving a calculated local conduction band density of states N_c = 3.72×10^{18} cm^{-3}, mobility of the channel layer and mobility of the semi-insulating substrate are set to be 118 and 20 $cm^2V^{-1}s^{-1}$ respectively [25].

A parameter (LAT.TEMP) was added to the model to account for poor heat flow in β-Ga_2O_3 material. The lattice temperature coefficient for the temperature dependence of electron mobility TMUN=2.0 was used as seen in Equation 1.

$$\mu_{n0} = MUN(\frac{T_L}{300})^{-TMUN} \quad (1)$$

Where μ_{n0} represents electron mobility adjusted for lattice temperature, MUN the originally input mobility value, T_L lattice temperature and TMUN the temperature dependence coefficient.

The material parameters of 4H-SiC are much better established and standard SILVACO parameters were used for this material.

III. Results & Discussion

Fig. 2 demonstrates the immediate benefit of switching to a 4H-SiC substrate for this technology, output characteristics are displayed for the original device as well as the modelled version on a 4H-SiC substrate simulated to have the same doping level (1.5 x 1016 cm^{-3}) as the original β-Ga2O3 substrate. Peak drain current increases for all gate bias points, an increase of 19% is seen for V_{gs} = +8V with peak lattice temperature reducing by 15% at this bias point, far extending the realm of operation of the original device.

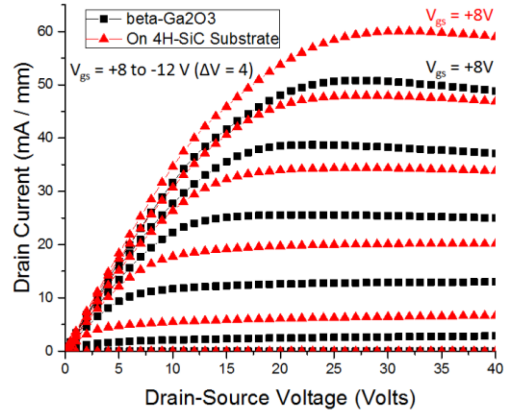

Fig. 2. Comparison of the output characteristics from a β-Ga_2O_3 MOSFET and the same on a 4H-SiC substrate, both are simulated to have a 300 nm thick epitaxial layer

A visual comparison is shown in the form of a heat contour map for the original device and the 4H-SiC substrate version in Fig. 3. For the β-Ga_2O_3 device at a V_{gs} of +8V and V_{ds} of +40V the lattice temperature reaches a peak of 166° C, for the same bias on a 4H-SiC substrate the peak lattice temperature reaches only 98° C.

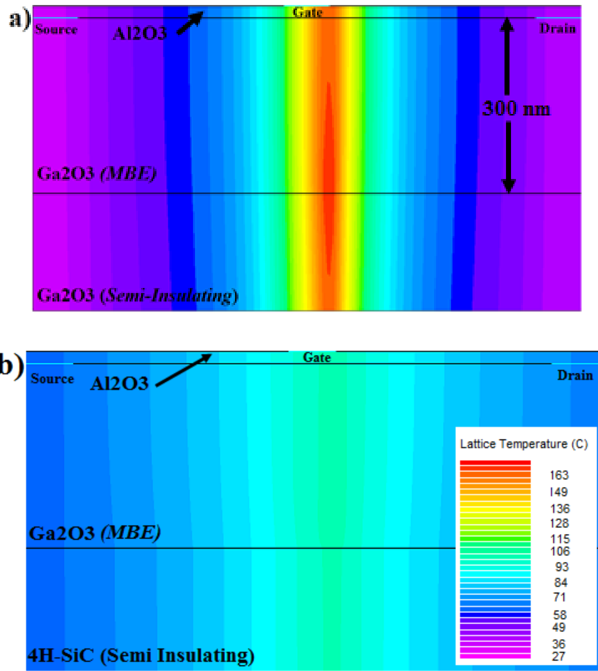

Fig. 3. Lattice temperature at V_{gs} = 8V for β-Ga_2O_3 (a) and 4H-SiC (b) substrate

The 4H-SiC version remains normally-on although this can be shifted in both cases by a reduction in thickness of the epilayer. Fig. 4. Shows the shift in threshold voltage (V_T) for modelled devices as the simulated epitaxial layer thickness is reduced, there is also an associated reduction in temperature.

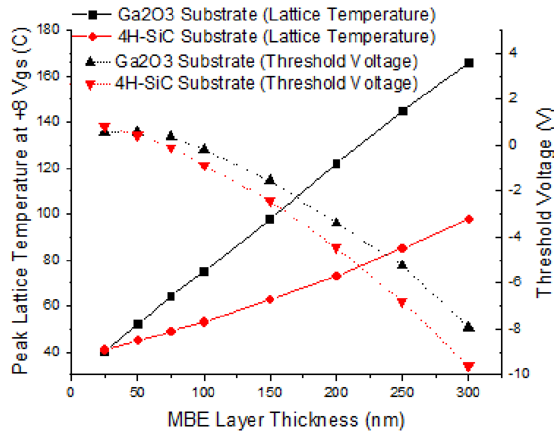

Fig. 4. Comparison of transfer characteristics for β-Ga_2O_3 MOSFET and the same on a 4H-SiC substrate

Fig. 5 shows the output characteristic of a 100 nm epitaxial layer FET on 4H-SiC device compared to the original β-Ga_2O_3 FET. Self-heating is virtually eliminated at this gate voltage (V_{gs}) of +8 V (lattice temperature = 53° C). Peak drain current is understandably reduced due to the more restricted and hence resistive route but the nature of this design and its improved thermal conductivity allows a much higher V_{gs} to be used.

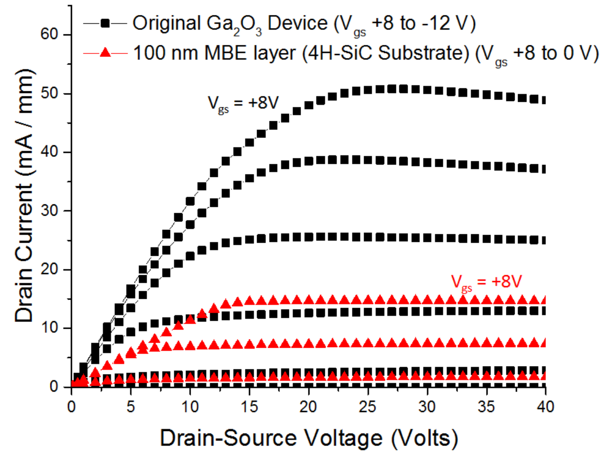

Fig. 5. Output characteristic for β-Ga_2O_3 substrate with 100 nm layer thickness.

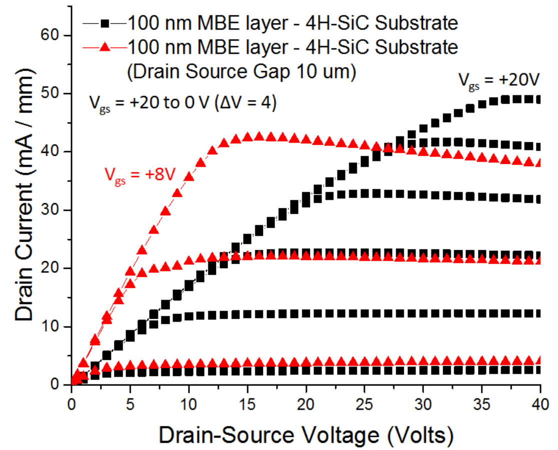

Fig. 6. Output characteristic for 4H-SiC substrate with 100 nm layer thickness, Vgs up to +20 (lattice temp max 71° C)

Fig. 6 shows how this device may be driven easily to V_{gs} = 20 V. A similar peak drain current to the original device is achieved although on-resistance of the device is increased. If however the source-drain gap is reduced to 10 µm a similar output characteristic to the original device may be seen with a substantially reduced V_T and a lower lattice temperature (91° C at V_{GS} = +8 V).

Analyzing current density for the β-Ga_2O_3 FET at voltages close to V_T the current path is partially forced through the semi-insulating substrate, albeit at a much reduced level due to the lower mobility of this layer. Reducing the MBE layer thickness ensures this occurs at a more positive V_{gs} and impacts upon the threshold voltage. On the 4H-SiC substrate the heterojunction present means negligible charge will migrate in to this layer giving rise to the marginal difference in V_T between substrates. This is visualized in Fig. 7.

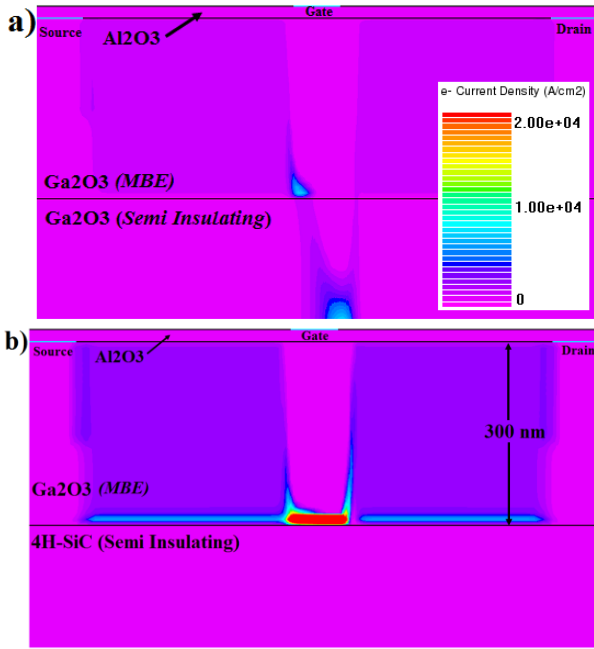

Fig. 7. Current route at Vgs = -8V for β-Ga_2O_3 (a) and 4H-SiC (b) substrate

Below a thickness of 100 nm the device becomes normally-off (below 75 nm for the 4H-SiC substrate). As the MBE layer thickness approaches 100 nm the shift in V_T plateaus and reducing beyond this point has little benefit and begins to severely limit current performance. With this reduced layer thickness less drain current is possible for the same gate voltage as the restricted route increases the resistance of the β-Ga_2O_3 MBE layer.

A source-drain distance of 20 microns is relatively large even for a power FET and utilising the 4H-SiC substrate allows further device scaling to increase current performance. Halving this to 10 microns and biasing at +8 V_{gs} a similar current level to the original device is obtained, still with a lower peak lattice temperature of 91° C. This scaling will of course put further stress on the dielectric layer. Simulation shows a maximum electric field of 1.22 $MVcm^{-1}$ even at +20 V_{gs} on the gate dielectric for the 100 nm on 4H-SiC device with reduced source-drain dimension. This is well within the remit of either Al_2O_3 or SiO_2 as a gate dielectric.

This demonstration allows many further routes to be taken in terms of scaling, the suitable lattice match of these two materials make it the perfect complement. Improvements in processing of this technology will undoubtedly yield more improvements from this promising material. It is accepted that 4H-SiC substrates are expensive however recent technological innovations such as those offered by Siltectra GmbH mean substrates may be split and recycled many times over [26]. The ability to grow high quality large area substrates of β-Ga_2O_3 also raises the possibility of wafer bonding to high thermal conductivity substrates.

IV. Conclusion

The replacement of the semi-insulating β-Ga_2O_3 substrate with a 4H-SiC alternative in this device yields two improvements. Firstly the reduction in self-heating due to the order of magnitude thermal conductivity of 4H-SiC compared to β-Ga_2O_3. Secondly due to this it is possible to scale the device in reducing the MBE layer thickness and reducing the source-drain gap, giving overall the same current performance with a drastically reduced V_T.

Future work should focus on the best gate oxide for this technology. Characterization of interface traps will shed some light on this matter and the best route to practically scaling these FETs. Attention also needs to be payed to ohmic metallization stacks as even in 4H-SiC devices stability of these at elevated temperature can still be an issue [27].

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