MOSFET degradation dependence on input signal power in a RF power amplifier

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Abstract

Aging produced by RF stress is experimentally analyzed on a RF CMOS power amplifier (PA), as a function of the stress power level. The selected circuit topology allows observing individual NMOS and PMOS transistors degradations, as well as the aging effect on the circuit functionality. A direct relation between DC MOSFETs and RF PA (gain) parameters has been observed. NMOS degradation (both in mobility and V_{th}) is stronger than that of the PMOS. Results suggest that transistors mobility reduction is the main cause of the RF degradation in this circuit.

Keywords: CMOS, MOSFET degradation, RF power amplifier, RF stress, aging.

1. Introduction

Aggressive device scaling has increased the relevance of stress-induced MOSFET degradation (due to dielectric aging mechanisms as Hot Carrier Injection, HCI, and Bias Temperature Instability, BTI) on circuit performance [1]. However, experimental observations of the device degradation under circuit operation conditions together with its impact on the circuit performance are not easy to obtain, because of the difficulty to access the transistor terminals once they are embedded in a more complex circuit. This problem is aggravated in radiofrequency (RF) circuits because of the practical impossibility to access internal nodes and the general complexity associated to high-frequency measurements. Thus, most experimental works about aging on RF amplifiers choose one-NMOS based-circuits where the access terminals for transistor and circuit are coincident [2,3,4]. In other works, the RF performance degradation is simply predicted by means of simulation, based on models of aged transistors [5,6,7]. In most works, aging is accelerated after a DC stress alone $-V_{DD}-$, which ignores the contribution of the RF signal component on the circuit degradation. This contribution may be relevant in power amplifiers (PA) that usually deliver high output powers, but little experimental evidence quantifies its importance. In [2], a single-transistor PA is stressed for two different combinations of V_{DD} and input power (P_{IN}) values, producing comparable degradation. Also in [3], the DC current degradation produced in a single NMOS is observed when subject to two particular DC and RF stress situations. In [8] the degradation of MOS DC parameters is observed when a RF signal is applied, with focus on frequency-dependence rather than power. In this paper, aging produced by RF stress of increasing power levels is experimentally analyzed on a linear PA implemented in a CMOS 65nm technology. The degradation of the NMOS and PMOS transistors in the circuit and its impact on the RF performance have been evaluated.

2. Samples and experimental setup

A schematic and a picture of the purposely designed and fabricated PA (DUT) in this work are shown in Fig. 1. The topology chosen for the PA is a self-biased complementary current-reuse amplifier. This topology allows observing the individual degradations of the NMOS and PMOS transistors, as well as the aging effect on the circuit functionality, allowing to obtain a realistic reliability relationship between the devices and circuit. Both NMOS and PMOS W/L are 180µm/60nm, split in 45 fingers. The circuit contains two feedback nets. An external resistive feedback provides self-biasing and sets the PA operating point in the gain region. Therefore this configuration is used for RF characterization and the stress process. This resistive feedback is external so it can be disabled for the individual transistor characterization. A second internal RC feedback provides RF impedance matching. With a nominal supply voltage of V_{DD} = 1.2V, the operating point is set to $V_{IN} = V_{OUT}$ = 520mV, I_{DC} = 7.3mA. The non-resonant topology allows a wideband response and power amplification in the range 300MHz – 8GHz. At 2.45GHz, the measured gain is S_{21} = 10.3dB, S_{11} = –8.5dB, S_{22}= –10.4dB, and the output referred 1dB compression point is P_{1dB} = 5dBm.

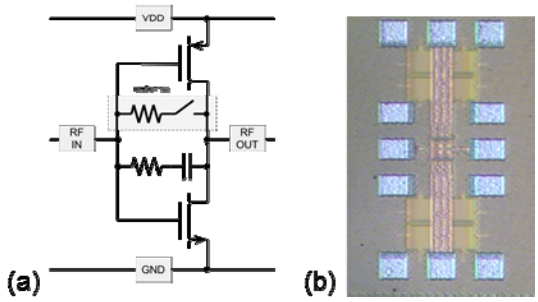

Fig. 1: Topology (a) and picture (b) of the designed and fabricated Power Amplifier (DUT).

A stress-measurement procedure was used to analyze PA aging. The experimental setup is shown in Fig. 2: a Rohde & Schwarz ZVM VNA is used to characterize the RF performance of the circuit as well as to provide RF stress, while a Keithley 4200 SPA is used to provide circuit supply voltage as well as to characterize each transistor independently in DC. The PA input and output are contacted with GSG coplanar passive probes, and two external bias-T provide connection of the input and output terminals to the VNA and to the external resistive feedback or SPA. The effect of all these cables and bias-T has been de-embedded, both in the RF measurements and at DC (including contact resistances). As the PA is always well matched to 50Ω, we can assure that the applied power reaches the PA input. A more detailed description of the set-up can be found in [9].

The RF stress consists in applying to the DUT an input signal at 2.45GHz, with power values (P_{IN}) ranged between -20dBm and 10dBm, together with V_{DD} =2.8V. In all cases, the stress duration was 30 minutes. Stress values and duration were chosen to provoke an appreciable damage to the circuit in a reasonable time. Each RF P_{IN} value was applied to a different circuit sample, which was characterized at nominal operation conditions before (fresh) and after the accelerated aging. The DC characterization consisted in the measurement of the electrical characteristics of the PMOS and NMOS transistors, as well as the DC transfer curves of the PA circuit (external R disabled), while RF characterization was only done at circuit (PA) level.

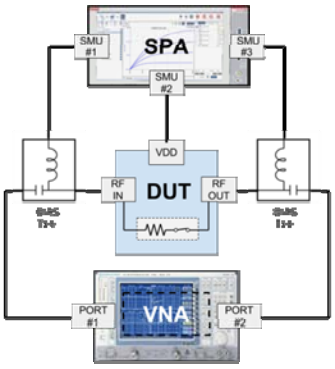

Fig. 2: Experimental set-up used for the stress and for the RF and DC characterization.

3. Results

Regarding the PA performance after aging, for all the stress cases a decrease of I_{DC} and a shift of the transfer curve to the right are produced (Fig. 3a). Fig. 3b plots the inversion voltage increase, ΔV_{INV}, produced as a consequence of each stress (where the inversion voltage V_{INV} is such that $V_{IN} = V_{OUT} = V_{INV}$, which is the DC self-bias voltage), as well as the decrease in the DC current consumption, ΔI_{DC}, as a function of P_{IN}.

Degradation of the threshold voltage (V_{th}) and mobility (µ) produced in both transistors is depicted in Fig. 4. Both parameters have been obtained by fitting the DC curves (I_D-V_{GS}) measured in deep ohmic region to a first order model including mobility degradation due to the vertical field [10]. Fig. 4a shows the relative ΔV_{th} increase (difference between stressed and fresh V_{th}, relative to the fresh values) for the NMOS (red

circles) and the PMOS (black squares) as a function of P_{IN} applied in the stress. Clearly, the V_{th} degradation in the NMOS is larger than in the PMOS, and the difference increases with P_{IN}. For -20 dBm (that can be considered a negligible RF power) ΔV_{th} is larger for the PMOS due the self-bias topology, where DC voltages at PMOS are higher than those at the NMOS terminals. However, the NMOS is more sensitive to RF stress conditions, and thus it suffers more degradation with the input power stress P_{IN}.

To distinguish the effects of the RF and DC components on the stress conditions, the experimental data have been fitted to a potential law (PMOS black thick line and NMOS red thick line). The equation used is shown in Fig. 4a. As the DC component is the same for all these measures, it produces a constant effect (C parameter in equation), while the effect of the RF component is fitted by a potential law (A and B parameters in equation). Dashed lines represent the V_{th} variation due the DC voltages applied to the PA for the NMOS (red) and the PMOS (black).

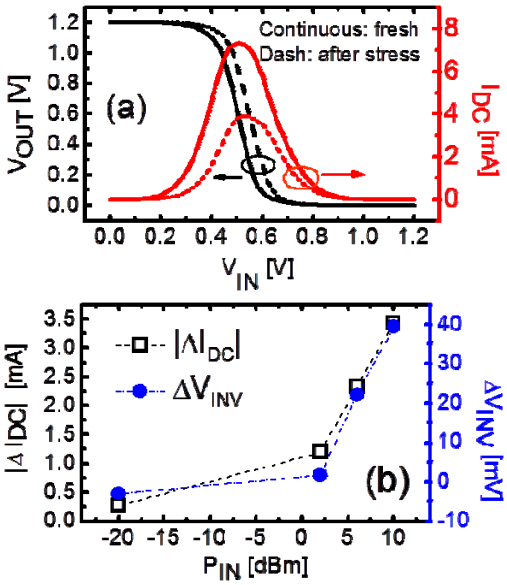

Fig. 3: a) Example of the variation of the inverter transfer curve and I_{DC} before and after a stress of V_{DD}=2.8V and P_{IN}=10dBm at 2.45GHz during 30 minutes. b) $|\Delta I_{DC}|$ and ΔV_{INV} as a function of the P_{IN} applied during the stress.

Fig. 4b shows the relative mobility reduction, Δμ, as a function of P_{IN}, which is also stronger for the NMOS transistor. Again, for neglectable RF signal power, Δμ is larger for the PMOS. However, as P_{IN} increases mobility reduction in the NMOS becomes more relevant. The same fitting has been done to the experimental Δμ, represented in Fig. 4b (thick lines) together with the DC stress contribution (dashed lines).

This degradation of the transistor parameters produces the observed change in the DC operating point of the PA, which in consequence results in a degradation of its RF performance. An example of the gain parameter S_{21} measured before and after the stress is shown in the inset of Fig. 5 around the 2.45 GHz frequency of interest, where a decrease of about 1dB can be observed. Both input and output have always been matched even after stress (a variation of just few tenths of dB in S_{11} or S_{22} has been observed). The impact of PA aging on the circuit gain is quantified in Fig. 5, where the degradation observed in the S_{21} parameter after the stress application is represented as a function of P_{IN}.

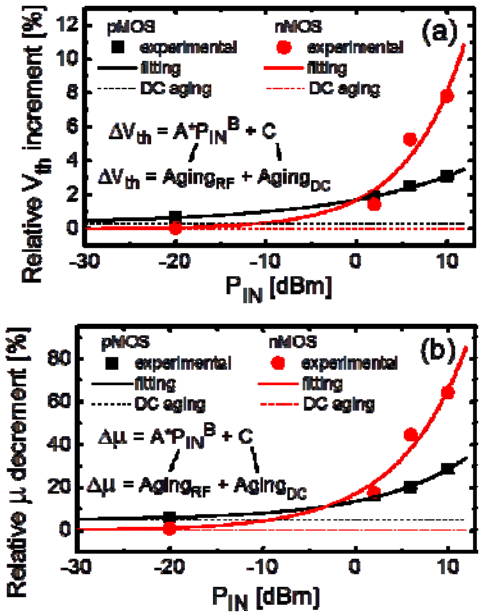

Fig. 4: a) Relative V_{th} degradation of the NMOS and PMOS and b) relative mobility degradation, as a function of the P_{IN} applied during the stress.

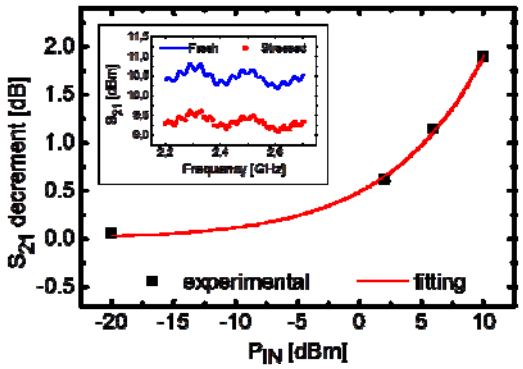

Fig. 5: PA gain variation as a function of P_{IN}. Inset: S_{21} parameter measurement of a fresh PA (line), and after a 30min stress of V_{DD}=2.8V and P_{IN}=6dBm (circles), around the 2.45GHz range of interest.

Fig. 6 shows the I_{DC} variation as a function of the amplifier gain degradation for the different P_{IN}. A linear relationship between the I_{DC} and gain degradation as a consequence of the stress is observed, which evidences the degradation of RF performance as a consequence of the DC degradation, in coherence with first-order analytical derivations [2,6,10]. Finally, the relationship between RF performance degradation (gain) and degradation of the transistor parameters (V_{th} and mobility) is shown in Fig. 7. NMOS degradation (both in V_{th} and especially in mobility) is stronger than that of the PMOS. Moreover, the relative mobility variation in both transistors is larger than the relative V_{th} variation, which points the mobility wear out as the main cause of the RF degradation in this circuit.

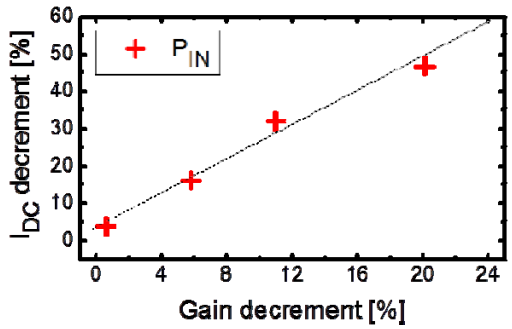

Fig. 6: Relative I_{DC} decrement as a function of relative gain decrease. A linear relation between the I_{DC} and gain decreases is observed.

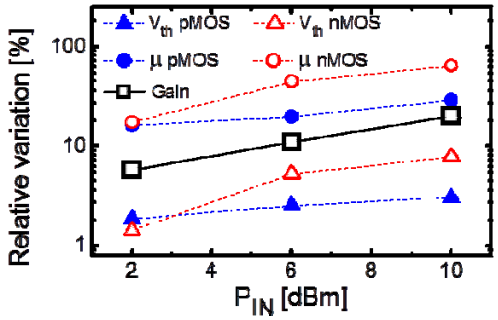

Fig. 7: Relative variation of DC parameters (NMOS and PMOS V_{th} and mobility) and a RF parameter (gain) as a function of P_{IN}.

4. Conclusions

MOSFET aging produced by RF stress has been experimentally analyzed on a purposely designed RF power amplifier, whose topology allows observing the individual degradations of the NMOS and PMOS circuit transistors and their impact on the circuit functionality. It has been observed how the RF signal produces important degradation of the MOSFETs and PA performance, significantly larger than that produced by DC voltages alone, in this self-biased topology. Transistor aging increases with the RF input signal power following a potential law, being larger for the NMOS than for the PMOS, both in V_{th} and especially in mobility. A direct relation of DC and RF parameters (gain) degradation has been observed, being the device mobility aging the dominant cause of the RF circuit damage.

Acknowledgements

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References

[1] V. Huard, F. Cacho, X. Federspiel, W. Arfaoui, M. Saliva, D. Angot, "Technology scaling and reliability: Challenges and opportunities", International Electron Devices Meeting (IEDM), (2015) 20.5.1-20.5.6.

[2] T. Quémerais, L. Moquillon, V. Huard, J.M. Fourniel, P. Benech, N. Corrao, X. Mescot, "Hot-Carrier Stress Effect on a CMOS 65nm 60GHz One-Stage Power Amplifier", IEEE Electron Device Letters (2010) 927-929.

[3] C. H. Liu, R. L. Wang, Y. K. Su, C. H. Tu, Y.Z. Juang, "DC and RF Degradation Induced by High RF Power Stresses in 0.18-μm nMOSFETs", IEEE Trans. Dev. Mat. Rel. (2010) 317-323.

[4] C. D. Presti, F. Carrara, A. Scuderi, S. Lombardo, G. Palmisano, "Degradation Mechanisms in CMOS Power Amplifiers Subject to Radio-Frequency Stress and Comparison to the DC Case", International Reliability Physics Symposium (IRPS) (2007) 86-92.

[5] P. M. Ferreira, H. Petit, J.F. Naviner, "A new synthesis methodology for reliable RF front-end Design," IEEE Int. Symp. on Circuits and Systems, (2011) 2926-2929.

[6] S. Mahato G. Gielen, "Impact of transistor aging on RF low noise amplifier performance of 28nm technology: Reliability assessment", IEEE Int. Conference on Electronics, Circuits and Systems, (2013) 413-416.

[7] E. Xiao, P.Zhu, J.S. Yuan, C. Yu, "Analysis and modeling of LNA circuit reliability," IEEE Radio Freq. Integrated Circuits Symp., (2005), 69- 72.

[8] G. T. Sasse, F. G. Kuper and J. Schmitz, "MOSFET Degradation Under RF Stress," in *IEEE Trans. on Electron Devices*, vol. 55, no. 11, (2008), pp. 3167-3174.

[9] E. Barajas, D. Mateo, X. Aragones, A. Crespo-Yepes, R. Rodriguez, J. Martin-Martinez, M. Nafria "Design of a Broadband CMOS RF Power Amplifier to establish device-circuit aging correlations", Int. Conf. On Microelectronic Test Structures ICMTS (2017), 99-101.

[10] J. S. Yuan, Y. Xu, S. D. Yen, Y. Bi and G. W. Hwang, "Hot Carrier Injection Stress Effect on a 65 nm LNA at 70 GHz," in *IEEE Transactions on Device and Materials Reliability*, vol. 14, no. 3, (2014), 931-934.