Experimental time evolution study of the HfO_2-based IMPLY gate operation

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***Abstract*—. In the last years, memristor devices have been proposed as key elements to develop a new paradigm to implement logic gates. In particular, the memristor-based material implication (IMPLY) gate has been presented as a potential powerful basis for logic applications. In the literature, the IMPLY operation has been widely simulated but most of the efforts have been just focused on accomplishing its truth table, only considering the initial and final states of the gate. However, a complete understanding of the time evolution between states is still missing and barely reported yet. In this work, the time evolution of memristor involved in an IMPLY gate are studied in detail for every case of the gate. Furthermore, the impact on IMPLY gate operation of the internal resistor connected in series with the memristors of the IMPLY gate is included.**

***Index Terms*— Resistive Switching, Material Implication, IMPLY, logic, memristors.**

I. Introduction

Memristors have acquired a huge importance in the last years for their advantageous characteristics mainly in terms of fast speed, high endurance and low power consumption [1]–[5]. Memristors main feature is based on the resistance switching (RS) phenomenon [6] which, in Metal-Insulator-Metal and Metal-Insulator-Semiconductor (MIM/MIS) structures, consists in the change of the dielectric resistance maintaining it in a non-volatile mode [7]. In some devices, this RS mechanism has been attributed to a formation and disruption of a metallic or non-metallic conductive filament (CF) [8]–[10] through the dielectric. When the filament is not formed or partially disrupted, the device is at high resistance state (HRS) and current barely flows (I_{OFF}). On the other hand, if the filament is formed and connects the device electrodes, then the low resistance state (LRS) is reached allowing large currents to flow through the dielectric (I_{ON}). A current limit is required when changing from HRS to LRS to allow the switching and avoid the final breakdown of the dielectric. The HRS and LRS states can be related with the two Boolean values implicated in digital operations, "0" and "1", respectively. This feature, together with the possibility of successively changing between different resistance states, allows the use of memristors as bit storage elements, with an increasing interest for the implementation of logic operations [11], [12]. Although some memristor issues as the switching dispersion or endurance degradation have to be still solved, the memristor potential for memory and logic applications is huge and with a lot of interest in the scientific community. Focusing on the logic field, Borghetti et al. proposed in [13] the memristor-based material implication (IMPLY) logic gate which consists in a 'stateful' logic where the data can be processed and stored in the same element. The simplicity of the IMPLY gate structure and its huge versatility are very promising characteristics for the use of material implication in future computational architectures. In the literature, adders, multipliers [12], [14], [15] and other type of logic circuits [16], [17] have been proposed using material implication logic. However, most of these works results are only based on simulations, without analyzing experimentally the real performance of the IMPLY gate. Moreover, authors are mainly focused on the verification of the IMPLY truth table, considering only the input and output states of memristors [13], what is indeed interesting in digital operations. Although some authors have barely covered the evolution of memristors currents during gate operation [16], a detailed analysis of such an evolution along time is still missing. However, this study is completely necessary for a deep knowledge of the IMPLY cell performance. Therefore, the focus of this work is to study the time behavior of the HfO_2-based memristors forming the IMPLY cell during the gate operation.

II. IMPLY Gate performance

IMPLY logic gate consists of two memristors (named P and Q) used as bit storage elements whose bottom electrodes are connected (Fig. 1(a)). Afterwards, they are connected to a resistance (R_G) whose free terminal is grounded and whose value must be LRS < R_G < HRS [13]. The voltage of the node at which both memristors bottom electrodes and R_G are connected is named as V_G. Top electrodes of memristors are biased to specific voltage pulses (V_P and V_Q). Regarding logic functionality, whereas in standard logic gates different voltage levels are related to the two binary states, in the case of the IMPLY gate, the binary states are associated to different memristor resistive states (or the current values for this resistance states). Furthermore, while inputs and outputs are differentiated each other in voltage-based logic gates, IMPLY gate makes use of one of the input memristors as the output too. Considering P and Q as the two input memristors of the IMPLY gate and Q as the output memristor as well, IMPLY is

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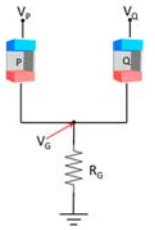
(a)



(b)

CASE	P	Q	Q (out)
1	0	0	1
2	0	1	1
3	1	0	0
4	1	1	1

Fig. 1. (a) Schematic circuit of the IMPLY gate with two memristors and a resistance (RG). Voltages VP and VQ are bias to be applied during operation. VG is the voltage in the node where memristors and RG are connected. (b) Imply truth table. P and Q are input memristors. Q (out) is the same memristor as the input whose final state corresponds with the output.

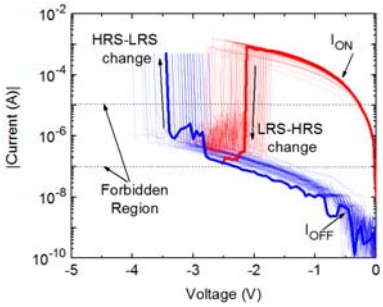


Fig. 2: Typical I-V curves of the memristors. I_{ON} and I_{OFF} currents, which for simplicity in this work are used to define the logic states, are also indicated.

a logic function whose operations are: "p implies q" or "if p then q" as it is shown in the IMPLY truth table in Fig. 1(b).

Interest thing of IMPLY gate is that by applying the same operational voltages to perform all the four gate case, the truth table shown in Fig. 1(b) is accomplished independently if a memristor state change is needed (case 1) or if not (case 2, 3 or 4). A more detailed circuital analysis of the IMPLY gate can be found in [12].

III. Samples and Measurement Procedure

Memristors used in this work are Ni/HfO_2/Si(n^+) devices with 5x5 μm^2 area [18]. These devices show better performance operating as negative unipolar RS devices [18], [19], i.e. applying negative voltages to provoke the change between both memristor resistance states. Fig. 2 shows typical I-V curves of such memristors. Apart from HRS to LRS (set) and LRS to HRS (reset) changes, I_{ON} and I_{OFF} corresponding to the current states at these resistance states are also indicated. As in voltage-based logic, current ranges are stablished for both I_{ON} and I_{OFF} in which logic states ("0" and "1") are valid. In this work, current values of I_{OFF} below 0.1 µA are considered as "0" logic state. On the other hand, current values of I_{ON} above 10 µA correspond to "1" logic state. This threshold values allow a forbidden region of 2 decades (region in between black dashed lines in Fig. 2).

Characterization studies of the HfO_2-based memristors have been performed in [7], [18] and [19]. In [18] and [19] the cycle-to-cycle variability of I_{ON} and I_{OFF} is analyzed. From the same works, a memristor endurance of thousands of cycles is also observed. Voltage variability has been analyzed from the 500-cycle measurement shown in Fig. 2. Extracted results for V_{SET} and V_{RESET} are averages of -3.26 V and -2.27 V and a sigma of 0.46 V and 0.48 V, respectively. On the other hand, in [7], an analysis of the energy necessary to trigger the RS processes is performed suggesting a critical energy of the order of pJ and µJ for the set and reset processes, respectively. Although these memristor features do not seem the most promising for their application in logic computing, they have allowed performing an initial analysis of the time evolution during gate operation.

The measurement procedure to study the time evolution of memristor for each case of the IMPLY gate consists, firstly, in the initialization of memristors to the corresponding input states (Fig.1(b)). The initial memristors states were verified measuring the current through the memristors at -0.5 V. Once input states were fixed, and slow voltage ramps were applied simultaneously to the top electrode of both memristors, P and Q, until a maximum value of V_P and V_Q respectively, and the currents through the memristors were registered. Semitriangular pulses have been applied to register the whole memristor behavior. As it is shown later, rectangular pulses as those used in transient studies [20] were also applied to demonstrate the same qualitative results than those obtained from semitriangular ones. Measurements with semitriangular pulses were performed with the semiconductor parameter analyzer (SPA) Agilent 4156C which allows registering both the programed and the actual voltages applied to memristors, which can be different when a current limit, I_C, (in this work I_C was 50 µA and, if not indicated, was supplied by the SPA compliance) is reached, as it will be shown later, provoking also differences in the current through the memristors. Although other current limiting methods can be found in the literature, (for example those based on transistors [21]), in this work, for simplicity, the current limit was supplied by the SPA compliance. For a correct IMPLY gate performance, V_Q must be higher than V_P [12]. On the other hand, after several attempts, the final values of V_P and V_Q voltages ramps, which allow performing all the IMPLY cases were found to be -2 V and -4 V, respectively. The time duration, indirectly measured, of both ramps were exactly the same in each gate case. So that, applied voltage ramps to P and Q were defined from 0 V to -2 V and -4 V respectively, in all IMPLY cases. V_G was also registered with the SPA, and the voltage drops through memristor P (V_P-V_G) and Q (V_Q-V_G) were evaluated. Finally, after the previous voltage ramps application, the final states of the memristors were verified again measuring the current through the memristors at -0.5V in all the cases. In all section IV, the value of R_G is 33 kΩ, except when we indicate other value. Note that the maximum current established in the SPA (50 µA) is smaller than the maximum current allowed by R_G at the maximum voltage (-4V), so that the current limitation is independent of R_G. The impact of R_G on the IMPLY operation is analyzed in detail in section V.

IV. Memristors Operation in an Imply Gate

In this section, temporal evolution of memristor behaviors (for simplicity, in terms of current) is evaluated for each IMPLY case.

A. *Case 1*

In this case, both memristors must be initialized to "0" logic state (I_{OFF} < 0.1 μA). Once initialized, applying the corresponding voltage ramps to the memristors, Q should change from "0" to "1" logic state and P should keep the same state, "0", as indicated. This means that the memristor Q should change its resistance to lower values, allowing large current values, which must be larger than 10 μA, as defined previously. Fig. 3 (a), where memristors current evolutions are depicted, shows the Q-state transition, in terms of current, which takes place as an abrupt increase (in absolute value) of the current flowing through memristor Q up to the stablished current limit value (50 μA). At the same time, memristor P barely suffers current variations, keeping its initial logic state. Initially, P is at "0" (current < 0.1 μA) and the applied voltage ramp during operation is not large enough to provoke any change on its current, which remains in the range of nA. Both final memristor logic states were measured at -0.5V to be in agreement with Fig. 1(b). In Fig. 3(b), the actual voltage drops across both memristors are depicted in order to show the bias behavior and the explained right before.

In order to know in more detail where memristors voltage drops come from, in Fig. 3(c) the actual voltage ramps applied by the semiconductor parameter analyzer to memristors P and Q (solid blue and dashed red lines, respectively); the programmed voltage ramps (open blue squares and open red circles respectively) and V_G (solid black circles) are depicted along the time. Note that a difference between the actual and programmed voltages is observed for Q due to the memristor current reaches the current limit value. At that moment, the analyzer keeps the current through the memristor at the current limit value by reducing the applied voltage whereas the programmed voltage remains increasing up to the maximum.

Before Q reaches the current limit value, V_G is approximately zero, so that voltage drops at memristors are equal to the applied voltages. Once the Q state change takes place, V_G follows V_Q, which is constant, to maintain the current limit level at Q. Since Q is at "1" its resistance value is

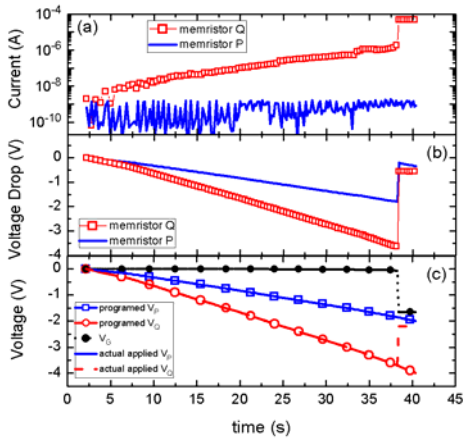


Fig. 3. For case 1: (a) Memristor current evolutions as a function of time (b) Voltage drops across P (solid blue line) and Q (red squares) memristors. (c) Actual voltages applied to P and Q top electrodes (solid blue and dashed red lines respectively), V_G (solid black circles) and programmed voltages of P and Q (open blue squares and open red circles respectively) as a function of time.

really small and current flow is allowed (I_{ON}). On the contrary, since P is at "0" its resistance is so large that almost no current can flow (I_{OFF}). This scenario provokes all the current from Q flows through R_G. Therefore, the IMPLY circuit shown in Fig. 1(a) becomes a voltage divider between the memristor Q and R_G, what makes V_G proportional to V_Q. At this point, P voltage drop is smaller than previously to the change of Q state, and therefore, current through P is still at low levels.

Additionally, to check if the duration of the voltage ramps applied to the memristor could have significant influence in the qualitative results, shorter ramp voltages were applied to each memristor using a pulse generator instead of the SPA. These applied voltages (V_P and V_Q) as well as the voltage drop across R_G (V_G) were registered with an oscilloscope. Since the pulse generator cannot apply a current limit during the set process, an adequate value of R_G (1 MΩ) was chosen to act also as current limiter. Fig. 4(a) shows the time evolution of the voltages V_P, V_Q and V_G (see Fig. 1(a)) registered for a ramp duration of 10μs. In addition, square pulses of 2μs-width (Fig. 4(b)) were applied to each memristor in order to check the gate working under conditions similar to those in commercial systems. In general, for these shorter timescales, the voltages behavior is similar as that shown in Fig. 3(c). When the memristor Q changes its state, V_G changes abruptly from zero to almost the voltage applied to that memristor (V_Q), now, most of the applied voltage drops across R_G. Note that a V_Q decay is not observed because the current limit is not applied by the SPA like in the case of Fig. 3(c). Some slight parasitic capacitance effects are observed in the time evolution of V_G, likely due to the faster ramps applied. Since no significant differences are observed in the time behavior, the study of shorter timescales influence is only included for case 1. Larger timescales and voltage ramps will be used in the following because of the simplicity of the required experimental setup and the ease of registering the whole current time evolution of memristors which is not possible of registering under pulsed conditions.

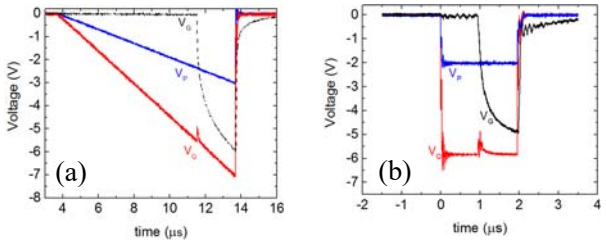


Fig. 4. Registered voltages V_P, V_Q and V_G as a function of time when (a) semitriangular and (b) square waveforms are applied to P and Q.

B. *Case 2*

For the second IMPLY case, initialization states must be "0" (current < 0.1 μA) for memristor P and "1" (current > 10 μA) for memristor Q. As for the case 1, the time evolution of the current through the Q (red square symbols) and P (blue solid line) memristors are experimentally registered, Fig. 5(a). In this case, memristor Q state should not change and, therefore, an abrupt change in Q current is not observed. Meanwhile, memristor P, which also must keep its state, maintains low current levels in the range of nA (Fig. 5(a)) as in case 1. Memristors current behaviors are

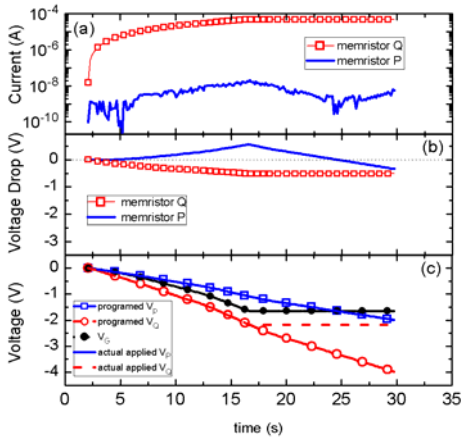


Fig 5. For case 2: (a) Memristor current evolutions as a function of time (b) Voltage drops across P (solid blue line) and Q (red squares) memristors. (c) Actual voltages applied to P (continuous blue line) and Q (dashed red line) top electrodes, V_G (solid black circles) and programmed voltages of P (open blue squares) and Q (open red circles) memristors depicted as a function of time.

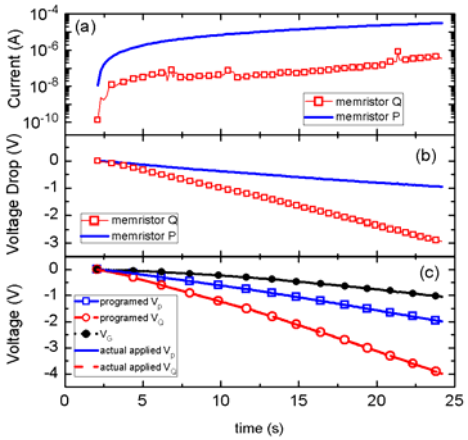


Fig. 6. For case 3: (a) Memristor current evolutions as a function of time (b) Voltage drops across memristors. (c) Actual voltages applied to P and Q top electrodes (continuous blue and dashed red lines respectively), V_G (solid black circles) and programmed voltages of P and Q (open blue squares and open red circles) depicted as a function of time. As I_C is not reached, applied and programmed voltages completely overlap.

justified taking into account the voltage drops depicted Fig. 5(b). Initially, voltage drop across memristor Q is too low to reach the defined I_C, so its current increases following Ohm's law, until I_C is reached. For P, its voltage drop remains at low levels avoiding undesirable memristor state change. In order to confirm that both memristors accomplish IMPLY case, final current states were also measured at -0.5 V.

In Fig. 5(c), actual applied voltage to P and Q (continuous blue and dashed red lines), programmed voltages (open blue squares and open red circles) and V_G (solid black circles) are depicted. Here, the difference between applied and programmed voltages in memristor Q is more appreciable. I_C is reached sooner (after ~ 15 seconds) than in case 1 and the SPA keeps V_Q constant at approximately -2.3 V in order to control the current flowing through Q memristor. Once I_C is reached in case 2, memristor Q behavior is similar to what occurs after the abrupt current change of Q current in case 1, that is, V_G follows V_Q behavior again. Note that, for a time around 25 s, V_G surpasses V_P, changing the polarity of P memristor voltage drop (solid blue line in Fig. 5(b)), which is due to the current limitation of 50 µA. As this voltage drop is kept always low, independently of the polarity, absolute value of P current value is below 0.1 µA all the time, in spite of changing its flow direction.

C. *Case 3*

Case 3 is similar to case 2, with the only difference of the initial states of memristor P and Q, i.e. "0" for "Q" and "1" for P. Current evolution, as voltage ramps are applied, are shown in Fig. 6(a) for Q (red squares) and P (solid blue line) memristors. Current flowing through Q is always low (< 0.1 µA) indicating Q is at "0" state all the time. On the contrary, P current increases up to high current levels, close to I_C, keeping P at "1" state. In this case, the maximum value of V_P is -2 V and, taking into account the final resistance value of P, which was approximately 50 kΩ, the maximum voltage drop across P (blue solid line in Fig. 6(b)) is not enough to reach I_C ($|I_{PMAX}|$ = 40 µA). On the hand, the value of V_Q equal -4 V might provoke the change of Q, however, the voltage drop across this memristor (red squares in Fig. 6(b)) is not sufficient to do that. At maximum values V_Q-V_G = -3 V, however since the resistance value of Q was higher enough (~ 5 MΩ), the current is kept at low levels (I_{QMAX}=0.47 µA) maintaining Q at "0" state. In spite of these facts, Q and P memristors reached the correct final states.

Likewise in case 2, Fig 6(c) shows the actual applied voltages to P and Q (continuous blue and dashed red lines), programmed voltage ramps (open blue squares and open red circles) and V_G (dashed line plus solid black circles). Now, since resistance value of Q is much larger than that of P, the voltage divider occurs between memristor P and R_G and therefore, V_G behavior resembles that of V_P. No voltage restriction applied by the SPA is observed due to the I_C value is not reached by P.

D. *Case 4*

Finally, for case 4 where Q and P initial states are both "1", the time evolutions are addressed in Fig. 7. As in cases 2 and 3, memristors state changes are not expected. In Fig. 7(a), the currents through memristors Q (red squares) and P (solid blue line) are represented as a function of time when the voltage ramps are applied. For memristor Q, current evolution is similar to that observed in case 2 for the same memristor, increasing with voltage up to the current limit stablished by the SPA. For the current through P, two unexpected behaviors can be observed. First, current never reaches the expected current limit level and second that current changes its direction twice.

Previous behaviors can be explained by the voltage drops across memristors depicted in Fig. 7(b) and the programmed and actual voltages applied to Q and P. When current through Q reaches I_C, the SPA reduces the increasing speed of V_Q (dashed red line in Fig 7(c)) to control the current flowing through this memristor. On the contrary, P does not reach the I_C value, maybe due to the low voltage drop across it (solid blue line in Fig. 7(b)) which was not sufficient to reach that current value. Direction changes of P current are owing to the polarity changes observed in the voltage drops across P (blue

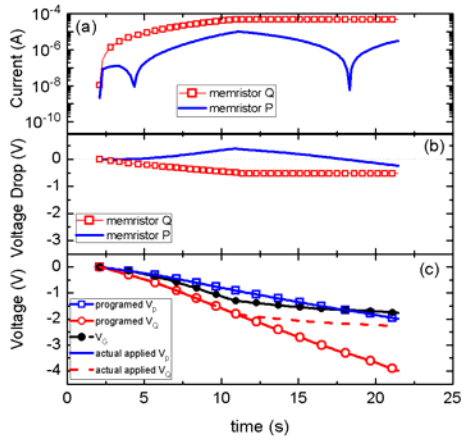


Fig. 7. For case 4: (a) Memristor current evolutions as a function of time (b) Voltage drops across memristors Q and P. (c) Actual voltages applied to P and Q top electrodes (continuous blue and dashed red lines respectively), V_G (solid black circles) and programmed voltages of P and Q (open blue squares and open red circles) as a function of time..

solid line in Fig. 7(b)). At the same time, this polarity changes are due to V_G (solid black circles in Fig. 7(c)) surpasses V_P (solid blue line in Fig. 7(c)) at around 5 and 17 seconds. This is directly related with the evolution of V_G in Fig. 7(c) which follows V_Q behavior (dashed red line in Fig. 7(c)) once Q current reaches I_C (around 11 seconds) and the analyzer adjusts V_Q to keep that constant maximum current value. Note that, in this case, after I_C is reached, V_Q (and therefore V_G), is not maintained completely constant but it goes on increasing, with an appreciable slope. This might be due to the influence of V_P, which also increases, varying V_G value and, consequently, V_Q too. Therefore, in this case, no voltage divider behavior is observed, as in the previous ones. In spite of all of that, both memristor Q and P keep their state at "1".

V. R_G IMPACT ON IMPLY OPERATION

R_G is also an important parameter in the performance of IMPLY gate [22]-[25]. In the literature, R_G is mainly defined as a resistor whose value must be larger than the resistance at LRS and smaller than at HRS [13]. However, such resistor may influence the performance of the gate operation, especially on reaching the selected or desired current limit. This effect is mainly observed in cases 2 and 3 of the IMPLY gate since the current which flows through the circuit is flowing through R_G. Depending obviously on the LRS and HRS resistance values, the effect can be remarkable for relatively high current limits. In the following, a study of mentioned effect is presented for a high current limit (300 µA provided by the SPA compliance) and different values of R_G with the memristors shown in previous sections whose LRS and HRS resistances were approximately 10 kΩ and 50 MΩ.

As above mentioned, scenarios in cases 2, 3 and 1 (when Q reaches current limit) is slightly different from that in case 4 because at least one of the memristors is at "0" (HRS). Because the resistance value at HRS is really high, current barely flows through that branch in the equivalent circuit of IMPLY gate (Fig. 8(a)). Therefore, the equivalent circuit may be considered as a voltage divider between the branches of the memristor at "1" (LRS) and the resistor R_G (Fig. 8(b)).

Thus, current flowing along divider branch is the same for both elements. Depending on the voltage applied to memristor through which the current is flowing and imposed current limit, R_G might act as current limiter (due to Ohm's law) instead of the semiconductor parameter analyzer used in the setup.

As an example of this effect, Fig. 9 shows currents through memristors P and Q (I_P and I_Q respectively) in case 2, in which memristor P is at "0" and Q at "1", for different values of R_G (1 kΩ, 33 kΩ, 155 kΩ 566 kΩ and 956 kΩ). Voltage ramps have been applied to memristors Q and P changing from 0 V to -4 V and -2 V, respectively. The current limit value has been stablished at a high value, 300 µA, to make more remarkable the R_G effect as a current limiter. The different chosen values of R_G accomplish HRS > R_G > LRS condition with the exception of 1 kΩ included in order to observe the current limit applied by the SPA. In Fig. 9, it can be observed that the larger R_G, the smaller the current flowing through Q. When R_G is 1 kΩ, current through such a resistor is larger than the selected current limit (as long as the voltage applied is large enough), therefore, when current limit is reached, SPA is acting as the current limiter, what can be identified by the flat part of the curve. However, as R_G increases the current through the resistor is smaller than the current limit, since the applied voltage, and therefore the voltage drop across the resistor, is not enough to reach the current limit values. In all those last cases, R_G is acting as a current limiter element.

This is corroborated in Fig. 10 where voltages drops across memristor Q (continuous red line) and R_G (dashed black line) are depicted for three representative values of R_G ((a) 1 kΩ, (b) 33 kΩ and (c) 566 kΩ). For the smallest value of R_G (1 kΩ), the voltage drop across R_G (black dashed line in Fig. 10(a)) is almost negligible and barely affects the current conduction through Q while voltage drops across the memristor (continuous red line in Fig. 10(a)) increases up to a certain value where memristor Q has reached the current limit and SPA controls applied voltage. On the contrary, as R_G increases, its voltage drop also increases what provokes a Q voltage drop decrease. Consequently, the current through R_G, and hence through Q, is controlled by Ohm's law on R_G. For example, if R_G = 33 kΩ and taking the maximum value of the applied voltage ramp (-4 V), according to Ohm's law, a current of 121 µA should flow, which is smaller than the current limit of 300 µA. Obviously, as R_G increases, the current flowing through the divider branch decreases since the applied voltage is always in the 0 V to -4 V range.

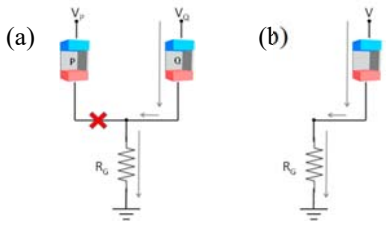


Fig. 8. Equivalent IMPLY circuit when one of the memristor is at "0" state, and therefore, its resistance is very large in comparison to R_G and that of the other memristor.

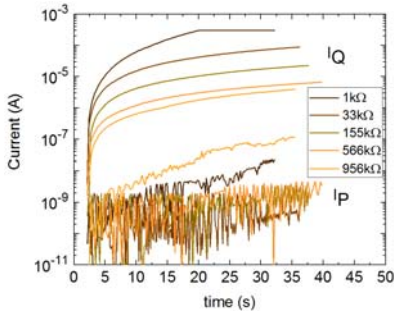


Fig. 9. Currents through P and Q memristors for different values of R_G (1 kΩ, 33 kΩ, 155 kΩ, 566 kΩ, 960 kΩ). As the value of R_G increases, the current limit is imposed by the resistor instead of SPA.

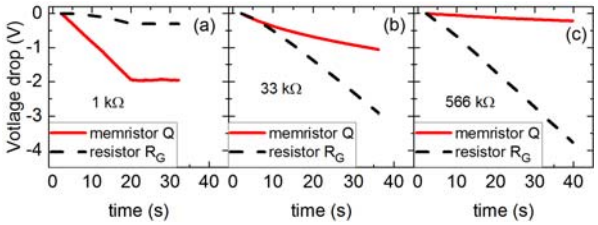


Fig. 10. Voltage drops across Q memristor and R_G in case 2 for different values of R_G, (a) 1kΩ, (b) 33kΩ and (c) 566kΩ). As R_G increases, voltage drop through R_G also increases until almost reaching the values of the voltage applied to memristor Q.

VI. Conclusion

In this work, a detailed study of the electrical time evolution of the two memristors involved in an IMPLY gate is performed for each IMPLY input-output case. The evolution of the memristors currents and the memristors voltage drops along time during each phase have been analyzed, observing in some cases, polarity changes of the memristors voltage drops. Finally, the impact of the internal resistor (R_G) in series with the memristors of the IMPLY gate has been analyzed. The results show that R_G can be also used to limit the current through the memristors at LRS.

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