Characterization of HfO$_2$-based devices with indication of second order memristor effects

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Abstract

Resistive switching is investigated in TiN/Ti/HfO$_2$(10nm)/TiN devices in series with a NMOS transistor as selector in a 1T1R configuration. A complete electrical characterization of the devices is carried out using DC voltage loops, constant-voltage stressed and pulses with varying voltage amplitude and time width. Good control of the ON resistance is achieved by applying different transistor gate voltages and multiple OFF states are controllably reached by varying the maximum reset voltage. The on/off resistance ratio is successfully controlled by changing the pulse amplitude and time duration. However, significant memory effects are reported, showing that the switching of a device depends on its switching history. Exploring the on/off ratio for different set and reset voltage amplitudes in otherwise identical set/reset pulse experiments is shown to depend on the order of application of the different stress conditions so that the on/off resistance map in the V_{SET}/V_{RESET} space is not unique. We interpret these results as an evidence of second-order memristive effects.

1. Introduction

In the last 15 years novel device technologies have emerged with the aim of replacing or complementing charge-based memories which have an intrinsic scaling issue due to the inability to keep charge within extremely thin barriers [1]. Devices such as random resistive switching memory (RRAM) [2], phase change memory (PCM) [3], and spin-transfer torque memories (STTRAM) [4] have emerged, each of them presenting advantages in terms of scaling and speed. All these memories share the fact that the resistance is used as a probed state variable. The resistance can be changed by application of electrical signals and, in RRAM, the most common situation is that the resistance changes following the state of a conductive filament (CF) created during electro forming within the insulating oxide layer. Since these are very simple two-terminal devices, they can be disposed in a crossbar array, which can be fabricated in the back-end of the line of CMOS processes. This leads to an extremely small bit area of only $4F^2$, where F is the minimum feature size accessible by lithography [5]. Another main advantage of RRAM is that, having short switching times, combined with relatively low-voltage operation, they are suitable for low-power applications. For all these reasons, resistive memories are very promising not only for nonvolatile memories, but also for computing memories, allowing fast data access to overcome the von Neumann bottleneck [6], and in particular for neuromorphic networks [7]. With respect to other candidate devices, RRAM has a good cycling endurance [8], moderately high speed [9], an extremely simple structure (only an insulator between two metal layers), ease of fabrication and good scaling behavior.

In this work, resistive switching is investigated in Ti/HfO$_2$(10nm)/TiN RRAM devices fabricated at LETI with a NMOS transistor as selector in a 1T1R configuration. These structures are ideal for embedded non-volatile memory applications because the

transistor allows to limit endurance issues due to excessive currents, and allows an easy reading without the sneak-path problem. Here we present a full characterization of the performance of these devices using different electrical characterization signals. Voltage Sweep Mode (VSM) experiments are performed to explore the effects of transistor current compliance limit during set (this allows to reach different values of ON resistance), to demonstrate the possibility of controlling several resistance states (multi-state memory) by changing the maximum voltage applied during reset (this allows controlling the OFF resistance within two orders of magnitude) and to study the influence of ramp rate during set and reset. By means of these ramp-rate experiments, information is extracted about the strongly non-linear time-voltage relationship. Pulsed experiments are also performed in a range of ~1V in voltage amplitude and three orders of magnitude in time pulse width (from 100ns to 100µs). It is demonstrated that the R_{OFF}/R_{ON} ratio can be controlled by changing the reset pulse characteristics and that the pulse characteristics have a significant impact on endurance. A maximum endurance of 10^8 is demonstrated. Finally, some experimental indications of the appearance of second-order memristor effects are presented. Second order effects might be very useful for neuromorphics applications [10,11] but might have also an impact on RRAM performance. These second-order effects are intrinsic to the switching mechanisms and a detailed understanding is required for proper device characterization.

2. Experimental details

The samples investigated in this work are 1T1R devices fabricated at LETI (CEA). The MIM structure, sketched in Fig. 1 (a), is formed by a 10 nm-thick ALD HfO_2 layer sandwiched between two metal electrodes (Ti and TiN). To prevent irreversible cell breakdown and to control the low resistance state (LRS), an NMOS transistor

(W/L=5μs/0.35μm) is used in series with the ReRAM device, embedding a 1T1R structure. The transistor does not play any role for the high resistance state (HRS). To activate the adequate switching property a forming step with gate voltage of 1.3 V is required. Quasi-static measurements were performed using the Keithley 4200-SCS semiconductor parameter analyzer equipped with a 4225-RPM PGU (pulse generator unit). Typical *I-V* characteristics for the 1T1R configuration after the forming process are shown in Fig. 1 (b) and Fig. 1 (c) for log-linear and linear-linear representation, respectively, where fifty cycles (gray solid line) were performed with a ramp rate (RR) of 50 Vs^{-1}. The heavy solid line represents the median curve of these cycles (blue solid line). As it can be seen, the devices exhibit bipolar switching with abrupt set and gradual reset transitions. It should be noted that V_{SET} and V_{RESET} are lower than 0.8 V, which suggests that the devices investigated here are suitable for low voltage applications [12]. Notice also the transistor action for positive bias $V > 0.75$ V. The limit imposed by the transistor saturation current allows controlling the damage caused to the ReRAM during the set process.

3. Data analysis and discussion

Figure 2. (a) illustrates the control of the set by the transistor gate voltage. The current compliance level (I_C) is adjusted by setting the transistor gate voltage from 1.2 V to 1.6 V in steps of 0.1 V for set and 4 V for reset condition in any case, being their corresponding I_C levels 140 μA, 240 μA, 352 μA, 470 μA, 600 μA for the set gate conditions and 3.5 mA for the reset gate conditions. Note that since the reset process is thermally activated, the reset gate voltage must be high enough to allow reaching the desired reset current level [13–15]. Notice also the ability to control the compliance current, as well as R_{ON} and I_{RESET}. Figure 2. (b) shows measured reset current as a

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function of I_C. Reset current scales linearly with I_C, since reset voltage controls the temperature and it has a dependence on the CF size formed during the compliance [1,16]. In addition, Figure 3 shows how the maximum reset voltage controls R_{OFF}. In this case, cycles were performed varying the maximum reset voltage (0.8 V, 1.0 V or 1.2 V). Moreover, the LRS value is independent of the maximum reset voltage. These observations agree with recent published works such as [12,17,18]. Both procedures shown in Fig. 2 and 3 can control multiple resistance states. Therefore, it can be asserted that the structures are worthy of low current multilevel RRAM application under modulation of reset voltages.

The devices were also characterized under Constant Voltage Stress (CVS) conditions. Since the set consists in the breakdown of the thin insulator remaining between two CF stumps after the reset, time to set can be identified as the time to breakdown (t_{BD}). These experiments consist in a typical CVS experiment for the set process (positive bias), and a ramp voltage stress for the reset process (negative bias). The experiment consists in 100 cycles performed for each CVS condition (V_{CVS}=0.45 0.50, 0.55, 0.60, and 0.65V). The results of t_{BD} as a function of stress voltage are shown in Figure 4(a). As it can be noticed, an increase of 50 mV in the CVS condition translates into a decrease of an order of magnitude in t_{BD}. On the other hand, if the samples are stressed with a typical VSM experiment for different ramp rates (RR), similar information can be extracted, as shown in Fig. 4(b). I-V-t data were obtained using pulsed measurements with pulse widths ranging from 1 µs to 1 ms, which in combination with a ramp step voltage of 50 mV, yields RR values ranging from 5·104 Vs^{-1} to 50 Vs^{-1}, respectively. V_{SET} and V_{RESET} follow the same logarithmic dependence with RR [19], as it can be seen in Fig. 4 (b). This results are in close agreement with the results reported in [20–23]. Both set of experiments reveal the same trend of one-time decade per 50 mV.

Resistance ratio can be adjusted during pulse measurements by changing pulse amplitude and pulse time duration, as it is demonstrated in Fig. 5. In this case, keeping the set conditions fixed at 1.5 V pulse amplitude and 5µs time width, we vary the reset pulse width time from 100 ns to 100 µs for three different reset pulse amplitudes of 1 V, 1.5 V and 2 V. Each point with it error bars corresponds to the statistics of 200 identical stress cycles. The measurements were performed in one device. The voltage pulse amplitude affects more significantly the R_{OFF}/R_{ON} ratio that the pulse time width even if voltage is only changed in ~1 V while the time width changes by three orders of magnitude. Note that the R_{ON} value is independent of the reset pulse amplitude which is due to the transistor effect. Figure 6 shows the CDF of R_{OFF} for the same data shown in Figure 5 and shows the same variability in each particular case. This is due to the highly non-linear time-voltage dependence. Note that this kind of extremely non-linear dependence is a requirement for the successful application of RRAM because of the set-speed/read-disturb trade-off. In these experiments, the on/off ratio is increased by increasing pulse height or width, i.e. by increasing the reset stress and the off-resistance. However, there is a trade-off between high resistance ratio and endurance. The best conditions for high endurance are obtained for a relatively small pulse amplitude. Fig. 7 demonstrates more than 100 Mcycles for V_{pulse}=1.25 V and $t_{RESET} = t_{SET} = 10$ µs.

RRAM devices are memristors [24], i.e. two-terminal electrical devices whose states are described by internal state variables and which are governed by dynamic ionic processes that finally determine and control the electrical conduction properties of the device. Usually, when described mathematically, RRAM devices have been treated as first-order memristors, i.e as having only one internal state variable, namely the device resistance, R. Mathematically, a first-order memristor can be described by

$$\frac{dR}{dt} = f(R, V, t) \tag{1}$$

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However, internal switching mechanisms are usually not that simple, and more variables can play a significant role during switching so that a higher-order description might be necessary. In particular, it has been recently shown that temperature T or another variable related to the ionic conductivity in the CF might play a significant role [10,11]. Whenever two variables have significant relevance to determine the internal state of the device, a second-order memristor model is required which is mathematically described as

$$\frac{dR}{dt} = f(R,T,V,t) \tag{2}$$

where T represents the second internal variable which can be the temperature or another variable. Second order memristor effects have been recently shown to allow biorealistic emulation of synaptic functions which can be very useful in neuromorphic circuits showing not only long-term memory but also short-term plasticity [10,11].

In the characterization of our RRAM devices, we have found some experimental results which suggest the occurrence of second-order memristive effects. Fig. 8 shows the results of pulsed experiments in which the voltage pulse amplitude is the same for set and reset ($V_{SET}=V_{RESET}$) and we explore how R_{OFF}/R_{ON} depends on pulse amplitude and time width. In this experiment, the pulse voltage is monotonously increased from 0.75 to 2.25 V and, for each voltage, the pulse width is increased from 100ns to 10µs and 200 pulses are applied for each stress condition (to obtain a distribution of results for each represented data point). The results are shown in Fig. 8 and it follows that, consistently with what reported in Fig. 5 and 6, off-resistance and on-off ratio increases with both voltage and pulse width. However, when, at the end of the stress, after applying the most severe reset conditions and reaching a maximum ratio $R_{OFF}/R_{ON} \sim 10^2$, the pulse voltage sequence is repeated for a lower pulse amplitude of

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1.25V (in the same time-width space) we find that the results are significantly different (almost one order of magnitude) from what previously found in the same experiment. This is an indication of a dependence of the device performance on its switching history. This indicates that the overall shape of the CF or the ionic mobility or the local stress or any, for the time being unknown, property shows long-term changes which depend on how the device has been stressed and which somehow determine its ulterior switching behaviour. This is a clear case of second-order memristor effects [10,11]. In this particular case, we can in principle discard the temperature as the second state variable because the time scales of our experiments are much longer than expected for heat dissipation [10]. Further investigation is required to unveil the details of high-order memristive effects in these devices but some other results further confirm our conclusions. Figure 9 shows a colour diagram of the resistance ratio (in logarithmic scale) in a V_{SET} vs. V_{RESET} plane. The experiment consisted in the application of pulses with $t_{SET}=t_{RESET}=10$ μs and varying V_{SET} and V_{RESET}. In Fig. 9 (a) V_{RESET} is swept from 0.75V to 2V for each constant value of V_{SET} beginning with the smallest value of V_{SET} and increasing its value after each reset voltage sweep. Alternatively, in Fig. 9 (b) V_{SET} is swept from 0.75V to 2V for each constant value of V_{RESET}. Although one would expect to find the same results for each pair of V_{SET} and V_{RESET} independently of the order that these two variables are changed, the fact is that significant differences are found between the two-colour maps. This provides an independent indication of the fact that switching depends on the previous switching history so that the system cannot be modelled as a first-order memristor. Again, these second-order effects are not likely related to local temperature changes in the CF because heat dissipation is expected to occur in a time scale much shorter than that of the times involved in the experiment. A final experiment consisted in the application of a train of pulses with increasing voltage

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and constant pulse width but with a variable delay time between them (see inset of Fig. 10 for signal definition). For a first-order memristor, one would expect that changing the delay time would not have any significant effect on the results since only a small voltage is applied to measure the state of the device after each stress pulse. Nevertheless, as shown in Figure 10, decreasing the delay time between pulses accelerates the set transition, and this is exactly what would expect for a second-order memristor. When there is a second variable affecting the internal state of the device, the separation of successive pulses is relevant because the application of one pulse leaves the device in a situation in which it is more prone to potentiation (conductance increase) or depression (conductance decrease) when the following pulse arrives. Since the effects of the second state variable, T in equation 2, usually decay in a shorter time scale and do not cause permanent long-term changes in the memristor internal state, if the separation between successive pulses is long enough, second-order memristor effects are expected to be negligible for long delay times. This is exactly what is found in Fig. 10, in the which the results obtained for the longer values of delay time (100 µs and 1 ms) almost fully coincide while a shift to lower reset voltages and a deeper change of device conductance is progressively found when the delay time is shortened (10 µs and 1 µs). This is another piece of evidence to support the existence of second-order memristor effects in the RRAM devices studied in this work.

5. Conclusions

We have electrically characterized ReRAM devices with a Ti/HfO$_2$(10nm)/TiN structure in a 1T1R configuration. We have demonstrated the strongly non-linear relation (~50 mV per time decade) between voltage and set switching time using voltage ramps and constant-voltage experiments. We have checked the efficiency of the

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transistor in controlling the maximum current during set and the on-resistance. Multiple resistance states are accomplished by varying the maximum reset voltage in VSM experiments. Pulse-based experiments have demonstrated that it is possible to change the on-off resistance ratio by changing pulse width and, more efficiently, the pulse voltage amplitude. However, a set of three different kinds of experiments revealed the existence of second-order memristor effects. This means that there is a second internal state variable that cannot be ignored during device operation or characterization. These effects can be very useful for the operation of these devices in neuromorphic circuits and cannot be ignored when operating the devices as non-volatile resistive memories or for their electrical characterization. Although determining the nature of this second state variable requires a deeper study, we speculate that the stress history determines the geometry of the CF which in turn changes the switching properties in second order.

Acknowledgements

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Figure captions

1. (a) Cross-section of the fabricated stack. I-V characteristics for quasi-static sweeps (RR = 50Vs^{-1}), 50 curves (light solid lines) and its median (heavy solid line) in (b) semi-log representation, (c) linear representation.

2. (a) The measured I-V characteristics for a HfO$_2$ RRAM device at a variable compliance current I$_C$ ranging from 1.2 to 1.6 V. Inset: Scheme of the measurement set-up. (b) Measured reset current as a function of I$_C$.

3. I-V characteristics show the control of R$_{OFF}$ by maximum reset voltage.

4. (a) Exponential voltage dependence of set (breakdown) time on CVS experiments. Each point represents 100 cycles. (b) Experimental data and trend line for set and reset voltage as a function of RR ranging from 50Vs^{-1} to 50 KVs^{-1}.

5. R$_{OFF}$ and R$_{ON}$ in single pulse experiments with different reset pulse amplitude, V$_{RESET}$=1 V, V$_{RESET}$=1.5 V and V$_{RESET}$=2 V (from left to right), and t$_{RESET}$ changing from 100 ns to 100μs. Set pulse kept constant (V$_{SET}$ =1.5 V t$_{SET}$=5 μs).

6. Cumulative distribution functions (CDF) of R$_{OFF}$ for the collected data in Figure 5.

7. Statistics for the endurance characteristic of the 1T1R device. The resistance ratios of HRS to LRS are more than 10 during the 100M cycles of fatigue test.

8. R$_{OFF}$ and R$_{ON}$ in pulsed (V$_{SET}$=V$_{RESET}$) experiments with voltage ranges from 0.75 to 2.25V. Reset time sweeps from 100 ns to 10μs in all the cases. 200 pulses per experiment. Notice that behaviour at 1.25V after applying higher voltages yields different results than after low voltages.

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9. Resistance ratio $(\text{Log}(R_{OFF}/R_{ON}))$ in pulsed experiments with $t_{SET}=t_{RESET}=10\mu s$ and varying V_{SET} and V_{RESET}. (a) In experiment V_{RESET} is swept from 0.75V to 2V for each constant value of V_{SET}. Alternatively, (b) experiment V_{SET} is swept from 0.75V to 2V for each constant value of V_{RESET}.

10. I-V characteristics keeping the pulse width time fixed to $1\mu s$, and ranging the pulse delay time from $1\mu s$ to 1ms. $V_G=1.2$ V.
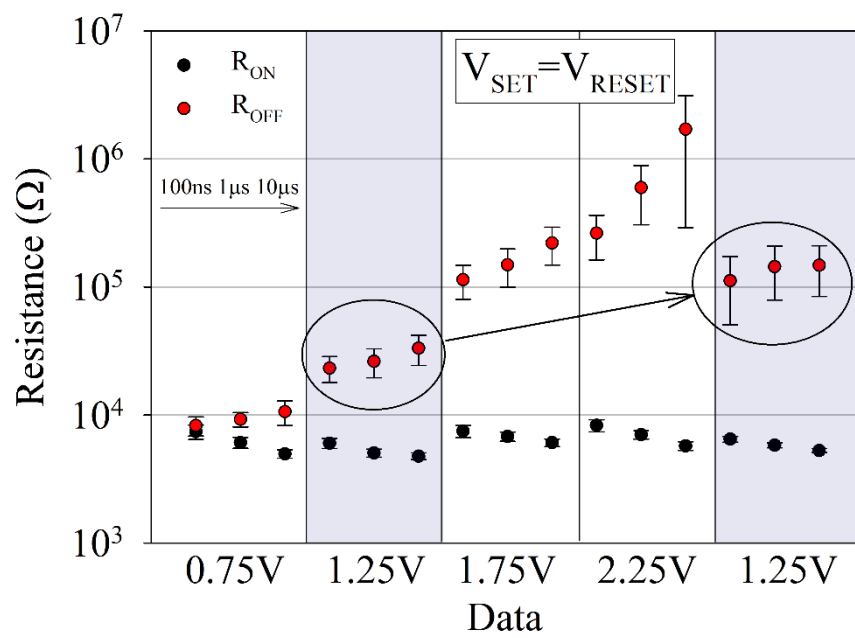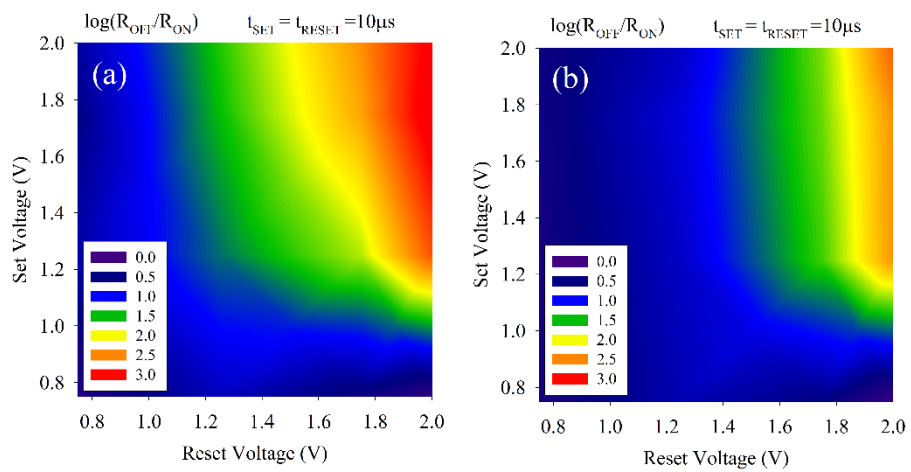
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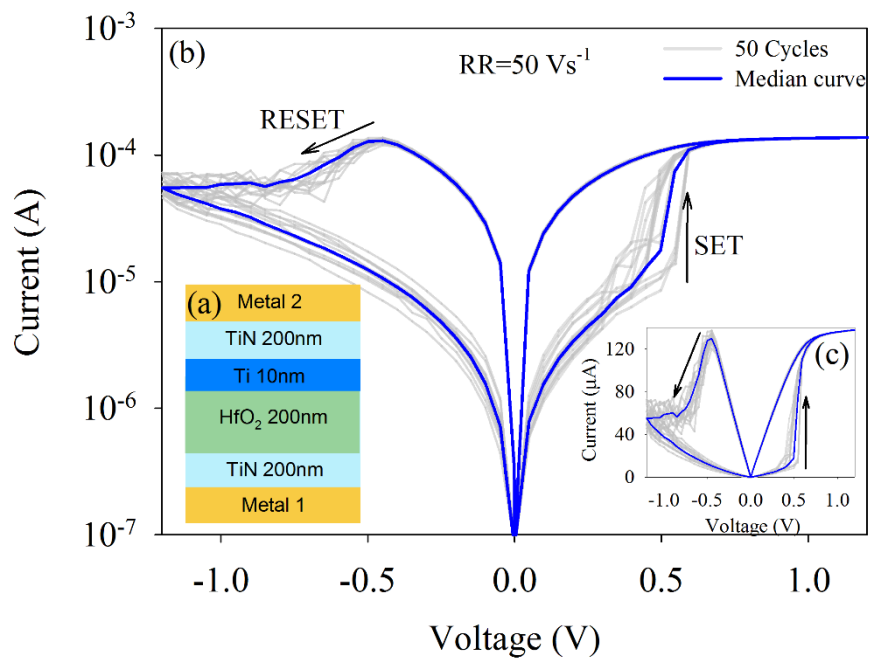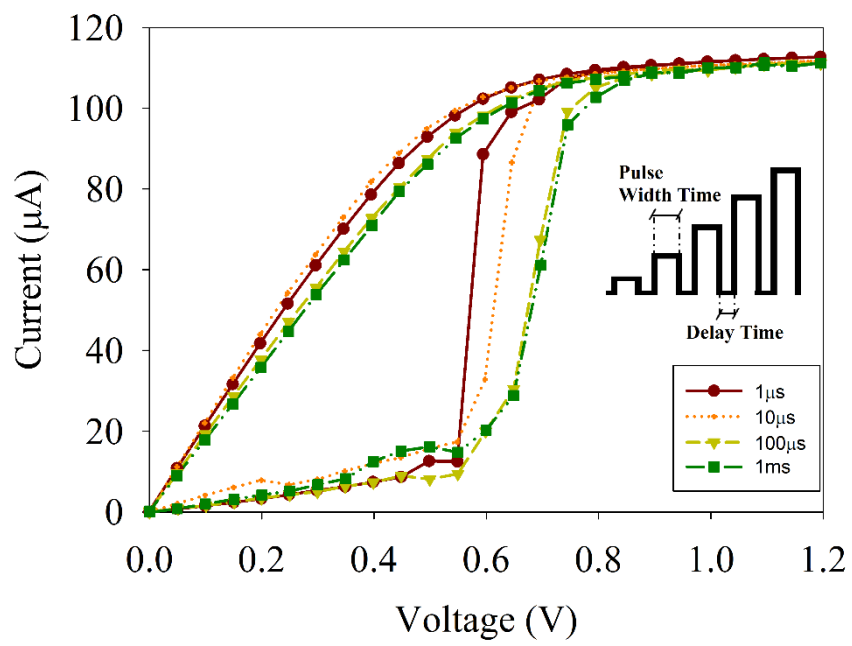

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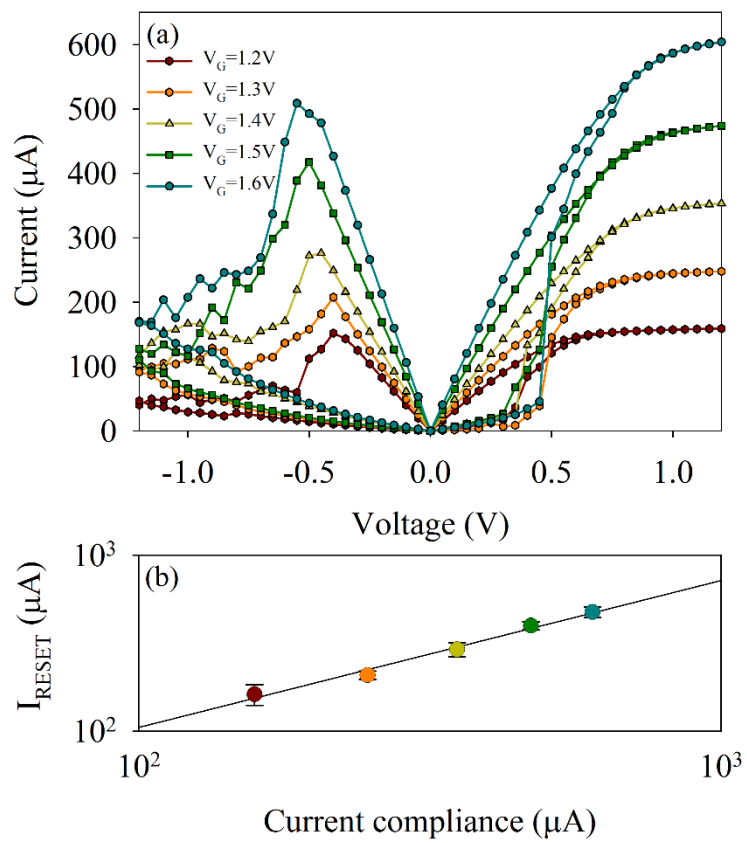
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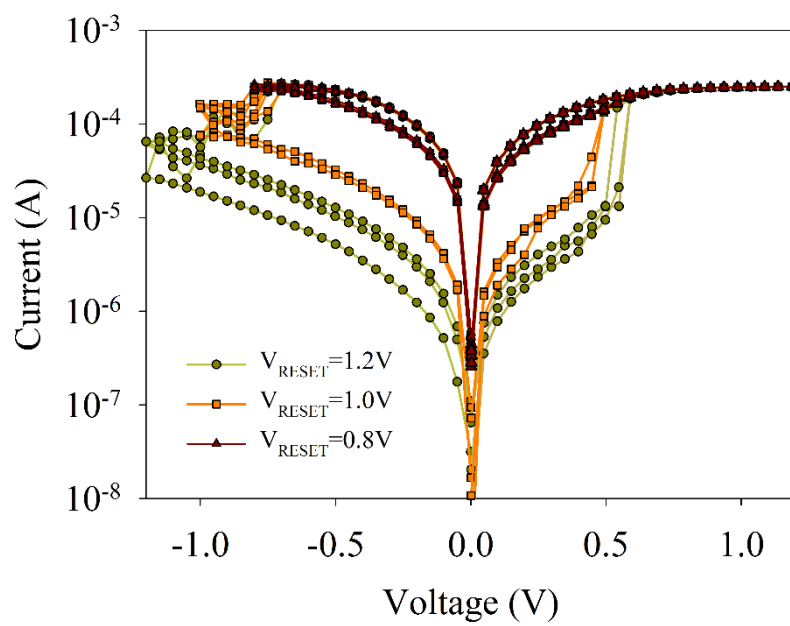
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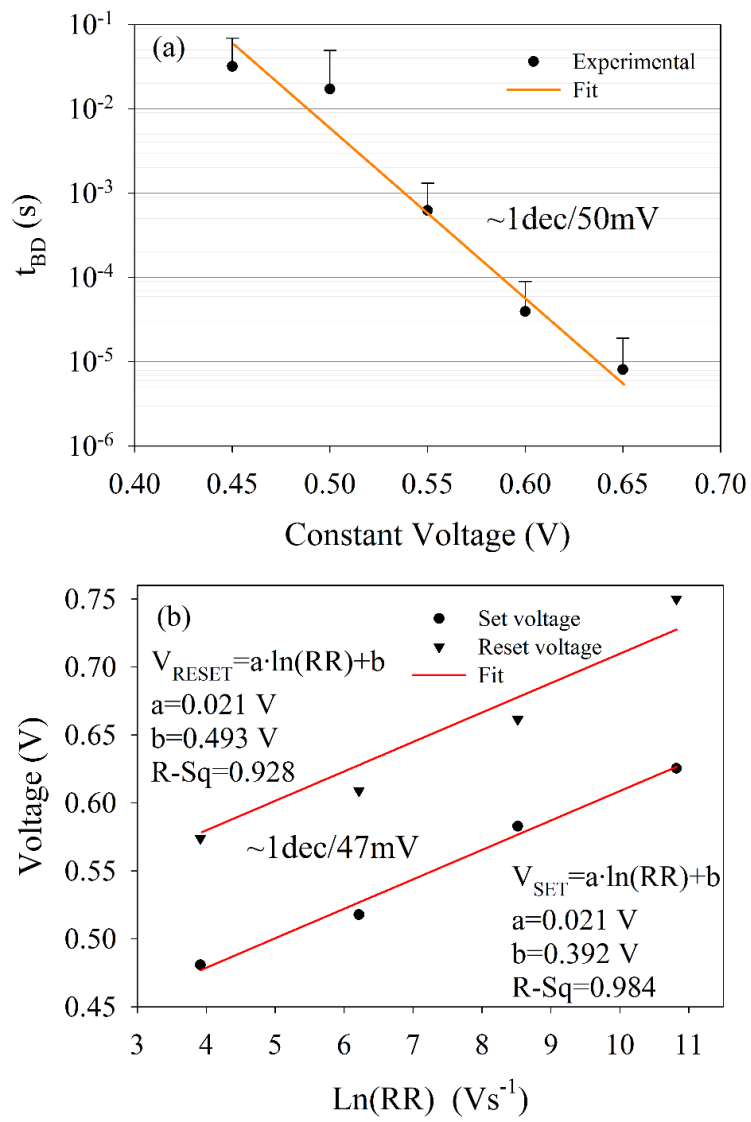
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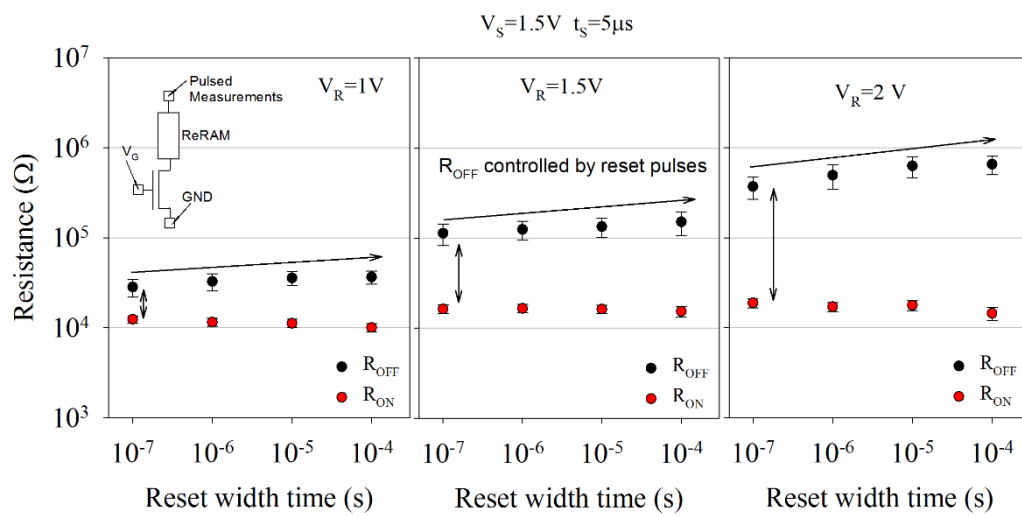
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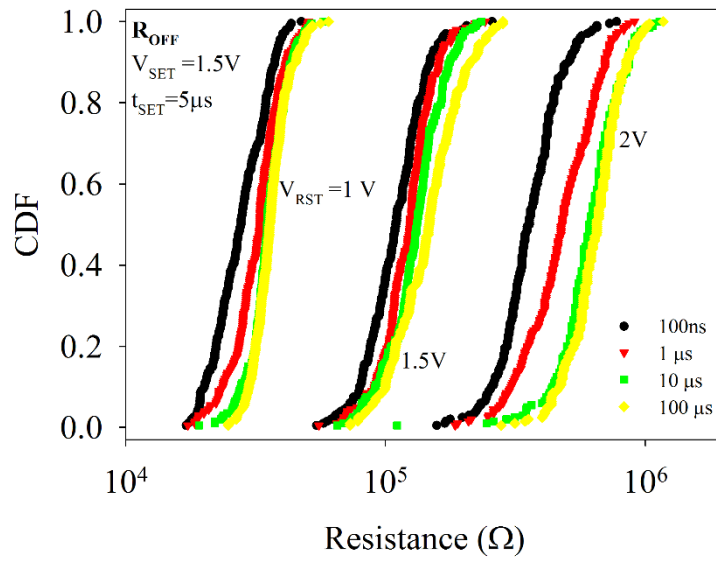
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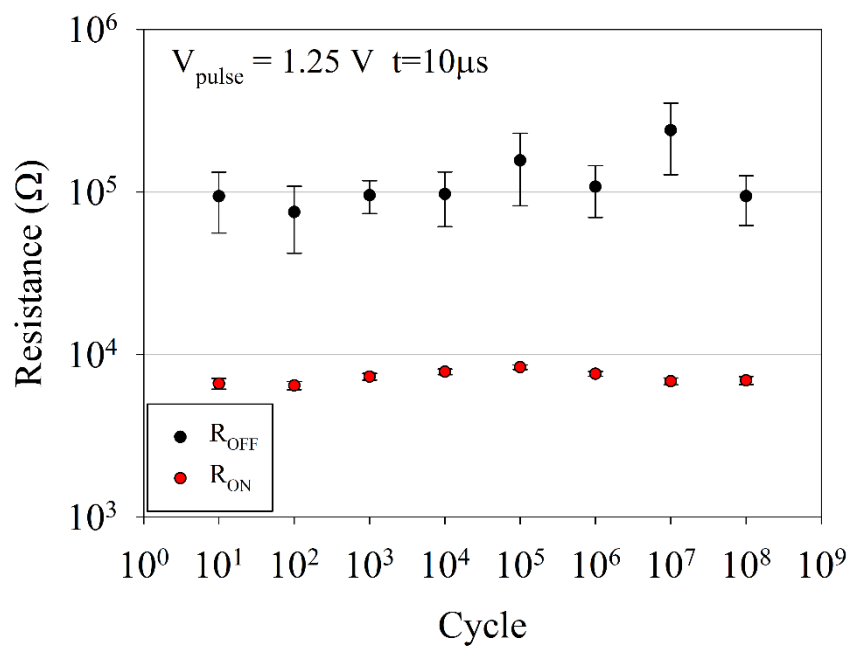
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