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Field effect enhancement in buffered quantum nanowire networks

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III-V semiconductor nanowires have shown great potential in various quantum transport experiments. However, realizing a scalable high-quality nanowire-based platform that could lead to quantum information applications has been challenging. Here, we study the potential of selective area growth by molecular beam epitaxy of InAs nanowire networks grown on GaAs-based buffer layers. The buffered geometry allows for substantial elastic strain relaxation and a strong enhancement of field effect mobility. We show that the networks possess strong spin-orbit interaction and long phase coherence lengths with a temperature dependence indicating ballistic transport. With these findings, and the compatibility of the growth method with hybrid epitaxy, we conclude that the material platform fulfills the requirements for a wide range of quantum experiments and applications.

Material science plays a key role in quantum computing research. Long quantum state lifetimes – the fundamental prerequisite for realizing quantum computers – rely on the ability to produce materials with high purity and structural quality. Together with the requirements of scalability and reproducibility, these properties are what mainly defines the challenges of material science in quantum computing today. Proposals for topological quantum computing,^{1–3} which are based on hybrid semiconductor-superconductor nanowire (NW) networks, are being pursued by numerous research groups and have ignited intense research efforts on hybrid epitaxy.^{4–8} NW scalability is tightly related to the semiconductor growth approach. Top-down lithography has been used to define NWs in two-dimensional layers^{5,9} and a variety of methods have been pursued for alignment and positioning of bottom-up vapor-liquid-solid (VLS) grown NWs, such as dielectrophoresis techniques,¹⁰ nanoscale combing¹¹ and magnetic aligning of NWs.¹² Despite of these developments, large-scale synthesis of bottom-up grown high-mobility NW networks that are compatible with epitaxial interwire connections and semiconductor/superconductor epitaxy has still not been realized. To realize the epitaxial connections, a lot of effort has been put into the growth of branched NWs via the VLS method.^{8,13–15} A scalable approach has been developed in Ref. [16, 17] using template assisted growth of in-plane NW networks.¹⁸ Nonetheless, this approach is not yet compatible with superconductor epitaxy. An alternative scalable approach is to use lithographically defined openings in a mask on a crystalline substrate. This method is referred to as selective area growth (SAG) and

until recently has mainly been used in conjunction with metal organic chemical vapour deposition^{19,20}, metal organic vapour phase epitaxy^{21,22}, chemical beam epitaxy and metal organic molecular beam epitaxy (chemical beam epitaxy).^{23–26} In contrast to molecular beam epitaxy (MBE), the dissociation kinetics of the chemical precursors in these methods enhance the growth selectivity on masked substrates by expanding the growth parameter window, but typically at a cost of crystal purity. Even though the initial work was reported about 30 years ago,^{27–30} only the recent promising results reported in Ref. [31–35] have renewed the interest in SAG by MBE.

In this work, we present selective area growth of InAs NW networks by MBE, which are grown either on GaAs based buffer layers or directly on semi-insulating InP and GaAs substrates. We demonstrate growth of lithographically designed NW networks with well-defined junctions, where the faceting depends on the mask alignment to the crystal orientation of the substrate. We selectively grow Sb-dilute GaAs buffer layers with flat top-facets that protrude out of the substrate plane and allow for significant elastic strain relaxation of the InAs. The improved interface quality results in enhanced field effect response close to conductance pinch-off. In addition, magnetoconductance experiments show strong spin-orbit coupling and phase coherence where the temperature dependence indicates ballistic transport. Therefore, the compatibility of the SAG NW platform with the growth of epitaxial superconductors on selected facets⁴ demonstrates its potential for large-scale applications in the field of gateable superconducting electronics (see Supplementary Information S1 and Ref. [36] for details).

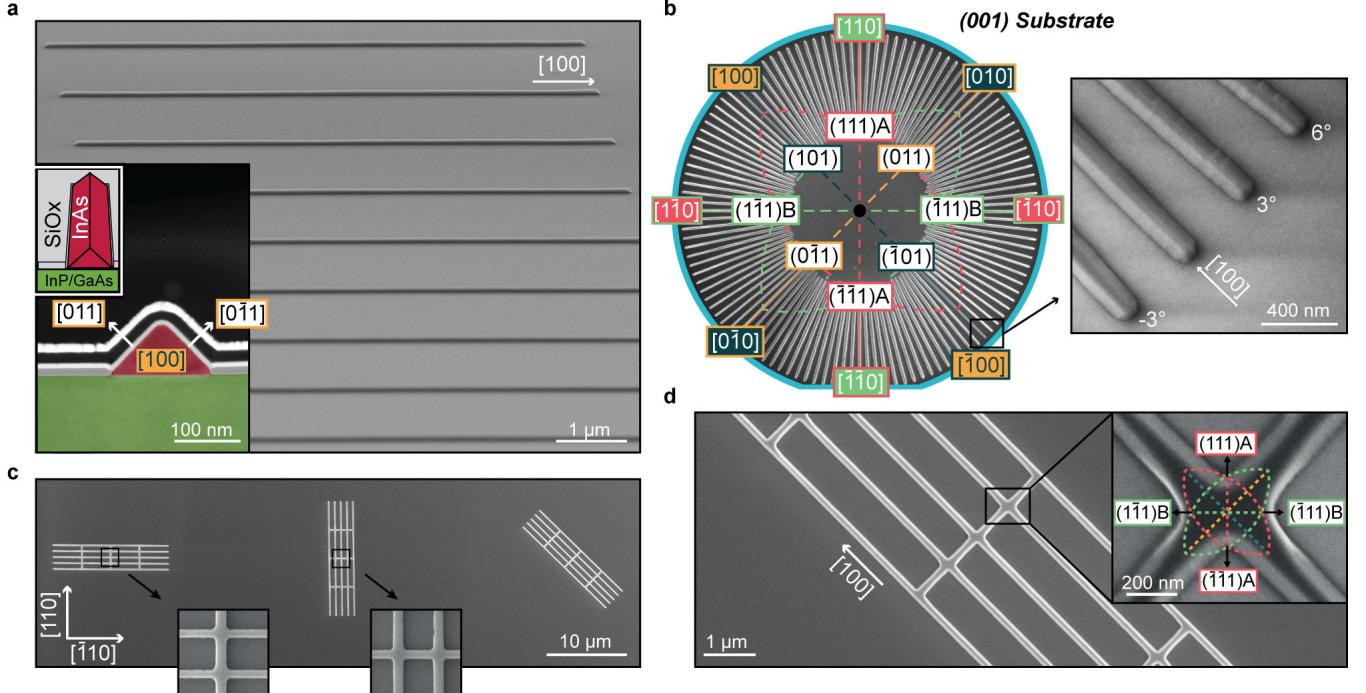


FIG. 1. Selective area grown InAs NW networks. **a**, SEM micrograph of $10\ \mu\text{m}$ long $[100]$ InAs NWs grown on InP (001) with a SiO_x mask. Inset shows a HAADF-STEM cross-section image of a NW, where the orientation and faceting is color-correlated to the stereographic projection in **b**. **b**, Stereographic projection including the high-symmetry orientations of a $[100]$ substrate, where the perimeter corresponds to in-plane NW directions (box fill color), with the facets normal to the NW given by the perpendicular orientations (corresponding border color). The graphics overlay an SEM micrograph of NWs selectively grown at increments of 3° . Zoom-in shows a $[100]$ NW grown next to off-axis NWs with roughened and vicinal faceting. **c**, SEM micrographs of three NW networks aligned along the $[110]$, $[1\bar{1}0]$ and $[100]$ directions. **d**, SEM micrograph of $[100]/[010]$ NW network junctions. Zoom-in shows how the crystal symmetry results in two-fold symmetric junctions indicated by the polar $(111)\text{A}$ and $(111)\text{B}$ facets.

RESULTS AND DISCUSSION

The NWs are grown on semi-insulating InP and GaAs substrates covered with thin dielectric masks, at relatively low growth rates and at growth temperatures similar to those used for corresponding planar growth by MBE, see **Methods**. The mask openings were defined by standard electron beam lithography (EBL) patterning and selective etching, as described in Supplementary Information S2. The substrates become fully insulating at low temperatures and are therefore suitable for as-grown device fabrication and transport experiments directly on the growth substrate. The scanning electron microscope (SEM) micrograph in Fig. 1a shows an array of InAs NWs oriented along the $[100]$ direction on a (001) Fe-doped InP substrate. For SAG of InAs NWs on GaAs substrates, see Supplementary Information S3. The NWs exhibit smooth (011) and $(0\bar{1}1)$ facets, as shown in the colored high-angle annular dark-field scanning transmission electron microscope (HAADF-STEM) image in the Fig. 1a inset. The uniformity of individual NW facets

depends on the growth conditions^{32,34} and the quality of the pre-patterned substrate. Moreover, uniform, high-symmetry facets were found only on NWs oriented along the high-symmetry $[100]$, $[010]$, $[1\bar{1}0]$ and $[110]$ crystal directions, as illustrated in the stereographic projection in Fig. 1b. For instance, a NW oriented along the $[100]$ direction has $\{\bar{0}11\}$, family facets due to local cusps in surface energy. Even though the roughness of the NWs depends on growth conditions, a slight misalignment with respect to the high-symmetry crystal orientation causes vicinal faceting, as shown in the zoom-in of Fig. 1b. Consequently, there are constraints on the in-plane directions, which set the overall symmetry and design of the NW networks. In the case of networks grown on (001) substrates, there are eight high-symmetry in-plane directions (indicated on the perimeter of the stereographic projection). As a result, one junction can be connected to eight NWs. There are two families of networks on (001) substrates consisting of perpendicularly oriented NWs, the $\langle 110 \rangle/\langle 1\bar{1}0 \rangle$ type and the $\langle 100 \rangle/\langle 010 \rangle$ type (see Fig. 1c). At given growth conditions, both types of

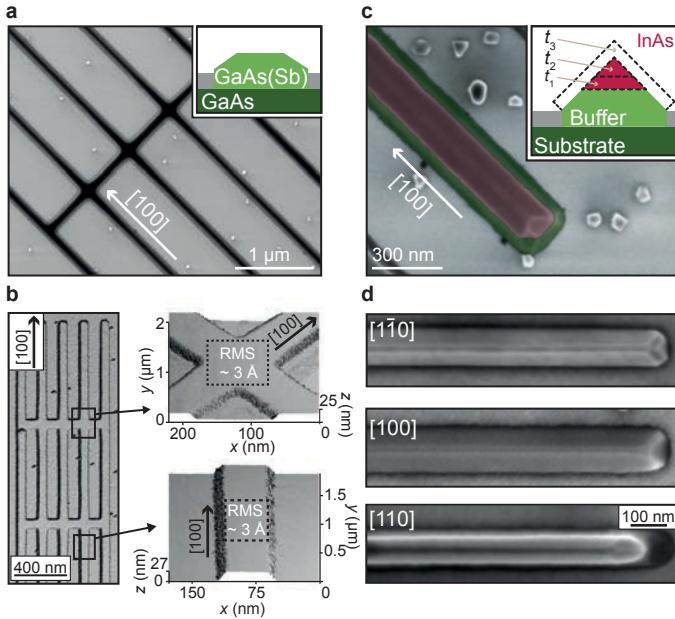


FIG. 2. Selectively grown GaAs(Sb) buffer. **a**, SEM micrograph of a selectively grown GaAs(Sb) NW network. **b**, AFM scans showing flat (001) top-facets of GaAs(Sb) networks aligned along the [100]/[010] directions. Zoom-ins on highlighted areas show the extracted roughness of the top-facet of a junction and a straight NW. **c**, SEM micrograph of InAs NWs selectively grown on the top-facet of the buffer. Inset shows the InAs NW morphology evolution with growth time, t_{1-3} . **d**, SEM micrographs of three types of high-symmetry oriented InAs NWs grown on the buffer.

junctions exhibit a four-fold symmetric morphology for short growth times. However, as the NWs grow thicker, the junctions tend to become two-fold symmetric, see Fig. 1d. In the case of the $\langle 110 \rangle/\langle 1\bar{1}0 \rangle$ junction the symmetry breaking is related to the growth kinetics, where the difference in adatom diffusion lengths along the [110] and [1\bar{1}0] directions causes the material to incorporate easier along the [110] direction.³⁷ At the given growth time and conditions, the $\langle 110 \rangle/\langle 1\bar{1}0 \rangle$ NW junctions maintain a non-tapered four-fold-like morphology as seen in the inset of Fig. 1c. In the $\langle 100 \rangle/\langle 010 \rangle$ case, the symmetry breaking appears earlier, likely due to the different polarity of faceting of the two orientations, as indicated in Fig. 1d.

We find that top-gated InAs NWs grown directly on non-buffered InP or GaAs substrates generally display a weak field effect response close to the conductance pinch-off region. This is most likely related to the NW/substrate interface. To enhance the electrical properties of the NWs we focus on improving the quality of the interface and turn our attention to GaAs_{1-x}Sb_x buffers where the lattice matching can be tuned from GaAs to InAs by changing the composition, x.

In Fig. 2a we show an SEM micrograph of a GaAs(Sb) buffer NW network grown on a semi-insulating (001) GaAs substrate at typical planar GaAs growth temperatures, see Methods. We find that the buffer layer has flat (001) top-facets, with a root-mean-square (RMS) roughness of $\sim 3 \text{ \AA}$. The roughness is uniform across the whole wafer as shown on both single NWs and within the junctions in Fig. 2b (see the Supplementary Information S4 for analysis of the other NW orientations). We emphasize that the flatness of the buffer is a crucial step towards obtaining a low disorder interface to the InAs transport channel. Compositional analysis performed by electron energy loss spectroscopy (EELS) and energy dispersive x-ray spectroscopy (EDX) reveals a very low fraction of Sb (close to the detection limit of $\sim 2\%$). This is lower than the calibrated flux ratios, which would predict $\sim 7\%$ if the incorporation rates of As and Sb were equal. The low incorporation efficiency of Sb is consistent with previous reports.^{38,39} Despite the low Sb incorporation, the surfactant properties of Sb could play an important role in the growth kinetics, and potentially promote a more smooth layer by layer buffer growth. The details of this effect are to be further investigated in forthcoming experiments.

In Fig. 2c we show InAs selectively grown solely on the top-facet of the GaAs(Sb) buffer. The InAs was grown in the lower temperature bound of the selective growth window, which is apparent by the crystallites on the oxide mask. The morphology of the NWs grown on the buffer is highly dependent on the growth time and the width of the buffer top-facet. In the inset of Fig. 2c we show an illustration of how a predicted evolution of the growth would look like if it was thermodynamically driven, i.e. able to reach the lowest free energy (or equilibrium shape) for any given volume. The equilibrium shape of a crystal results from minimizing its anisotropic surface free energy under the constraint of constant volume. If there are additional constraints, such as a mask opening into which the crystal is confined to, then the equilibrium shape will depend on its volume. Assuming that the cross-sectional shape of the SAG NWs are equilibrium shapes, the NWs will most likely first grow solely on the top-facets of the buffer until a fully faceted shape is reached, as illustrated in the inset of Fig. 2c at growth time t_2 . This particular equilibrium shape is also of special interest for realization of high quality SAG NWs, for reasons discussed below. It is clear, that the ratio of the buffer/NW growth time affects the shape and dimensions of the NW structures, and understanding the detailed processes whether it is in thermodynamical or kinetically driven regimes will be subject of ongoing studies.

The top-view SEM micrographs in Fig. 2d show the morphology of the [1\bar{1}0], [100] and [110] high-symmetry NWs, where the InAs NWs completely covers the buffer layer. Interestingly, the incorporation rate is higher on the [110] NWs in this growth. The reasons can be of

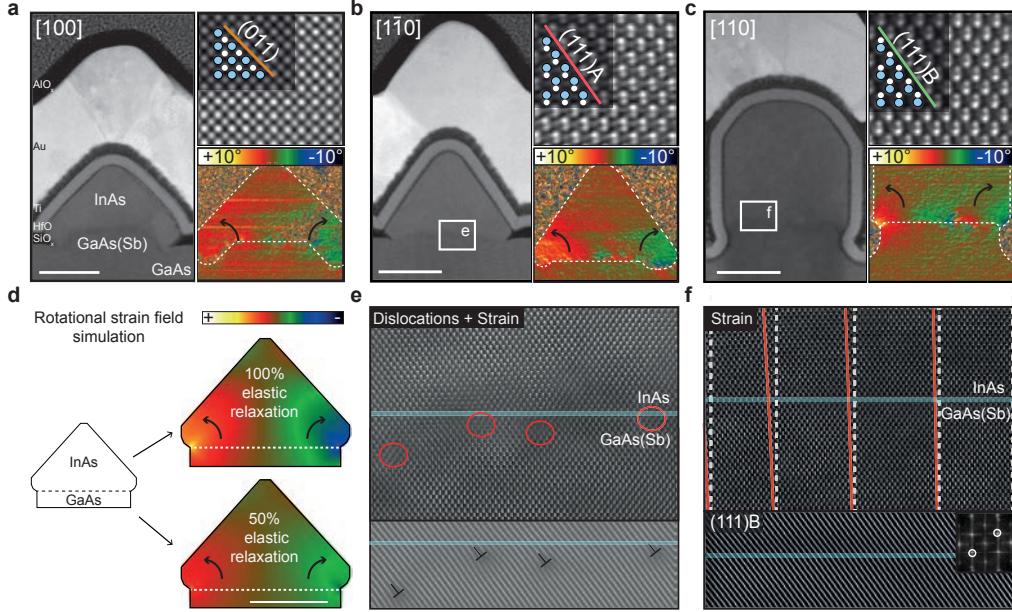


FIG. 3. Elastic strain relaxation of InAs on GaAs(Sb) buffer. **a-c**, Cross-sectional TEM micrographs of top-gated devices with InAs NWs grown on top of GaAs(Sb) buffer layers along the [100], [110] and [110] orientations. Top right insets are cross-sectional HAADF-STEM images of the InAs NW segments with pure crystalline structures, where the illustrated high-symmetry plane highlights the related facet polarity (As atoms: white, In atoms: blue). Bottom right insets show GPA rotational maps around the (111) planes. Scale-bars are 50 nm. **d**, GPA rotational map simulation for a [100] oriented buffered NW showing elastic strain relaxation profiles. Scale-bar is 50 nm. **e**, Atomic resolution aberration corrected HAADF-STEM micrograph of the interface indicated in **b** showing misfit dislocations and strain. The bottom panel is the same image after FFT filtering, with a highlighted aperiodic misfit dislocation array. The blue line indicates the interface. **f**, Atomic resolution aberration corrected HAADF-STEM micrograph of the interface indicated in **c** showing no misfit dislocations and pronounced strain as indicated by the white dashed lines (no strain) and red line (the actual plane displacement). The bottom panel is the same image after FFT filtering, with no visible misfit dislocations.

both thermodynamic or kinetic origin, i.e. due to lower surface energies or lower activation barriers for incorporation, respectively. The latter is a viable possibility, since adatom kinetics on (001) surfaces is known to be highly anisotropic.⁴⁰

Control over the width of the mask opening becomes difficult for features below 90 nm when wet etching is used. However, implementation of the buffer layer, where the top-facet width is decreasing with growth time, also provides an in-situ method for tuning the InAs NW width. This opens up for the possibility of engineering thinner NWs that are not in contact with either the oxide mask or the processed mask-opening (see Supplementary Information S5).

Atomic resolution and aberration corrected HAADF-STEM characterization was performed on cross-sectional cuts of top-gated NW devices in the three high-symmetry orientations. Figure 3 shows the distinct cross-sectional shapes of **a** [100], **b** [110] and **c** [110] InAs NWs, which were grown on the GaAs(Sb) buffer. The HAADF-STEM micrographs show that there are no threading dislocations running through the NWs (as also reported in Ref. [34]) and that the bulk structure is single crystalline for

all the three NW orientations. The highlighted facet planes correspond to the stereographic projection shown in Fig. 1b which will also determine the corresponding NW shape. We further note that the three different types of facets, non-polar, A-polar and B-polar, are likely to have different electron affinities and provide additional band alignment options when optimizing contact to superconductors or metals.

The relative lattice mismatch between the InAs NW and the InP or GaAs substrates is 3% and 7%, respectively. As shown in Supplementary Information S6, when growing directly on InP substrates, without a buffer layer, the lattice mismatch to InAs is fully compensated by relaxation at the interface via periodic arrays of misfit dislocations. That results in an abrupt change of the lattice spacing at the substrate/NW interface. The situation is different for the buffered NWs, where the buffer protrudes out of the substrate plane. Consequently, the InAs NWs have significantly more freedom to make the elastic rotation needed to relax to its equilibrium lattice parameter without introducing dislocations. This effect is observed on all analyzed buffered GaAs(Sb)//InAs interfaces, which is apparent from the gradual change in

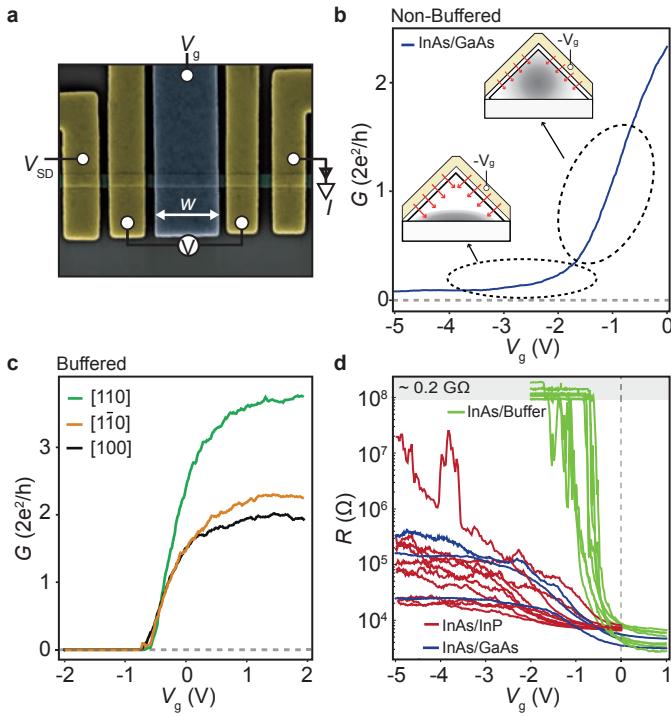


FIG. 4. Carrier density tuning. **a**, False-colored SEM micrograph of a typical top-gated four-probe NW device. Yellow, Ti/Au contacts; blue, gates; grey, InAs NW; V_{SD} , bias voltage; I , measured current; V_g , gate voltage controlling the chemical potential; W , gate width; G , conductance, as a function of V_g , for InAs grown on a GaAs substrate. Sketches illustrate the carrier density distribution as a function of V_g . The two regimes correspond to transport residing in the whole InAs transport channel (lower negative V_g) and at the InAs/substrate interface (more negative V_g). **c**, Conductance as a function of V_g for InAs NWs grown on the GaAs(Sb) buffer along the [110], [1-10] and [100] directions. **d**, Resistance, R , as a function of V_g for multiple NW samples grown directly on InP, GaAs and the buffer layer.

lattice constant and significantly lower density of misfit dislocations.

The lower right insets of Fig. 3a-c show the geometric phase analysis (GPA) of the rotational displacement of the (111) crystal planes. The rotation is a sign of a gradual and partially elastic change of the lattice spacing from GaAs to InAs. An average value for rotation in these structures is on the order of 3° (left side) to -3° (right side). This signature of elastic strain relaxation is illustrated in a qualitative simulation of the rotational displacement field of a fully strained and partially strained GaAs/InAs NW in Fig. 3d, see Methods for simulation details. Figure 3e shows an image of the GaAs(Sb)//InAs interface of the [1-10] NW, where non-periodic misfit dislocations (clearly visible after Fourier filtering) indicate partial plastic strain relaxation. Fig-

ure 3f shows a zoom-in on a GaAs(Sb)//InAs dislocation free interface region of the [110] NW, where the rotation of the (111) crystal planes peaks at 4.5° . Here, the interface is nearly dislocation free except for a small region close to the middle of the NW, which means that the NW is close to be fully elastically strain relaxed in the transverse component. The results of the GPA analysis show that most of the elastic strain is released within ~ 20 nm around the interface, where the lattice constant changes from 5.71 to 6.06 Å with a mean dilatation of 6.1 %, see Supplementary Information S6.

We note that the strain relaxation mechanism is similar to that in axial heterostructures of free standing VLS grown NWs⁴¹ and to the elastic rotation previously observed in InGaN/GaN⁴² and InAs/InSb.^{43,44} This very important trend opens new possibilities for engineering of elastically strain relaxed SAG NW structures and clearly shows the potential and importance of growth on the top-facet of SAG buffers. This is also apparent from the fact that the InAs NW on the GaAs(Sb) buffer has fewer misfit dislocations than in the case of direct growth on InP substrate, which has a lower lattice mismatch to InAs, see Supplementary Information S6.

For computing applications – classical or quantum – the device performance depends on the ability to effectively gate and pinch-off conductance. Since back-gating can be challenging on semi-insulating substrates we use top-gates for the carrier density control. Figure 4a shows a false-colored device lithographically similar to the characterized devices, where only gate width, W , is varied. Figure 4b shows conductance, G , as a function of gate voltage, V_g , for an InAs NW grown on the non-buffered GaAs substrate. The charge carrier density is not fully depleted even for very negative V_g and the down and up gate traces are highly hysteretic, see Supplementary Information S7. This is a general trend for the non-buffered NWs we measured (on both GaAs and InP). The schematics depict two characteristic gate voltage regions with different slopes of conductance. Due to the top-gate geometry, the carriers in the NW will first be depleted in the top part of the NW, corresponding to the region with the highest slope in Fig. 4b. As more negative V_g is applied, the carrier density moves towards the NW/substrate interface. The transconductance depends on the quality of the semiconductor crystal. This allows for qualitative distinction between bulk NW and NW/buffer interface properties. Therefore, the interface is mainly probed at more negative gate voltages (as indicated by the sketch in Fig. 4b). For NWs grown directly on the substrate, the bottom interface appears to have a significantly lower field effect mobility. The low interfacial quality caused by the presence of misfit dislocations, potential impurities and roughness originating from the etching process. Additionally, the pre-growth annealing step used to remove the native oxide is likely to play an important role.⁴⁵

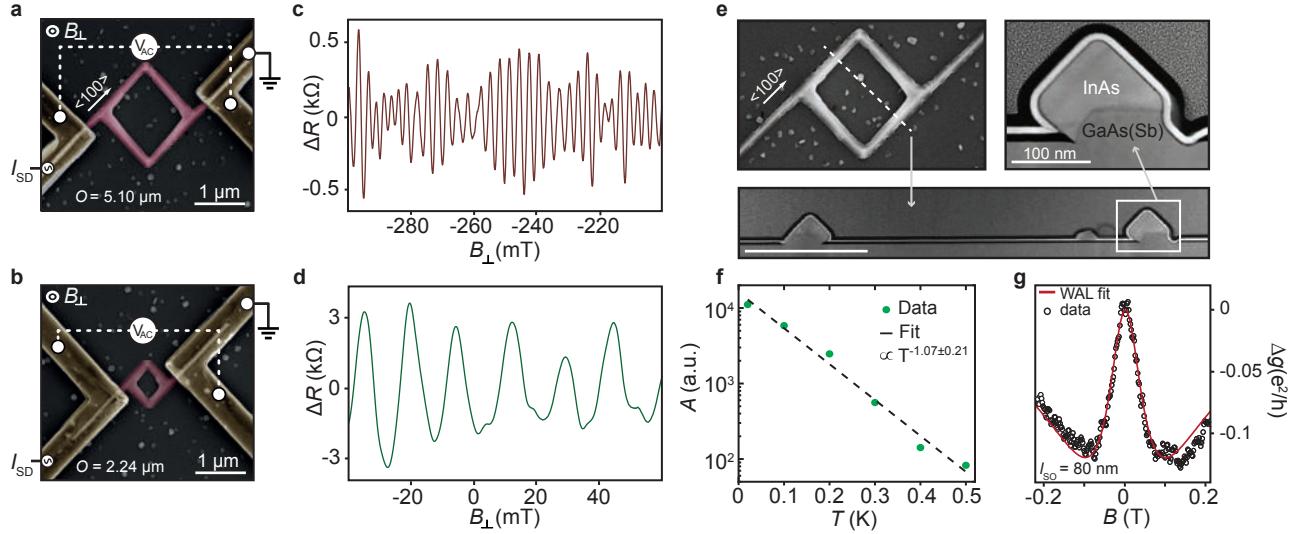


FIG. 5. Low temperature magneto-conductance measurements. **a-b**, False-colored SEM micrographs of the four-probe NW loop devices. **c-d**, Change in resistance, ΔR , as a function of perpendicular magnetic field, B_{\perp} , over a 100 mT range showing electron phase interference oscillations for the larger and smaller loop, respectively. **e**, Overview SEM and cross-section HAADF-STEM micrographs of the Aharonov-Bohm loop structure showing the asymmetric cross-section. The dashed white line indicates where the cross-section was made. Scale-bar corresponds to 500 nm. **f**, Integrated FFT of the oscillations plotted as a function of temperature. Fit corresponds to the linear fit of the h/e oscillation where $l_{\phi} \sim 13 \mu\text{m}$. **g**, Off-set magneto-conductance traces showing WAL effects around $B = 0$. The spin-orbit length ($l_{\text{SO}} \sim 80 \text{ nm}$) is found from the diffusive regime WAL expression fit.

Figure 4c shows examples of G as a function of V_g for three InAs NWs grown on the buffer layer in the three high-symmetry crystal orientations. The measurements on buffered NWs show a high degree of reproducibility, as all the NWs measured on this growth, pinch-off within a window of ~ 250 mV. In contrast to the non-buffered NWs in Fig. 4b, there is no apparent difference in transconductance between the bulk and the interface gate regions, indicating that the quality of the interfaces is significantly improved. In Fig. 4d we show data from multiple buffered and the non-buffered NWs of comparable dimensions. Here, the gate dependent resistance is shown for different high-symmetry NW orientations, with W varying from 250 nm to $2.5 \mu\text{m}$. On the logarithmic scale, it is apparent that the conductance is not completely pinched-off in any of the non-buffered NW devices (within reasonable gate range and with selected NW volumes). In addition the non-buffered NWs show more pronounced hysteresis in down/up gate sweeps than the buffered NWs, as presented in Supplementary Information S7.

Even though the field effect mobility depends on the gate voltage, V_g , range and carrier density distribution, we use a full fit to the conductance as a function of V_g to extract the mean mobility, as shown in Ref. [46]. For details of fitting and finite element modeling of the capacitance see Supplementary Information S8 and S9. The

average mean mobility measured on the buffered NWs is about $\bar{\mu} \sim 5600 \pm 1300 \frac{\text{cm}^2}{\text{V}\cdot\text{s}}$ with a maximum at $\sim 7600 \frac{\text{cm}^2}{\text{V}\cdot\text{s}}$ (extracted from 24 data sets - 6 buffered devices at 1, 2, 5 and 10 mV bias). More detailed finite element method modeling of the capacitances, including the detailed modeling of the specific cross-sectional shapes, is required for a more exact estimation and for comparison of different NWs and NW orientations. It is clear that the buffer layer significantly improves the transport characteristics of the NWs, regardless of their orientation or cross-sectional area.

We now turn our focus to the quantum transport properties, where quantum phase coherence, scattering length and spin-orbit strength are important characteristics. To study the phase coherence we first fabricated two four-probe loop devices with a circumference of $5.1 \mu\text{m}$ and $2.24 \mu\text{m}$ for Aharonov-Bohm (AB) type measurements as shown in Fig. 5a and b, respectively. The resistance shows oscillations in perpendicular magnetic field, B_{\perp} , as seen in the 100 mT sweep range in Fig. 5c and d. Magnetic fields on the order of 900 mT were applied along the $[110]$ and $[1\bar{1}0]$ in-plane substrate orientations in order to reduce weak anti-localization effects and the aperiodic oscillating background was removed by Savitzky-Golay filtering.⁴⁷ The oscillation periods of $\sim 2.5 \text{ mT}$ (large loop) and $\sim 14 \text{ mT}$ (small loop) are in good agreement with the areas of the loops, given as $\sim h/(e \cdot \text{area})$. In Fig. 5e we show a cross-sectional TEM image of the

loop, as indicated with the dashed line on the SEM image. The asymmetric shape of the InAs NWs on the GaAs(Sb) buffer is related to the growth mechanism of minimizing surface to volume ratio at the junction between the two high-symmetry orientations. We expect this effect to be suppressed with shorter growth time, in line with the discussion on the growth evolution above.

The phase coherence length $l_\phi(T)$ can be extracted by fitting the temperature dependence of the AB oscillation amplitude, A , obtained from the Fourier spectra (see Supplementary Information S10). Assuming that the amplitude scales as $A(T) \propto \exp(-\frac{O}{l_\phi(T)})$, where O is the loop circumference⁴⁸, then the exponent m in $l_\phi(T) \propto T^{-m}$ can be determined. For the small loop we extract the exponent and the phase coherence length by fitting to the logarithm of the amplitude, and get $m = 1.07 \pm 0.21$ and $l_\phi(20\text{mK}) = 13 \pm 1 \mu\text{m}$, see Fig. 5f. It was not possible to obtain a reliable temperature dependence on the large loop due to charge noise switching. In the diffusive regime the temperature dependence of the coherence length in a loop shaped structure follows $l_\phi \propto T^{-1/2}$, while in the ballistic case with a weak coupling to the environment $l_\phi \propto T^{-1}$ as reported in Ref. [49–51]. This indicates that the small loop resides in the ballistic regime below $\sim 500 \text{ mK}$ while the non-buffered loop reported in Ref. [36] in the diffusive regime.

The dephasing mechanisms are different in a quasi-one dimensional NW and exhibit a different temperature dependence of $l_\phi \propto T^{-1/3}$ in the diffusive regime.^{52–54} With weak anti-localization (WAL) measurements on single NW, we extract a significantly smaller l_ϕ than compared to the loop measured in Fig. 5f. The theoretical model for the WAL effect, as explained by Ref. [55, 56], is fitted to the data. We emphasize that no analytical expression exists for finite 3D cross-section and this type of extraction should only used for comparison between NWs. From the fit we extract a spin-orbit length, l_{SO} , on the order of 80 nm and l_ϕ on the order of 180 nm, which is comparable to numbers extracted from similar measurements on VLS grown InAs, InSb and InAs_{1-x}Sb_x NWs.^{7,57–60}

In conclusion, we show that selective area growth of high-quality InAs NW networks with well defined junctions is feasible in MBE. The NWs can attain significant elastic strain relaxation when grown on top of flat selective area grown buffer layers, with significant improvement of the transport properties in terms of field effect response. Moreover, the material possesses promising quantum transport properties, e.g. strong spin-orbit coupling extracted from WAL and phase coherence demonstrated by AB experiments. We believe that these findings, combined with superconductor epitaxy,³⁶ make this material platform an ideal large-scale architecture for quantum applications that are based on gateable superconducting electronics.

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AUTHOR CONTRIBUTIONS

The crystal growth was done by FK, JES, PA, FB and PK with support from YL, RK and EU, and substrate fabrication by FK, JES, LC and AF. Device fabrication was done by FK, JES, SV, LC. Atomic force microscopy characterization by SAK. Transmission electron microscopy based characterization, sample preparation and related analysis (including GPA and EELS) was carried out by SMS and JA, with strain analysis and simulation by TS, FK, JES, PK. Electronic characterization and analysis was done by JES, FK, SV, LC, AW, LPK, CMM and PK. FK, JES and PK wrote the paper with contributions from all authors.

COMPETING INTERESTS

The authors declare no competing interests.

METHODS

Substrate preparation. Semi-insulating and epi-ready Fe doped InP and un-doped GaAs substrates were covered with 10–30 nm of SiO_x in a SPTS Multiplex plasma enhanced chemical vapor deposition system at 300°C.

The patterning of the wafers was done by standard electron beam lithography processing, and the oxide mask was etched in an ammonium fluoride solution or reactive ion etching before stripping the resist in acetone.

SAG NW growth by MBE. InP/GaAs substrates with $\text{SiO}_x/\text{SiN}_x$ masks, were used for non-buffered selective area growth of InAs. The native oxide was removed under an As_2 overpressure following standard procedure on bare substrates. InAs was grown at around 500°C with a corresponding planar growth rate of $\sim 0.1 \mu\text{m}/\text{h}$ for InAs and $0.26 \mu\text{m}/\text{h}$ for GaAs substrates. For buffered growth on GaAs the native oxide was blown-off as described above, before GaAs(Sb) was grown under similar conditions using a corresponding planar growth rate of $\sim 0.1 \mu\text{m}/\text{h}$ and an $\text{As}_2/\text{Sb}_{2+4}$ ratio of 7. Following InAs growth on the buffered GaAs(Sb) on GaAs was carried out at the same temperature with a corresponding planar growth rate of $\sim 0.1 \mu\text{m}/\text{h}$.

Cross-section STEM characterization. Selected devices were covered with 15 nm of ALD Al_2O_3 and thinned into cross-sectional lamellae. Several cross-sectional lamellae on selected NWs were cut by using a focused ion beam. TEM Characterization: HR-TEM, HAADF scanning TEM (STEM) and EELS spectrum imaging (SI) were performed using a TECNAI F20 field emission gun microscope operated at 200 kV with a point to point resolution of 0.14 nm coupled to a GATAN Quantum EELS spectrometer. The atomic resolution HAADF-STEM images were acquired on a probe corrected FEI Titan 60-300 equipped with a high brightness field emission gun (XFEG) and a CETCOR corrector from CEOS to produce a probe size below 1 Å. The microscope was operated at 300 kV, with a convergence angle of 25 mrad and an inner collection angle of the detector of 58 mrad. Atomic resolution aberration corrected HAADF-STEM was used to determine with high accuracy the atomic column positions, allowing the detailed study of polarity⁶¹ as well as the final strain analysis by means of GPA⁶².

Elastic strain simulations. Rotational deformation fields were simulated using finite element method software COMSOL Multiphysics®. A 2D model was made, consisting of GaAs and InAs parts with a continuous boundary in between. Initial compressive strain was applied to InAs, in order to simulate the effect of the lattice mismatch. A stable solution of elastic strain distribution was then found assuming anisotropic linear elasticity, with elastic constants for GaAs⁶³ and InAs⁶⁴. Presence of dislocations at the interface results in lower values of elastic relaxation in a form of lattice rotation, compared to the fully epitaxial case.

Device fabrication. Devices were fabricated directly on the growth substrate by spinning poly-MMA resist at 4000 RPM for 45 s and baked at 185°C . Standard EBL procedures were used to expose contacts. The native oxide was removed by RF Argon ion milling at 15 W for 5 min before depositing 10 nm Ti and 180 nm Au as

ohmic contacts. 8 nm of ALD HfO_2 was grown at 90°C , before standard EBL patterning followed by deposition of Au top-gates.

5 K measurements. The samples were cooled and outgassed overnight in a Lakeshore 4K cryo-free probe station operating at a base temperature of $T \sim 5 \text{ K}$. Standard four-probe measurements were performed using a Keithley 2600 sourcemeter to control the gate voltage, the source-drain bias and measure the current. An Agilent digital multimeter was used to probe the voltage drop on the inner contacts.

20 mK measurements. The WAL measurements were carried out using standard current-biased ac lock-in techniques in a Bluefors XLD-400 dilution refrigerator operating at a base temperature of $T \sim 20 \text{ mK}$. The AB experiments were carried out using current-biased ac lock-in technique in a Oxford Triton 100 dilution refrigerator with a base temperature of $T \sim 20 \text{ mK}$. Magnetic fields aligned to the [110] and [1̄10] directions on the order of 900 mT were applied to suppress the WAL effect during the measurement while sweeping the perpendicular magnetic field.

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