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Compact CPW power splitter with filtering capability based on slow-wave structures

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Abstract

A compact coplanar waveguide (CPW) power splitter with filtering capability is presented in this paper. The splitter consists of a pair of 70.71 Ω impedance inverters implemented by means of inductively and capacitively loaded slow-wave structures. Such slow-wave structures efficiently shorten the length of the inverters, thereby providing substantial size reduction to the power splitter. The filtering functionality is due to the Bragg effect, related to periodicity. The proposed splitter, designed to be functional at 1 GHz, exhibits good performance at that frequency, with measured return loss of 20.6 dB and insertion loss of 3.15 dB and 3.23 dB at the output ports. Moreover, the suppression level (at the output ports) at the first (3 GHz), second (5 GHz) and third (7 GHz) harmonic frequency is better than 12.4 dB, 34.6 dB and 24.7 dB, respectively. As compared to the length of the ordinary inverters, the length of the constitutive slow-wave impedance inverters of the designed power splitter is reduced by a factor of two.

Keywords: slow-wave structures, coplanar waveguides, power splitter

1. Introduction

Slow-wave transmission lines are artificial lines typically consisting of a host line periodically loaded with reactive elements [1,2]. The presence of reactive elements, e.g., shunt-connected capacitances [3-17], series-connected inductances [18-22], or a combination of both reactive elements [23-27], decreases the phase velocity of the line (slow-wave effect), thereby shortening the wavelength of the propagating signals. Therefore, these slow-wave artificial lines are useful for device miniaturization, since, for a required electrical length (dictated by design specifications), the physical length of such lines is shorter than the one of their ordinary counterparts. An additional property of such lines is the filtering capability, related to periodicity (Bragg effect) [2,28,29]. Namely, reactively loaded periodic lines exhibit pass bands and stop bands [30]. By properly designing the slow-wave transmission lines, it is possible to generate the rejection bands in frequency regions useful for harmonic or spurious suppression, and simultaneously obtain a behavior similar to the one of ordinary lines at lower frequencies (i.e., dispersion-less and all-pass functionality). Within these context,
several works report compact microwave components with harmonic or spurious suppression capability [3-27,31-38].

Most slow-wave artificial lines and the corresponding (compact and eventually harmonic suppressed) microwave circuits have been implemented in microstrip technology [8,9,11,14,16,17,18,22,26,33,34], and only few of them have been designed and fabricated in coplanar waveguide (CPW) technology [1,20,25]. In [25], slow-wave CPW transmission lines based on simultaneous capacitive and inductive loading were reported. Such lines, applied to the design and fabrication of a compact and harmonic suppressed power splitter based on a single 35.35 Ω impedance inverter in [25], consist of a CPW line where the series inductances and shunt capacitances are implemented by means of slots in the ground plane and backside patches, respectively. In this paper, the main aim is to apply such slow-wave CPW transmission lines to the design of a power splitter with compact dimensions and filtering functionality, but alternatively to [25], based on a scheme where a pair of 70.71 Ω impedance inverters is considered. Consequently, the constitutive 90º (as corresponds to a quarter-wavelength impedance inverter) and 70.71 Ω slow-wave lines are first designed, and then they are applied to the implementation of the power splitter. The fabrication and characterization results are presented in the last part of the paper.

2. Design of the slow-wave transmission lines

The topology and equivalent circuit model of the slow-wave transmission line (unit cell) are depicted in Fig. 1. The host line (a CPW) is loaded with a series inductance, $L_{ls}$, implemented by means of a pair of symmetric slots etched in the ground plane, and with a pair of shunt capacitances, $C_{ls}/2$, achieved by means of two patches etched in the back substrate side and connected to the central strip by means of a via. The host line is described by the characteristic impedance $Z_0$, and by the electrical length ($kl$), where $k$ is the phase constant and $l$ is the total (physical) length of the unit cell. Losses are excluded in the circuit model. As it was demonstrated in [25], the electrical length, $\beta l$, and the characteristic impedance, $Z_B$, of the loaded line, the two fundamental design parameters, are given by:

$$\cos(\beta l) = \cos(kl) - \left(\frac{L_{ls}}{2Z_0} + \frac{C_{ls}Z_0}{2}\right)\omega \sin(kl) - \frac{L_{ls}C_{ls}}{2} \omega^2 \cos^2(kl/2)$$ (1)

$$Z_B = \frac{-jB}{\sin(\beta l)} = \frac{Z_0 \sin(kl) + \omega L_{ls} \cos^2(kl/2)}{\sin(\beta l)}$$ (2)

$\omega$ being the angular frequency. Note that from the previous two equations, the four unknowns ($Z_0$, $kl$, $L_{ls}$ and $C_{ls}$) cannot be unequivocally determined. Indeed, an additional condition comes from the required size reduction of the slow-wave transmission line, determined by the so-called slow wave ratio, $swr$, defined by
where \( v_{pl} \) and \( v_{po} \) are the phase velocities of the loaded and unloaded lines, respectively. As it was pointed out in [25], the physical length of the slow wave transmission line, as compared to the one of the ordinary line, is dictated by the \( \text{swr} \). Nevertheless, due to the finite size of the reactive elements loading the line, the actual length of the slow-wave transmission line is not as small as the value predicted by the \( \text{swr} \).

From expression (3), once \( \beta l \) is set to a given value (dictated by design specifications), \( kl \) is directly obtained. The remaining parameters of the slow-wave transmission line, \( Z_0 \), \( L_{ls} \), and \( C_{ls} \), cannot be unequivocally determined from equations (1) and (2). However, extreme values of \( L_{ls} \) and \( C_{ls} \), that may prevent the implementation of such reactive components, must be avoided. In this regard, a trial-error approach is reasonable, where a guess value of \( Z_0 \) is provided and then \( L_{ls} \) and \( C_{ls} \) are isolated from (1) and (2). If such values are implementable, the value of \( Z_0 \) is considered to be the one to be synthesized (note, however, that \( Z_0 \) may be swept over a certain finite interval, yet providing implementable \( L_{ls} \) and \( C_{ls} \) values).

Another important aspect is the number of cells, \( N \), of the considered slow-wave transmission line section. Obviously, it is intimately related to the electrical length of the unit cell, \( \beta l \), which must be a submultiple of the total electrical length of the transmission line, designated as \( \theta \). In other words, \( \theta = N \cdot \beta l \). Actually, the design parameter is \( \theta \) (e.g., \( \theta = \pi/2 \) for an impedance or admittance inverter), rather than \( \beta l \), but once \( N \) is set to a certain value, then \( \beta l \) is automatically determined. It was demonstrated in [25], and in other papers by the authors [14,26], that the preferred option to simultaneously leave the passband of interest unaltered and suppress the first harmonic bands in circuits based on transmission line impedance inverters, is to set \( N = 2 \). Therefore, this is the value adopted in this paper, as long as a harmonic suppressed power splitter based on a 70.71 \( \Omega \) impedance inverter is pursued.

3. Synthesis of the slow-wave impedance inverter

The slow-wave transmission line to be synthesized is an impedance inverter with \( \theta = \pi/2 \), \( Z_B = 70.71 \Omega \) (the considered operating frequency has been set to \( f_0 = 1 \text{ GHz} \)). Since \( N = 2 \) (see previous section), it follows that \( \beta l = 45^\circ \). The slow wave ratio has been set to \( \text{swr} = 0.5 \), and, therefore, \( kl = 22.5^\circ \). In regard to the remaining unknowns, \( Z_0 \), \( C_{ls} \) and \( L_{ls} \), the characteristic impedance of the host line has been tentatively set to \( Z_0 = 70 \Omega \), providing the following reactive values: \( C_{ls} = 0.93 \text{ pF} \) and \( L_{ls} = 3.96 \text{ nH} \). It has been found that such values can be easily implemented in CPW technology by means of the aforementioned backside patches and ground plane slots, respectively (hence these values of \( Z_0 \), \( C_{ls} \) and \( L_{ls} \) have been considered to be definitive).

In order to generate the unit cell layout, the slot dimensions providing the required inductance value, as well as the dimensions of the transverse backside patches
necessary to achieve the shunt capacitance, have been independently determined. Nevertheless, some post-optimization has been necessary in order to adjust the characteristic impedance and electrical length to the design values at the operating frequency. The resulting layout of the unit cell is the one depicted in Fig. 1. The characteristic impedance and the electrical length of the unit cell, inferred by electromagnetic simulation of the layout by means of Keysight Momentum, are depicted in Fig. 2, where it is apparent that the required values at \( f_0 \) (i.e., \( Z_B = 70.71 \, \Omega \) and \( \beta l = 45^\circ \)) are achieved. By concatenating two cells, we do expect that \( \theta = 90^\circ \) at \( f_0 \), as Fig. 3 corroborates. In such figure, the transmission and reflection coefficients, referred to a 50 \( \Omega \) port impedance, are also depicted. Moreover, we have included in Fig. 3 (and in Fig. 2) the corresponding curves obtained through circuit simulation of the equivalent circuit model, and the agreement is excellent up to roughly 4.5 GHz, i.e., clearly above \( f_0 \). At higher frequencies, the disagreement is because the patch capacitance and inductive slots can no longer be considered semi-lumped components. In the previous electromagnetic simulations, the considered substrate is Rogers RO3010 with thickness \( h = 1.27 \, \text{mm} \), dielectric constant \( \varepsilon_r = 10.2 \) and loss tangent \( \tan \delta = 0.0023 \).

4. Fabrication of the power splitter and experimental results

The layout and the photograph of the designed slow-wave power splitter are depicted in Fig. 4 (notice that air-bridges, implemented by means of backside strips and vias, have been used in order to suppress the parasitic CPW slot mode). Fig. 5 depicts the return loss \( (S_{11}) \) and power splitting \( (S_{21} \text{ and } S_{31}) \) of the divider, inferred from circuit, electromagnetic simulation (with and without losses) and measurement. The designed slow-wave power splitter has been fabricated by means of a LPKF-H100 drilling machine, and the measured response has been obtained by means of the Keysight PNA 5221A vector network analyzer. The response of the slow-wave power splitter is roughly the same than the one of the ordinary splitter in the region of interest (vicinity of \( f_0 \)), also included in Fig. 5(a). Particularly, \( S_{21} = -3.15 \, \text{dB} \), \( S_{31} = -3.23 \, \text{dB} \) and \( S_{11} = -20.6 \, \text{dB} \) at \( f_0 \) (measured values). However, the first (at \( 3f_0 \)), second (at \( 5f_0 \)), and third (at \( 7f_0 \)) harmonic bands of the conventional splitter are significantly suppressed in the slow-wave implementation, i.e., the measured suppression levels for port 2 have been found to be 12.4 dB, 34.6 dB and 34.3 dB, respectively, and 12.7 dB, 42.6 dB and 24.7 dB, respectively, for port 3. With these results, it is clearly demonstrated that the proposed strategy, based on replacing the ordinary inverter of the splitter with a slow-wave transmission line, is useful to achieve power splitting and filtering simultaneously. Moreover, the filtering action provides significant levels of harmonic suppression. Indeed, the achieved stopband region (considering a suppression level of at least 10 dB) extends up to at least \( 7f_0 \), superior than in the splitter reported in [25].

Concerning splitter dimensions, these are mainly determined by the length of the synthesized slow-wave impedance inverter. The actual ratio between the length of the designed inverter and the ordinary counterpart (implemented by means of a conventional 90° line) is 0.505, i.e., slightly superior that the theoretical value given by the considered \( swr \) (for the reasons explained above). However, the achieved size
reduction of the inverter is very close to the nominal value, hence providing a small size to the fabricated splitter.

5. Conclusions

In conclusion, a compact and harmonic suppressed CPW power splitter based on a pair of slow-wave transmission line 70.71 Ω impedance inverters has been designed and fabricated. Roughly 50% length reduction in the inverters has been achieved (as compared to the length of the ordinary CPW inverters), and the fabricated splitter has been demonstrated to efficiently reject at least the first three harmonic bands, leaving the response in the region of interest unaltered. It has been shown that the proposed circuit model of the slow-wave transmission line inverter, useful for design purposes, provides a good description of the behavior of the splitter in the region of interest, and such good agreement between the circuit and the electromagnetic responses extends up to 4.5\(f_0\).

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References


Fig. 1. Topology (unit cell) (a) and circuit schematic (b) of the slow wave CPW transmission line.
Fig. 2. Electrical length (a) and characteristic impedance (b) of the inverter unit cell. Dimensions are (in reference to Fig. 1): \(L_w = 7.00\) mm, \(W_w = 5.00\) mm, \(L_f = 1.30\) mm, \(W_f = 1.63\) mm, \(L_C = 4.55\) mm, \(W_C = 0.50\) mm, \(w = 0.38\) mm, \(s = 0.40\) mm.
Fig. 3. Layout of the whole inverter, including two cells (a), transmission and reflection coefficients (b), and electrical length (c).
Fig. 4. Layout (a) and photograph (b) of the designed and fabricated power splitter.
Fig. 5. Response of the splitter, including matching ($S_{11}$) and power splitting ($S_{21}$ and $S_{31}$). (a) Circuit and lossless electromagnetic simulation; (b) lossy electromagnetic simulation and measurements. The lossless electromagnetic simulation of the conventional power splitter is also included in (a).