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Vescio, Giovanni; Martín, Gemma; Crespo-Yepes, Albert; [et al.]. «Low-power, high-performance, non-volatile inkjet-printed HfO 2 -based resistive random access memory: from device to nanoscale characterization». ACS Applied Materials and Interfaces, Vol. 11, issue 26 (2019), p. 23659-23666. DOI 10.1021/acsami.9b01731

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# Low-Power High-Performance Non-Volatile Inkjet

## 2 Printed HfO<sub>2</sub>-based ReRAM: from Device to

## 3 Nanoscale Characterization

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- 14 KEYWORDS:
- 15 Inkjet Printed ReRAM, high-k HfO<sub>2</sub>, cost-efficient technology, high-performance Resistive
- 16 Switching, TEM.

ABSTRACT: Low-power high-performance metal-insulator-metal (MIM) non-volatile resistive memories based on HfO<sub>2</sub> high-*k* dielectric are fabricated using drop-on-demand inkjet printing technique as low-cost and eco-friendly method. The characteristics of resistive switching of Pt (bottom)/HfO<sub>2</sub>/Ag (top) stacks on Si/SiO<sub>2</sub> substrates are investigated in order to study the bottom electrode interaction with the HfO<sub>2</sub> dielectric layer and the resulting effects on resistive switching. The devices show low Set and Reset voltages, high ON/OFF current ratio and relatively low switching current (~1 μA), which are comparable to the characteristics of current commercial CMOS memories. In order to understand the resistive switching mechanism, direct structural observation is carried out by field-emission scanning electron microscopy (FE-SEM) and high-resolution transmission electron microscopy (HRTEM) on cross-sectioned samples prepared by focused ion beam (FIB). Electron energy loss spectroscopy (EELS) inspections discard a silver electro migration effect.

The increasing demand for flexible, wearable and transparent devices has been stimulated by the irruption of the Internet-of-Things (IoT), where electronic applications are, at any time and everywhere, responsive to and communicating with the whole environment by means of a wireless network. <sup>2</sup> Considering the horizon of IoT and the existing requirement for pervasive computing and sensing, the low-cost manufacturing of low-power consumption electronic objects, as well as the properties of flexibility and/or wereability, can be achieved by means of printing technologies.<sup>3-5</sup> During the last decade, printing processes have progressed from a design and patterning technique to highly-precise and scalable solutions for the deposition of disrupting materials for low-cost electronic applications onto a large-area flexible substrate.<sup>4-8</sup> The strong development of rising printing technologies, like inkjet printing, is providing new opportunities to cheaply fabricate electronic devices and circuits. 9,10 Despite its low device performance when compared to conventional CMOS parameters, 11 inkjet-printing exhibits increased potentiality when applied to the development of non-volatile memory (NVM) elements for data storage. 12,13 Amongst the existing NVM technologies that have been proposed to date, phase-change random access memory (PCRAM), <sup>14</sup> ferroelectric RAM (FERAM) <sup>15</sup> or magnetoresistive RAM (MRAM)<sup>16</sup> have demonstrated to fulfill the general performance requirements for memory devices.<sup>17</sup> In addition, several two-terminal small-size resistive random access memory (ReRAM) devices have become a disruptive technology because of their simplicity and outstanding compatibility with the CMOS manufacturing technology. 18 So far, a wide range of materials exists that are suitable building blocks for memory applications, such as organic insulators (mainly polymers),19 graphene oxide,20 amorphous silicon,21 chalcogenides (selenides and tellurides),<sup>22</sup> carbon nanotubes,<sup>23</sup> perovskite oxides,<sup>24</sup> and binary transition metal oxides.<sup>25</sup> Critical parameter specifications, common to all the mentioned

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1 materials, are: write and read switching speeds, high-to-low resistance ratio, power consumption, 2 endurance, and data retention time and simultaneously being a very cost effective solution. 26,27,28,29 In particular, ReRAMs based on HfO<sub>2</sub> have been deeply studied and proved as 3 a suitable material for memory devices. 30-33 4 5 In this article, an inkjet-printed HfO<sub>2</sub>-based ReRAM, which exhibits very high-performance and 6 low-power consumption in addition to self-compliance current, is presented and characterized 7 from device level to nanoscale structure, respectively by means of electrical measurements and 8 direct microscopy observation. The switching mechanism and the effect of the electrode material 9 and its implications on the device features are analyzed in detail. These promising characteristics 10 make these inkjet-printed ReRAM devices as good candidate for portable and flexible systems. 11 Results. The metal-insulator-metal (MIM) structures under study were fabricated onto oxidized 12 Si (Si/SiO<sub>2</sub>) substrate. Ag and HfO<sub>2</sub> inks were used to inkjet-print, respectively, the top electrode 13 and the dielectric layer on top of a previously sputtered Ti/Pt bottom electrode. The resulting 14 Pt/HfO<sub>2</sub>/Ag MIM stack is sketched in Figure 1a, and a field-emission scanning electron microscope (FE-SEM) cross-sectional image of such a ReRAM device is presented in Figure 1b, 15 16 evidencing the proper layer stacking as nominally expected. As revealed by our previous study,<sup>34</sup> 17 the as-printed HfO<sub>2</sub> layer appears as a series of nanoparticles (NPs), sphere-shaped with average diameters of ~25 nm, forming a uniformly-deposited polycrystalline layer. Atomic Force 18 19 Microscopy measurements (Fig. 1c) demonstrated that de resulting HfO<sub>2</sub> layer has a Root Mean 20 Square (RMS) roughness of 25 nm, compatible with previous measurements. <sup>34</sup> This roughness

of the oxide-electrode interfaces affects the microstructure of the oxide and provides defect-rich

sites where vacancy formation and oxygen ion mobility can be enhanced, which results in

favorable switching properties.<sup>35</sup> Once the adequate layer deposition was assessed, the resulting

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devices were electrically tested. For this, a measurement protocol was designed. First of all, to build up the experiments, the devices were stressed to determine the voltage polarity when the RS process occurs and current ranges that must be withstood when operating. In particular, a preliminary characterization of the devices has shown that, when positive voltages are applied to the top terminal, a Forming/Set process was obtained; in contrast, the Reset process was only achieved once negative voltages were applied. The Forming process can be achieved applying negative bias at the top electrode of a pristine device, but in this case no Reset process is observed for both, negative or positive bias. Then, a current compliance (1 µA) was fixed to avoid permanent breakdown, thus allowing the secure application of the proper voltage bias required to promote the resistive switching phenomenon. A positive voltage was then applied to the silver top electrode, in order to induce the electroforming process that means the conductive filament (CF) formation for the first time. 14,36 The creation of a CF through the dielectric layer 14 determines a low resistive state (LRS) between top and bottom electrodes. Afterwards, reversing the applied voltage polarity (Reset) without any current compliance protection leads to a high resistive state (HRS), which is due to the partial or total disruption of the previously formed CF into the dielectric. Finally, the implemented procedure to program (write) the memory devices consisted of inducing the cyclic creation (Set, by positive voltage ramps, usually lower than the required voltage for the electroforming) and dissolution (Reset, by negative voltage ramps) of CFs. As an application example of the abovementioned measurement protocol, Figure 1d plots two consecutive current-voltage (I-V) curves (randomly selected from a set of highlyreproducible measurements) from an inkjet-printed memory device, after electroforming was carried out. The *I-V* measurements exhibit a typical bipolar resistive switching feature. 14,37 On one hand, for positive voltages (Set process, blue lines in the figure) the current compliance,

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- 1 fixed at 1 μA, is reached around 0.1 V. On the other hand, without any current limitation, for
- 2 negative voltages (Reset process, red lines in the figure) a current around 1 mA (IoN) at -0.05 V
- 3 is registered, corresponding to the LRS state (ON state). When the negative voltage ramp reaches
- 4 -0.1 V, the large current immediately descends to  $\sim$ 5 pA ( $I_{\rm OFF}$ ), around 9 orders of magnitude
- 5 lower, indicating that the sample has switched to the HRS state (OFF state).

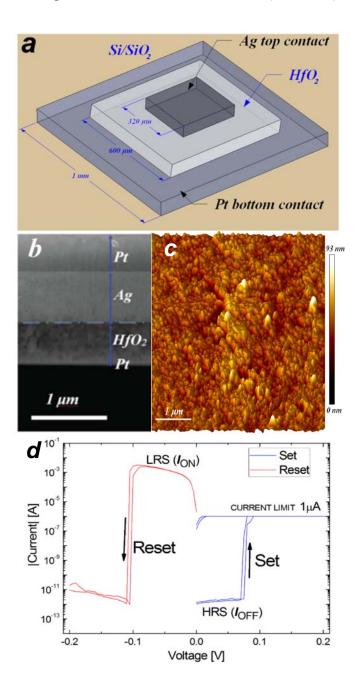
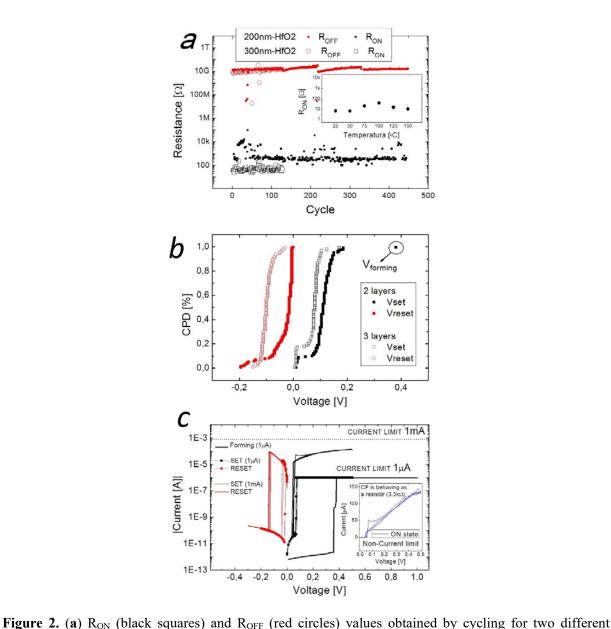


Figure 1. (a) 3D sketch of the HfO<sub>2</sub>-based ReRAM devices. (b) Cross-section image obtained by FIB-1 2 assisted FE-SEM. The structure consists of a thin Pt bottom electrode (50 nm) on top of a Si/SiO<sub>2</sub> 3 substrate, followed by a 300-nm-thick HfO<sub>2</sub> dielectric layer and a 700-nm-thick Ag top electrode. An 4 extra Pt layer is deposited on top of the overall structure as a requisite of FIB sample cutting. (c) 5 6 Topographical image obtained by AFM of the HfO<sub>2</sub> layer deposited by inkjet-printing. (d) Representative Bipolar Resistive Switching I-V curves of two consecutive cycles measured on an inkjet-printed ReRAM 7 device. The current compliance limit is established at 1 µA to ensure avoiding the permanent breakdown 8 of the dielectric. Blue and red lines correspond to the Set and Reset processes, respectively. 9 The described experimental sequence of consecutive Set and Reset processes was applied in 10 several devices containing two different inkjet-printed HfO<sub>2</sub> layer thicknesses (200 nm and 300 11 nm), in order to find the optimum device structure for reliable and low-consumption memory 12 devices. With this aim, the  $I_{\rm ON}/I_{\rm OFF}$  current ratio and the  $V_{\rm Set}$  - $V_{\rm Reset}$  voltages switching 13 parameters were analyzed in detail as function of the dielectric thickness. 14 Figure 2a shows the resistance value obtained by cycling in the same sample of the ON state (squares) and OFF state (circles) measured at 0.01 V (in absolute value) during 512 cycles for 15 16 the memory device based on inkjet-printed 200-nm HfO<sub>2</sub> layer. As can be observed in the case of 17 the 200-nm-thick dielectric, both ON (LRS, black solid squares) and OFF (HRS, red solid 18 circles) are highly stable, mainly exhibiting narrow relative dispersions and within the same 19 order of magnitude. However, the ON state presents a higher relative dispersion than the OFF state one, in opposition to the typical RS current distributions. 14 The high stability for current 20 21 values larger than 100 µA of the ON state could be attributed to a very stable Set process in 22 combination of the applied current limitation (1 µA in the measurements shown in Figure 2a), 23 indicating a very repetitive filament formation by cycling. In the case of a memory cell based on 24 a 300-nm-thick HfO<sub>2</sub> layer (Figure 2a), under the same measurement conditions, both states 25 present more stable values, especially for the ON state (empty black squares), but also for the OFF one (empty red circles). Moreover, whereas OFF states currents are comparable in both 26 27 measured samples (red empty and solid circles), the mean current values of the ON state differ 28 about one order of magnitude while maintaining stable values. The inset of figure 2a shows the

- ON Resistance value as a function of temperature (ranged from 25 to 150°C and measured at
- 2 50mV) in order to analyze the nature of the switchable filament.
- 3 Analogous analysis was carried out of V<sub>Set</sub> and V<sub>Reset</sub>. Figure 2b shows the Set (black squares)
- 4 and Reset (red circles) voltage CPDs obtained for the same samples. The programming voltages
- 5 ranged from -0.2 V to 0.2 V, resulting in a very low power supply (power consumption  $< 1 \mu W$ )
- 6 required for these resistive switching devices in comparison to consolidated CMOS-based
- 7 ReRAM technologies.<sup>17</sup>
- 8 As also observed for ON/OFF resistance values, the device containing a 300-nm-thick HfO<sub>2</sub>
- 9 layer presents, for both Set and Reset voltage distributions, stable and reliable values around 0.1
- 10 V (in absolute value). For the memory device with a 200-nm-thick dielectric layer, the Set
- voltage distributions have larger values, whereas the Reset voltage distributions show a larger
- 12 dispersion.
- 13 Despite the low power consumption achieved, in order to avoid using an on-chip transistor
- during the Set process, ReRAM devices should be controlled by a self-compliance current to
- ensure resistance switching and the decrease of the total energy consumption. For this reason, the
- 16 impact of the current compliance value was evaluated, to determine whether the inkjet-printed
- memory cells exhibit a self-compliance current phenomenon during the Set process.
- Figure 2c shows the I-V characteristic curves of a different 300-nm-thick HfO<sub>2</sub> memory cell than
- 19 figures 2a and 2b, which was switched during the first 50 cycles by employing a safety current
- 20 limit of 1 µA (black squares), whereas the compliance limit was increased to 1 mA for the
- 21 following cycles (black lines). With this methodology, when the compliance was increased to 1
- 22 mA, the current intensity across the dielectric layer reached a self-compliance current of about
- $\sim 100 \,\mu\text{A}$ , thus resulting in a low power consumption of  $\sim 10 \,\mu\text{W}$ . The resulting CF becomes

stronger than under external current-limited conditions, consequently exhibiting higher current values during ON state, whereas the OFF state remains unchanged. Moreover, the effect of the new conditions during filament formation increases the power needed to disrupt the CF (higher Reset voltages in Figure 2c) and promotes its reopening (lower Set voltages). I-V curve of the forming process is also shown in figure 2c (black thick line).



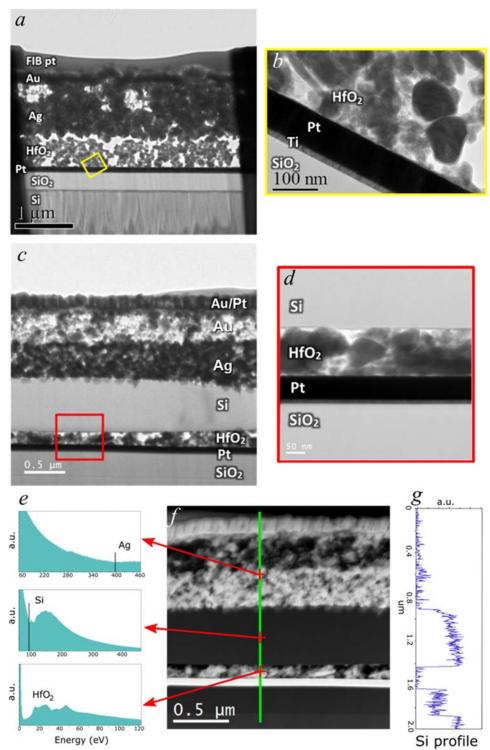
samples with an HfO<sub>2</sub> dielectric layer thickness of 200 nm (full symbols) and 300 nm (open symbols). Inset in figure 2a shows the temperature dependence of the ON state resistance. (b) Set (black squares) and Reset (red circles) voltage distributions for the same samples in (a). (c) I-V curves of the Resistive Switching observed in a 300-nm-thick HfO<sub>2</sub> sample, where after 50 cycles the current limitation is increased from 1  $\mu$ A (four consecutive cycles are plotted by solid symbols) to 1 mA (four consecutive cycles are plotted by lines). The forming process is also plotted (black thick line). The inset in figure 2c shows the resistive behavior of the device, 3.3 k $\Omega$ , which takes into account both the resistance value of the CF and the series resistance.

Generally, the self-compliance current limit might be caused by the generation of internal resistance in series with the ReRAM resistance, which can be observed in the inset of Figure 2c as a linear dependence after SET (blue lines).<sup>38</sup> In the sample shown in Figure 2c, the equivalent

1 resistance of the ReRAM device plus the series internal resistance is around 3.3 k $\Omega$  and seems to 2 be very repetitive by cycling, in agreement with the stable current values during the ON state. 3 In order to establish a correlation between the structural arrangement taking place within the 4 dielectric layer and the consequent electrical switching mechanism of the inkjet-printed ReRAM 5 devices, Scanning Electron Microscopy (SEM) and Transmission Electron Microscopy (TEM) 6 characterization of the devices was carried out, starting by the assessment of the thickness and 7 composition of the layers in pristine devices. Inspections by SEM of pristine samples reveal no 8 unexpected features in the sample surface. Figures 3a and 3b show HRTEM images of the inkjet-9 printed ReRAM device with a Pt layer bottom electrode thickness of 80 nm and a Ti layer 10 thickness of 17 nm, the 300-nm-thick HfO<sub>2</sub> layer, and the 700-nm-thick top electrode layer of Ag 11 on the Si/SiO<sub>2</sub> substrate. Then, after the electroforming process and several Set-Reset switching cycles, SEM images of the memory cell (Figure S1a) were acquired that present clear randomly-12 13 distributed bubble-like features with diameters of ~1 µm. Actually, these sort of features, 14 typically observed in ReRAM devices, are usually attributed to oxygen diffusion during the Set-15 Reset cycles.<sup>39</sup> 16 In order to study the nature of these bubbles in our samples, a TEM lamella was prepared by 17 Focused Ion Beam (FIB) in that particular feature, cutting the whole region slice-by-slice, using 18 simultaneous SEM observation until a CF became visible (Figures S1b and S1c). Figures 3c and 19 3d show the TEM images of the memory cell controlled by self-current compliance, whereas 20 Figure 3e displays the corresponding electron energy loss spectroscopy (EELS) results. 21 Remarkably, as can be observed in the figure, the changes in the morphology of the devices (i.e., 22 the presence of bubble-like features) are due to the presence of Si clustering (agglomeration) at 23 the top Ag-HfO<sub>2</sub> interface. No evidence of Ag electromigration was detected.

Yang *et al.* demonstrated enhanced switching uniformity and stability in TiO<sub>2</sub>-based ReRAM due to the diffusion of the underlying Ti through the Pt bottom electrode, which in turn reacted with the metal-oxide layer, consequently generating oxygen vacancies (Vo) in the dielectric film.<sup>36</sup> In our case, Si diffusion is detected instead of Ti one. This phenomenon also enhances the uniformity of the RS and the stability of the ReRAM. On the contrary, as demonstrated in the past by using an Au electrode instead of Ti/Pt, no Si diffuses through the HfO<sub>2</sub>,<sup>40</sup> the current distributions become therefore less uniform (Figure S2) and in some cases the ReRAM can be damaged by the excess of O ions (formation of O<sub>2</sub> bubbles due to high temperature)<sup>36</sup> at the Ag-HfO<sub>2</sub> interface (Figure S3). The lack of Ti diffusion can be explained by the annealing temperature used to deposit the inks, usually around 200 °C, whereas Ti diffusion only takes place when annealing the Ti/Pt electrode at a temperature above 600 °C.<sup>41</sup> Moreover, the generated Si interlayer seems to be the material that acts as a series resistance to the CF generated from the V<sub>0</sub>-type defects, thus promoting the controlled self-compliance.

**Discussion.** The inkjet-printed memory cell consists of an electrochemically active electrode (Ag, top electrode), a reducible transition metal oxide layer (HfO<sub>2</sub>) and an inert (not electrochemically active) electrode (Pt). In such a structure, the HfO<sub>2</sub> stoichiometry plays an important role.<sup>42</sup> In our device, the estimated ratio O:Hf is ~1.85,<sup>34</sup> thus resulting in oxygen deficiency; in turn, this leads to a high concentration of oxygen vacancies within the dielectric layer.



**Figure 3.** (a) TEM image of the pristine inkjet-printed ReRAM device; (b) high magnification HRTEM image from the yellow square in (a); (c)TEM image of the biased ReRAM device; (d) high magnification HRTEM image from the red square in (c); (e) single spectra from the Ag layer (M4,5 edge of Ag at 367 eV), the Si precipitate (L2,3 edge of Si at 99 eV) and HfO<sub>2</sub> layer (plasmon energy of HfO<sub>2</sub> at 15.5 eV), as indicated with red arrows in (f); (f) STEM image of the biased sample with Pt electrode; (g) Si intensity profile along the highlighted line in (f).

It has been recently reported that transport through highly-defective HfO2 may take place via trap-assisted tunneling, 43 in which carriers are injected from the electrode into the dielectric, tunneling through its inner electronic states until reaching the opposite electrode. Nevertheless, although this mechanism is plausible taking into account the material characteristics, tunneling is strongly dependent on both the dielectric/metal band offsets and the applied electric field. In fact, at the low electric fields employed, other mechanisms may become more favorable. In particular, in wide-band gap materials with a high density of intrinsic defects, such as HfO2 or ZrO2, 32,44,45 charge transport usually takes place via thermally-activated charge hopping through intra-band gap allowed (defect) states, 46 the so-called Poole-Frenkel mechanism. 44 In any case, within the frame of both proposed mechanisms for the HRS, the randomly distributed Vo near the grain boundaries of the polycrystalline inkjet-printed HfO247,48,49,50 are responsible for the very low currents registered in pristine state of the memory cell. It should be mentioned here that the electroforming voltages are extremely low in comparison to thinner HfO<sub>2</sub> layer obtained by CMOS-standard processes.<sup>15</sup> This may be due the large amount of defects (oxygen vacancies) present in the layer due its stichometry [Bradley, Dai] or generated by the roughness present in the oxide-electrode interfaces, that increases the vacancy formation. <sup>35</sup> Moreover, its relatively high roughness could lead to the formation of nano-pits, that together with the high porosity of the layer, could reduce ever more the electroforming voltage. Given the current level difference between HRS and LRS states (about 9 orders of magnitude), the transport mechanisms taking place within every state must necessarily differ, which obeys to a structural modification of the film when Reset state is switched into Set. As we did not find evidence of Ag electromigration, metal filamentation could be ruled out. This hypothesis is compatible with the information obtained from the measurement of the ON Resistance with

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Temperature (inset Fig. 2a). Note that R<sub>ON</sub> is not dependent on the temperature, which implies that defect conductive filaments are dominant in the device<sup>51,52,53</sup>. Therefore, although further experiments are necessary to strengthen our hypothesis, we suggest that the switching mechanism could be driven by the oxygen vacancies migration. Assuming this assumption, the increase in the positive voltage induces the loosely-bound oxygen ions in lattice positions (as a consequence of the breakage of the metal-oxygen bonds, Hf-O) to diffuse towards the Ag top electrode. This ionic diffusion leads to the creation of new oxygen vacancies (generated from the released O ions, causing a change of the inkjet-printed film stoichiometry) that randomly accumulate close to the inert Pt bottom electrode. When the applied voltage stress overcomes a critical threshold for the dielectric layer, the Vo defects reach a local density that promotes the formation of a CF through the whole dielectric thickness.<sup>42</sup> Therefore, a current, flowing preferentially at the grain boundaries, <sup>48,49,50</sup> switches the memory device from pristine state to the LRS. Under this state, the vertical arrangement of oxygen vacancies (i.e., the CF) can be seen as a quasi-continuum of (defect-related) electronic allowed levels. Since the high Vo density dramatically reduces the inter-state distance, trap filling is not achieved (i.e., constant charge flow is possible), carrier transport probability through the CF thus increases, and either trapassisted tunneling or thermal hopping no longer apply. Instead, one can see the new set of electronic states as a mini-band settled deep within the HfO2 band gap, through which quasi-Ohmic transport takes place.<sup>41</sup> The structural modification cycle ends during the Reset process, when the applied negative voltage drives back the oxygen ions from the top electrode to the inert bottom electrode. In this case, as the maximum current flows through the CF, the diffused-back O2- anions randomly fill previously-formed Vo within the CF crystalline sites. Once this stochastic total re-oxidation of

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the CF occurs, <sup>40</sup> the memory device switches from LRS to the HRS due to the abrupt increase in the electrode/dielectric barrier height, and again purely dielectric-based mechanisms govern charge transport. Indeed, for the 200-nm-thick devices, from a structural point of view, higher current dispersion observed during the ON state may account for the continuous creation of new paths during the CF formation resulting from the random Vo defects distribution. Hence, when a specific CF path prevails over other ones not yet completely formed, a stable current distribution is registered. During the OFF state, only certain conduction paths through defect states are allowed, irrespective of the applied electrical field. When increasing the dielectric layer thickness to 300 nm, the length of the filament obviously increases, which is more likely to present a larger section (lower amount of alternative conduction paths), and thus higher current and narrower CPD distributions are expected. The results reported and discussed so far suggest that thinner dielectric layers, i.e., shorter conduction filaments, are more prompt to form weak CF at low applied voltages, which might negatively affect the RS cycle, and thus the overall device performance. Therefore, it is plausible to state that, since there seems to be a direct correlation between structural CF stability and the reliability in the switching process between HRS and LRS, thicker dielectric layers (300 nm), HfO<sub>2</sub> in the present study, become better candidates as memristive material in operational ReRAM devices.

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Conclusions. To summarize, resistive switching properties of inkjet-printed ReRAM devices with a simple stack structure of Pt (bottom)/HfO<sub>2</sub>/Ag (top) have been investigated. The devices have shown excellent switching cycle uniformity and stability, with a low-voltage operation at  $\pm 0.2$  V and an  $I_{ON}/I_{OFF}$  ratio of about  $\sim 10^9$ . Furthermore, the memory cells exhibit a self-compliance current ( $\sim 100 \, \mu A$ ) during the Set process, allowing a low Set power consumption up

to  $\sim \! 10~\mu W$ , while maintaining a higher stability (in terms of current and operating voltages) than the measurements with external current limit. Electron microscopy techniques were used to directly observe the structure and morphology of the memory stack. Since Ag has not been observed in the locations were CF were created, we suggest that the resistive switching mechanism could be related to the formation of oxygen vacancy-based conductive filaments through the HfO2 layer. Moreover, the Si electromigration observed could be the responsible for the self-compliance and stability of the ReRAM. Finally, the results hereby reported suggest that thicker dielectric layers (300-nm-thick in our study) provide higher stability during the resistive switching process.

Experimental Section. *Material deposition*. The sample fabrication was carried out by means of a Fujifilm Dimatix DMP 2831 (Japan) inkjet printer, equipped with cartridges with a droplet volume of 1 pL and 10 pL, respectively for conductive ink and 2D materials. Two types of inks were used to inkjet-print the final MIM structure: a conductive Ag-nanoparticles (NPs)-based ink and HfO<sub>2</sub> NPs ink as high-*k* dielectric (Torrecid S.L.). Contact leads were printed using Ag NPs-based ink from Advanced Nano Product (DGP-HR, 30% w/w). Further details on the HfO<sub>2</sub> NPs ink formulation and printing can be found elsewhere.<sup>34</sup> *ReRAM MIM structure fabrication*. The ReRAM MIM devices were fabricated on top of oxidized Si (Si/SiO<sub>2</sub>) substrates. First, a Pt thin film (50 nm) was deposited as bottom electrode by sputtering on a Ti layer (15 nm). Afterwards, an HfO<sub>2</sub> NPs-based layer (each sample containing a different thickness) was selectively printed over the bottom electrode covering an area of 0.1 mm<sup>2</sup>, while keeping the substrate temperature constant at 30 °C. A post-deposition annealing process at 240 °C for 3 h was then carried out in a vacuum furnace, to ensure the elimination of solvents. Finally, a 300-nm-thick Ag electrode was

- 1 printed on top of the structure. Structural characterization. FE-SEM and TEM were performed
- 2 on the cross-section of the fully-printed devices, which were cut for this purpose by focused ion-
- 3 beam (FIB CrossBeam 1560XB, Zeiss). After the FIB cross-section cut, the samples were
- 4 analyzed by high-resolution field-emission variable-pressure (VP) SEM (Zeiss 1555 VP-
- 5 FESEM). X-ray microanalyses were performed using an Oxford Instruments X-Max 80 silicon
- 6 drift EDS system employing the AZtec and INCA softwares. TEM lamellas were prepared by
- 7 FIB (CrossBeam 1560XB, Zeiss, operated at 30 kV) using the lift-out technique. An in-depth
- 8 analysis based on HRTEM and scanning TEM (STEM) imaging was carried out in a Jeol 2010F
- 9 TEM operated at 200 kV coupled to a GIF Gatan filter. Chemical analysis was performed with
- 10 the same instrument in STEM mode for EELS studies. *Electrical measurements*. The current
- versus DC voltage characteristics were measured by a Keithley 4200 Semiconductor Device
- 12 Analyzer that allows the automation of maximum 128 cycles of the measurement sequence. For
- 13 the acquisition of transport data, the devices characterization was carried out at room temperature
- 14 ( $\sim$ 24 ° C) using a four-probes configuration.
- 15 ASSOCIATED CONTENT
- 16 **Supporting Information**. Additional information and figures about memory devices analyzed
- by SEM and TEM microscopies. The following files are available free of charge.
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#### 2 Author Contributions

- 3 The manuscript was written through contributions of all authors. All authors have given approval
- 4 to the final version of the manuscript. \*G.V. and \*A.C-Y. contributed equally to this work.

#### 5 Notes

6 The authors declare no competing financial interest.

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#### 8 ACKNOWLEDGMENTS

- 9 G.Vescio acknowledges the Spanish Government for his PhD grant in the FPU program. UAB
- authors acknowledge funding from the Spanish MINECO and ERDF (TEC2013-45638-C3-1-R)
- and the Generalitat de Catalunya (2014SGR-384). A. Cirera acknowledges financial support
- 12 from the Spanish MINECO (MAT2015-66443-C2-2-R).

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