DC characterization and small signal modelling of organic thin film transistors with different geometries

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***Abstract*— Organic Devices offer low-cost manufacturing and better flexibility, sustainability and solution-processability than their Si-based MOS counterparts, which make them suitable for new applications where those characteristics are an advantage. However, organic device performance is still far from that provided by CMOS technology and many issues are still unclear. In this work, a performance comparison of Interdigitated and Corbino geometries of Organic Thin Film Transistors (OTFT), with different areas but fabricated with identical stack materials and techniques, is done. With this purpose, I-V characteristics and C-V curves of the OTFTs were measured and a Common-Source circuit was proposed and implemented for extracting relevant electrical parameters of the devices, through a standard small signal analysis. The parameter extraction methodology in the frequency domain proposed allows rapid testing of the device/circuit performance of this technology, which is for the first time applied to organic devices. Results show that organic transistors exhibit similar channel dimensions dependencies as MOS devices, despite the large voltages, and can be also described by the same small signal model.**

Organic Thin Film Transistor (OTFT), Corbino Thin Film Transistor (CTFT), Organic Electronics, Capacitance-Voltage, DC characterization, small signal model.

I. Introduction

Organic Electronics (OE) is one of the most promising technologies for the fabrication of new smart and flexible electronic systems [1]. Thanks to the diverse fabrication techniques that it comprises [2]–[5], this technology allows the use of flexible substrates and novel solution-based materials, in new smart systems in different fields such as Radio Frequency Identification (RFID) tags, disposable sensors, flexible displays or functional circuits [6]–[8]. These systems can be instant made, fully additive, low temperature processed, lightweight, bendable, scalable and sustainable, all of this combined with low-cost manufacturing. These new features enable wearable and disposable electronic systems, unfeasible for the moment with the traditional silicon technology. However, more investigations are still needed to analyze the performance of different architectures and to develop suitable models. To evaluate the properties of Organic Thin Film Transistors (OTFT) some works analyze and model their DC behavior through different parameters such as Threshold Voltage, Mobility or Driving Current, and also the Operating Voltages, which are much larger than for MOSFETs [9]. Other works analyze the frequency response of OTFTs through the measurement of S-parameters in isolated devices [10]. Moreover, some functional circuits could be used to study the OTFT performance and their response in the frequency domain, since the circuit frequency response (gain and cut-off frequency) mainly depends on the transistor parameters. Then, this work takes advantage of this dependence in a Common-Source (CS) amplifier to experimentally study the performance of Organic Thin Film Transistors (OTFT) with different architectures and areas fabricated with an already patented and commercial technology [11]. Device level measurements are also carried out, for comparison. Special emphasis is done on their frequency response related parameters, i.e., the role of the dielectric stack capacitance was analyzed in detail, for its inclusion in a small signal model. This novel methodology allows a fast extraction of device performance parameters, through the modelling of the frequency response of the test circuit. The method has been applied to the characterization of OTFTs, which operates far afield from CMOS devices.

II. Samples and Experimental Setup

Two different architectures of Organic Thin Film Transistors have been studied: 1) Interdigitated fingers for the source and drain terminals (OTFT), and 2) Corbino [12] OTFT (CTFT) with a cylindrical shape (see Figure 1A and B, respectively). The devices are fabricated by NeuDrive Ltd. (UK) [13], using gold contacts, Cytop™ as a dielectric and proprietary organic p-type semiconductor FlexOS™ [14]. The fabrication process combines sputtering, spin coating and photolithographic steps. The cross section of the OTFT (Fig. 1A) and CTFT (Fig. 1B) are presented together with the stack of materials in Figure 1C.

The Interdigitated OTFTs processed by NeuDrive present the classical interdigitated geometry, where source and drain are interleaved behind the gate. This geometry allows easy scalability since different widths can be achieved by using multiple fingers. Two different interdigitated channel lengths were used, 10µm and 4µm. For the 10µm length devices, two widths were studied: 980µm and 9800µm. For the 4µm channel length devices, five widths were studied: 160, 320, 640, 1280 and 2560µm using two different finger widths. For the Corbino OTFT, four different channels lengths (5, 10, 20 and 40µm), combining three different external radius R_2 (105, 100 and 120µm) with two internal radiuses R_1 (100 and 80µm) were studied [15].

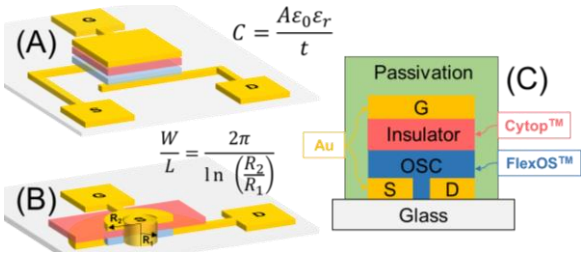

Fig. 1. Architecture of the (A) Interdigitated OTFT, and (B) Corbino OTFT. (C) OTFT Stack materials, common to both architectures.

I-V and C-V curves of the devices were measured with the Semiconductor Parameter Analyzer Keithley 4200, which allows large current and capacitance resolution measurements with high voltage biasing (±30V). The frequency response of the Common-Source amplifiers built with the studied OTFTs was determined by measuring the amplitude of the output voltage, when the frequency of the input signal was swept from 100Hz to 1MHz. General-purpose digital scope was used for the output signal measurement.

III. Device Characterization

To evaluate the device performance, I-V characteristics and C-V curves were measured on the devices with different architectures and dimensions. Figure 2 shows typical Drain Current – Gate Voltage (I_D-V_G) characteristics of all of them. As can be seen, subthreshold region is located at voltages above 0V, implying that these devices (p-type transistors) are operating in depletion mode [16]. Off currents are of the order of pA in most of the cases, meaning a low consumption when the device is off (Fig. 2). Note that, when device is on, currents in the ~100µA-1mA range are achieved with mobilities between 1 to 1.75 $cm^2/V{\cdot}s$, under operating voltages around ±30V [17]. These voltages are much larger than in CMOS technology (~0.8V) [18], but usual in organic devices [19].

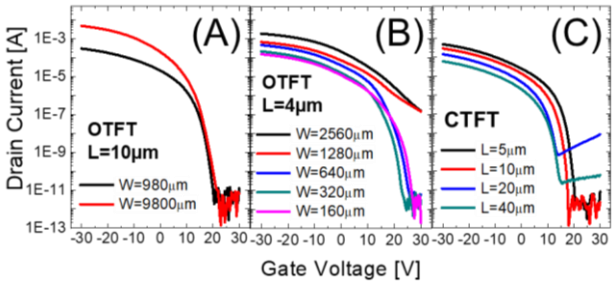

Fig. 2. Drain Current–Gate Voltage characteristics measured on Interdigitated OTFT with (A) L=10µm, (B) L=4µm and (C) Corbino OTFT.

For the interdigitated OTFTs, I_D increases as expected, linearly with device width (Fig. 3A). Contrarily, for the Corbino architecture, an I_D reduction is observed (Fig. 3A), because device width and length, change with the radiuses as well ($L=R_1-R_2$). However, when representing I_D as a function of device aspect ratio, in both cases, Interdigitated and Corbino, it is proportional to W/L (Fig. 3B). To evaluate the dependence of V_{th} on the device area, as a criterium, V_{th} was defined as the gate voltage at which I_D=10µA. Figure 3C shows that V_{th} of Interdigitated devices grows linearly with the device width, while in the Corbino it decreases with the channel length. Note that I_D and V_{th} follow the same geometry scaling dependence that MOS technologies [20].

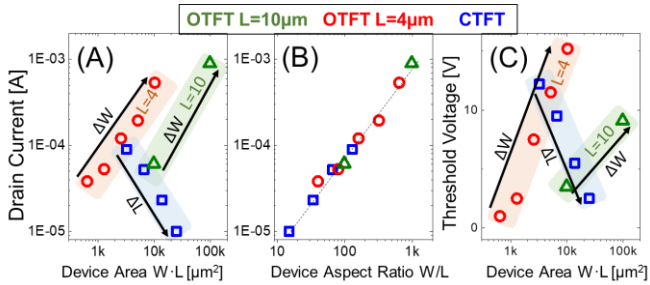

Fig. 3. I_D as a function of (A) the device area for OTFT and CTFT and (B) as a function of the aspect ratio W/L. (C) V_{th} as a function of device area.

The parasitic capacitances associated to the stack were also measured (C-V curves) in the same devices. The gate capacitance (Cox) was measured when source and drain were grounded (similar values to those measured on MIM structures were obtained for the capacitances per unit area, $5{,}94{\cdot}10^{-5}$F/m) C_{GD} and C_{GS} were also measured, with the drain or source terminals grounded, respectively, while the other terminal is kept floating. A strong dependence of the measured capacitance with the device area is observed (Fig. 4) for the two OTFTs architectures. The inset in Figure 4A shows that, for negative polarities, the three capacitances (C_{OX}, C_{GS} and C_{GD}) are almost equal, indicating that the channel region acts as a bottom terminal of the stack when device is ON (accumulation of p-type carriers). In the case of CTFT devices, capacitance increases with device area (i.e. channel length decreases) when applying positive bias (subthreshold region). This dependence is observed because, in that regime, the area of the capacitance depends only on the overlapping between the gate and drain-source electrodes. However, at negative bias, CTFT capacitance exhibits similar values for different areas, because the effective area under the gate terminal is the same due to the effect of the channel (i.e. gate metal electrode does not scale with device area). Therefore, their cylindrical architecture implies a L-independent gate area when CTFT device is ON.

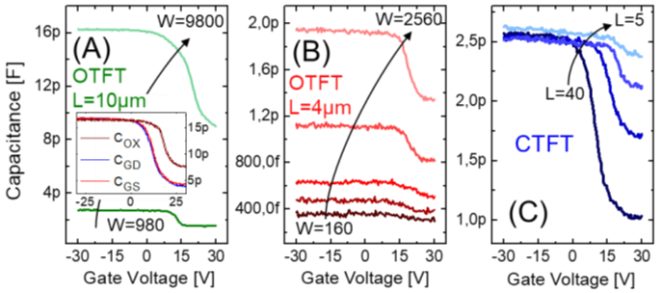

Fig. 4. C-V characteristic of the Gate stack for the interdigitated OTFT with (A) L=10µm, (B) with L=4µm, and for (C) Corbino OTFT. The inset in (A) shows the area dependence of the three measured capacitances.

IV. Frequency Response and Small Signal Model

In order to evaluate the performance of the studied OTFT and CTFT, a Common Source (CS) amplifier is used [21], which allows easy correlation of device and circuit performances, because the amplifier's gain and cut-off frequency strongly depend on the transistor parameters [22]. This configuration is represented in Figure 5A and the corresponding small signal equivalent circuit in Figure 5B, where a MOSFET-like small-signal model is considered for the OTFT. Circuit analysis leads to a transfer function given by equation 1, which shows that the CS circuit gain depends on the transconductance (g_m) and output resistance of the transistor (the last one included in R_{OUT}, which is defined as $R_{OUT}= r_0//R_D//R_{OSC}$). In addition, the cut-off frequency is determined by the parasitic Gate-Drain capacitance (C_{GD}), being independent of C_{GS}. These parameters can be extracted from |H(s)| measurements. In our experiments, the value of R_{SS} (the output resistance of our input source), R_{G1}, R_{G2}, C_S, R_{OSC} and C_{OSC} (being the last one the input impedance of our scope) and the DC voltage supply, V_{CC}, were fixed. It must be emphasized that, in these experiments several parameters change from experiment to experiment (i.e. when a different device area or geometry are used, different voltages at device terminals are registered), thus direct comparisons are meaningless. Moreover, circuit values such as R_D or V_x were selected in order to maximize the gain. Then, to account for the differences in the OTFTs, R_D valued could vary between 340kΩ and 1MΩ. V_{GS} and V_{DS} DC values were registered before extracting the frequency response, to assure the transistor operating point. A frequency sweep of the input signal was performed from 100Hz to 1MHz. Only the mid and

high frequency regimes were analysed, since low frequency response is mainly given by the circuit parameters.

$$H(S) = \frac{V_{OUT}(S)}{V_{IN}(S)} = \frac{R_{OUT}C_{GD}S - gmR_{OUT}}{S(C_{OSC}+C_{GD})R_{OUT}+1} \qquad \text{Eq. 1}$$

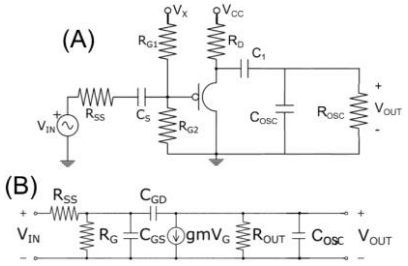

Fig. 5. (A) Common Source (CS) amplifier implemented to evaluate the OTFT performance in the frequency domain, and (B) small signal model for mid and high frequency regims. R_G=R_{G1}//R_{G2} and R_{OUT}= r_0//R_D//R_{OSC}.

Figure 6 shows the magnitude of the frequency responses of the CS amplifiers built with the different Organic transistors, measured (lines) and their fitting to eq. 1 (circles). As observed, the gain increases with the device width and in the best case it is ~6dB. The cut-off frequency also increases with the device width. In addition, the effect of the transmission zero (given by C_{GD}) in eq. 1 is clearly observed in the 100kHz-1MHz interval.

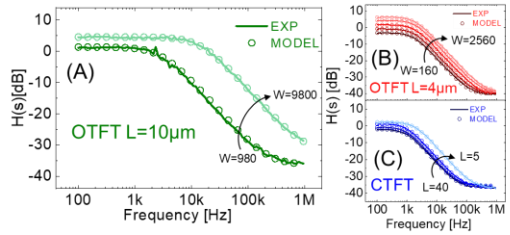

Fig. 6. (A) Experimental (lines) and fitted (circles) frequency response for the Interdigitated OTFT with L = 10 µm, (B) Interdigitated OTFT with L = 4 µm and (C) Corbino OTFT.

The device parameters obtained from the fitting of the experimental data in Figure 6 to eq. 1 are depicted in Figure 7. Figure 7A shows the parasitic capacitance between gate and drain terminals (C_{GD}) as a function of the device aspect ratio obtained analytically (considering that for negative voltages C_{GD}=C_{OX}, as shown in the inset in Fig. 4A) (squares), from the experimental C-V curve (circles) and from the fitting of the amplifier frequency response to the eq. 1 (triangles). Similar values of C_{GD} are obtained for the different topologies and areas for the three extraction methods. The r_0 and g_m parameters are depicted in Figure 7B. A large dependence of these parameters with the channel dimensions is observed in both OTFT architectures, being less significant in the case of CTFT due to their complex device width and length radiuses-dependence. As observed, for the Interdigitated OTFT, g_m increases and r_0 decreases linearly with device area. Inversely, for the CTFT, g_m decreases and r_0 increases non-linearly with device area, what means larger separation between radiuses (i.e. L increase).

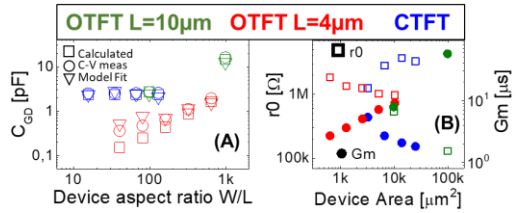

Fig. 7. (A) Analytically calculated Gate-Drain capacitance (squares), measured from the C-V curves (circles) and obtained from the data fitting (triangles). (B) r_0 (empty squares) and g_m (circles) obtained from the fitting.

V. Conclusions

Two different architectures of organic thin film transistors (Interdigitated and Corbino) with different dimensions have been studied. Their performance has been evaluated through the frequency response of an OTFT-based Common-Source (CS) amplifier, since it strongly depends on the device properties.

To extract the transistor parameters from the CS experimental data, a MOSFET-like small signal model of the OTFT has been assumed. The dependences observed for C_{GD} in all the devices have been verified from the comparison of the CS-extracted values with those obtained from C-V data and analytical calculation. The results show that the extracted small signal model parameters (g_m, r_0, and C_{GD}) depend on the device dimensions and materials properties. A linear dependence of r_0, g_m and C_{GD} with device width is observed in the Interdigitated OTFT. In the case of the Corbino devices, C_{GD} does not depend on the device widths or lengths (i.e. radiuses), since there is the same effective area under the gate electrode for negative biasing. g_m and r_0 present a non-linear area dependence, due to the relation between width and length in the CTFT. Therefore, the circuit performance is strongly driven by device dimensions, as for MOS devices, despite the large voltages applied.

Acknowledgments

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