
This is the **accepted version** of the journal article:

Pacheco-Sánchez, Aníbal; Feijoo, Pedro Carlos; Jiménez Jiménez, David. «Contact resistance extraction of graphene FET technologies based on individual device characterization». Solid-State Electronics, Vol. 172 (October 2020), art. 107882. DOI 10.1016/j.sse.2020.107882

This version is available at <https://ddd.uab.cat/record/321716>

under the terms of the  license

Highlights

Contact resistance extraction of graphene FET technologies based on individual device characterization

Anibal Pacheco-Sanchez, Pedro C. Feijoo, David Jiménez

- Contact resistances of graphene transistors are extracted with adapted Y -function methods
- Bias dependent and independent contact resistance values can be obtained
- No additional test structures are required for the extraction
- Results are in agreement with physics-based and other experimental approaches
- High-frequency performance highly degraded by non-optimal contacts

Contact resistance extraction of graphene FET technologies based on individual device characterization

Anibal Pacheco-Sanchez, Pedro C. Feijoo, David Jiménez

Departament d'Enginyeria Electrònica, Escola d'Enginyeria, Universitat Autònoma de Barcelona, Bellaterra 08193, Spain.

Abstract

Straightforward contact resistance extraction methods based on electrical device characteristics are described and applied here to graphene field-effect transistors from different technologies. The methods are an educated adaptation of extraction procedures originally developed for conventional transistors by exploiting the drift-diffusion-like transport in graphene devices under certain bias conditions. In contrast to other available approaches for contact resistance extraction of graphene transistors, the practical methods used here do not require either the fabrication of dedicated test structures or internal device phenomena characterization. The methodologies are evaluated with simulation-based data and applied to fabricated devices. The extracted values are close to the ones obtained with other more intricate methodologies. Bias-dependent contact and channel resistances studies, bias-dependent high-frequency performance studies and contact engineering studies are enhanced and evaluated by the extracted contact resistance values.

Keywords: graphene transistor, contact resistance, extraction method

1. Introduction

Graphene (G) field-effect transistors (FETs) have been demonstrated to be suitable candidates for low-power high-frequency (HF) applications in both rigid and flexible substrates [1]. Despite the early stage of this technology, extrinsic cutoff and maximum oscillation frequencies of tens of GHz have already been reported in fabricated GFETs [2]-[6]. In addition to other technological issues to be overcome, the metal-graphene interface in GFETs needs to be further optimized towards exploiting the graphene intrinsic properties, e.g., high velocity saturation and high mobility, at a device level, towards improving static and dynamic device characteristics [7]-[9]

In general, the contact resistance in GFETs is a representation of the physical mechanisms preventing the current flow at the interface between the metal contacts and the graphene channel. A correct and efficient characterization of this parameter is a critical point for the development of this emerging technology. A sophisticated physical description of the metal-graphene interface is preferred for the understanding of the carrier injection processes [9, 10], however, this might be unsuitable for an immediate device characterization since internal device quantities are required in this approach. As an alternative, analytical and compact device models are able to describe specific GFETs by using certain fitting parameters, including the contact resistance [11]-[18]. However, these are technology-specific approaches which rely on the physical basis of the models and on the calibration procedure.

Test-structure-based characterization methods are of more practical use in laboratories than the modeling approaches for contact resistance assessment. Some of them such as the two-point/four-point-measurement (2P/4P) technique [2], [19], the cross bridge Kelvin method [19], [20] and the widely used transfer length method (TLM) [3, 9, 14, 21, 22] have been used in GFETs. However, they involve the fabrication of additional devices and/or special measurement setups and hence, they represent a higher-cost solution in fabrication terms and a less straightforward option for immediate characterization purposes. Furthermore, the reliability of some of these methodologies for graphene FETs is still an open discussion at this early stage of the technology [7, 22, 23].

Practical and efficient extraction methods in which contact resistance values can be obtained from individual transistor characteristics are required in order to ease device and technology evaluation. In this work, two $I - V$ -based methodologies, enabled by a drift-diffusion description of the transport in GFETs, are presented and applied to simulation and experimental data.

2. GFET contact resistances

The device total resistance $R_{\text{tot}} (= V_{\text{DS}}/I_{\text{D}})$ of a GFET embraces the channel resistance R_{ch} due to scattering processes and/or defects in the graphene layer(s) and the resistances associated to the source and drain contact regions, $R_{\text{C,S}}$ and $R_{\text{C,D}}$, respectively. The latter can be lumped into a total contact resistance $R_{\text{C}} (= R_{\text{C,S}} + R_{\text{C,D}})$, i.e., $R_{\text{tot}} = R_{\text{ch}} + R_{\text{C}}$.

In general, two transport processes occur in a metal-graphene interface: from the metal contact to the coated-graphene region

Email address: AnibalUriel.Pacheco@uab.cat, PedroCarlos.Feijoo@uab.cat, david.jimenez@uab.cat (Anibal Pacheco-Sanchez, Pedro C. Feijoo, David Jiménez)

and from the coated-graphene region to the uncoated-graphene region [9], [10], [24]. The contact material [10], [21], the contact geometry and dimensions [19], [21], [24] as well as possible additional layers between metal and graphene [8] have an impact on the resistance originated by the first process. A bias-dependent potential barrier induced by a difference in the electronic properties of the coated and the uncoated graphene portions [9], [10] is the main cause of the resistance associated to the second process. By considering a practical point of view, these resistances are embraced in this work by the contact resistance corresponding to the drain or source contact in a GFET. Notice that, from a modeling point of view, the impact of the potential barrier at the metal-graphene interface on the performance of Schottky-type devices, such as GFETs, can be considered either into the channel resistance or into a bias-dependent contact resistance. R_C extracted at a single bias point in the device linear operation regime is generally provided for technology evaluation [8], [18], [21], however, a bias-dependent R_C reveals more information on internal physical phenomena at the metal-graphene interface.

3. Y-function-based contact resistance extraction methods for GFETs

Graphene transistors of different channel and gate lengths have been successfully described by a drift-diffusion (DD) approach [25]-[29] due to unavoidable scattering centers deviating the carrier transport within the channel from ideal ballistic conditions. Furthermore, mobility models inspired by conventional Si theory have described GFET experimental results [28], [29]. Extraction methods for contact resistance of GFETs, based on drift-diffusion theory, are presented next.

The Y -function [30] describes a relation of a DD drain current I_D equation at the linear region and its corresponding transconductance $g_m (= \partial I_D / \partial V_{GS})$ such as $Y = I_D / \sqrt{g_m}$, where the impact of mobility reduction effects has been removed [30]. Straightforward Y -function-based methodologies (YFMs) have been adapted [31], [32] and applied [33] for device parameters extraction, including R_C , of emerging transistor technologies. In order to consider YFM for GFETs, the underlying transport equation needs to embrace the physical phenomena associated to graphene devices, e.g., Dirac-cone bandstructure [25]-[27].

By assuming that the electron carrier transport in GFETs can be described by the DD-approach at the linear unipolar (ohmic) operation regime, and assuming that the carrier concentration can be computed as the average between the charge at the source side $C_{ox}(V_{GS} - V_{Dirac})$ and the charge at the drain side $C_{ox}(V_{GD} - V_{Dirac})$, I_D is given by [31], [32]

$$I_D \approx \beta \frac{(V_{GS} - V_{Dirac} - \frac{V_{DS}}{2})}{1 + \theta(V_{GS} - V_{Dirac} - \frac{V_{DS}}{2})} V_{DS}, \quad (1)$$

where $V_{GS/DS}$ is the extrinsic gate-to-source/drain-to-source voltage, $V_{Dirac} = V_{GS|_{\min(I_{Dirac})}} \sim V_{GS0} + V_{DS}/2$ is the Dirac voltage with V_{GS0} as the flat-band voltage [26], $\beta = \mu_0 C_{ox} w_g / L_g$ with a low-field mobility μ_0 , the oxide capacitance C_{ox} , the gate

width w_g and length L_g , and θ is the *extrinsic* mobility attenuation factor $\theta = \theta_0 + R_C \beta$ [30], [34] with the *intrinsic* attenuation factor due to vertical fields θ_0 .

By considering Eq. (1), the corresponding Y -function yields

$$Y = \sqrt{\beta V_{DS}} \left(V_{GS} - V_{Dirac} - \frac{V_{DS}}{2} \right), \quad (2)$$

from where β can be obtained at the maximum point of its derivative Y' with respect to V_{GS} for each V_{DS} . The maximum derivative has been chosen in order to guarantee a linear operation limit. Similarly, a function $X = 1 / \sqrt{g_m}$ is given by

$$X = \frac{1 + \theta(V_{GS} - V_{Dirac} - \frac{V_{DS}}{2})}{\sqrt{\beta V_{DS}}}, \quad (3)$$

the derivative of which yields a value for θ at the maximum point of its derivative X' with respect to V_{GS} for each V_{DS} . A V_{GS} -independent contact resistance value $R_{C,1}$ is extracted from the slope of the relation of θ with respect to β , once these terms have been obtained as described above, i.e., $R_{C,1} = \partial \theta / \partial \beta$.

Alternatively, in order to obtain a V_{GS} -dependent contact resistance $R_{C,2}$, an expression can be obtained by applying the definition of θ in Eq. (1) and using Eqs. (2) and (3) for rearranging terms. $R_{C,2}$ is hence given by [32]

$$R_{C,2} = \frac{V_{DS}}{Y^2} \left(V_{GS} - V_{Dirac} - \frac{V_{DS}}{2} \right)^2 \left[\frac{XY - 1}{\left(V_{GS} - V_{Dirac} - \frac{V_{DS}}{2} \right)^2} - \theta_0 \right]. \quad (4)$$

According to the methods' features, the transfer characteristics at different V_{DS} , rather than the output characteristics of the device are required for the R_C extraction. The methods can be also applied to hole transport by properly adapting Eq. (1) to a hole drain current model and following a similar approach as described above. In contrast to the widely used TLM, no assumption of uniform sheet resistance along the channel and the region under the contacts [48] is required in YFM. In order to obtain reliable reproducible values, the impact of unavoidable traps is recommended to be reduced in experimental data, e.g., by pulsed measurements [35], [36]. The extracted contact resistance values are useful for practical applications since they correspond to the bias region where GFETs are expected to work in HF circuits. In contrast to a previous study where R_C of GFETs has been extracted with a different YFM [37], the DD current model here involves minimum simplifications which has been proven to yield more accurate results in one-dimensional (1D) and two-dimensional (2D) transistors [31], [49]. Furthermore, a practical difference with the method in [37] is that for the extraction of R_C here, the characterization of μ_0 and C_{ox} is not required.

4. Contact characterization of different GFET technologies

4.1. Simulated devices

Scattering-affected DC transfer characteristics of top-gate GFETs with identical device architecture but with different gate

lengths have been generated with numerical device simulations consisting on a self-consistent solution of the Poisson's equation and the current-continuity equation [26]. This set of different L_g devices enables to imitate a TLM structure. The simulated devices consist of an hexagonal boron nitride (h-BN) encapsulated graphene channel with top and bottom h-BN layers thicknesses of 30 nm each and relative permittivity of 3 and a 285 nm SiO_2 substrate layer. The mobility is assumed to decrease with the vertical field. Further details on the considerations made for device geometry and carrier mobility can be found in [26]. A reference constant contact resistivity of $400 \Omega \cdot \mu\text{m}$ associated to interface layers has been set. The latter value corresponds to a previously reported metal-graphene interfaces [9] and it has been used previously for exhaustive performance projection studies [50]. Moreover, values close to the one used in this work for the contact resistivity have been used also for the description of experimental data within the same simulation framework used here [50], [51]. The devices gate lengths are of 30 nm, 56 nm, 100 nm, 178 nm and 300 nm. The corresponding TLM curves obtained at different bias are shown in Fig. 1(a).

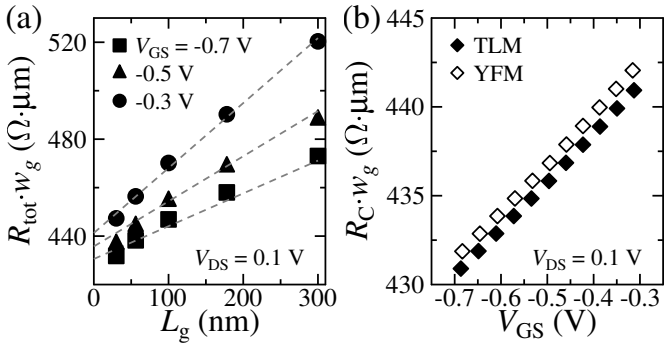


Figure 1: (a) TLM plot obtained from simulated devices at different bias. Dashed lines correspond to a linear fitting of each curve. (b) Contact resistivity of simulated devices extracted with TLM and YFM presented here (Eq. (4)).

The contact resistivity $R_{\text{C}} \cdot w_g$, extracted with Eq. (4), for the 100 nm-long simulated device¹ is in good agreement with results of the same parameter obtained via TLM within the same bias region as shown in Fig. 1(b). The V_{GS} -dependence and the larger value of extracted $R_{\text{C}} \cdot w_g (> 400 \Omega \cdot \mu\text{m})$ in comparison to the reference value indicate that both extraction methods embrace not only the impact of interfacial layers but also phenomena associated to the internal bias-dependence potential barrier (see Section 2).

The extraction methods have also been applied to data from a physics-based model (Landauer transport theory) [45] of a graphene-based transistor-like device (see Fig. 10 in [45]) with a reference contact resistance in the model $R_{\text{C,Land}} = R_{\text{C,PB,ref}} + R_{\text{C,IL}}$. $R_{\text{C,Land}}$ in [45] embraces a resistance associated to a potential barrier $R_{\text{C,PB,ref}}$ of 250 k Ω and a resistance associated to other interfacial layers $R_{\text{C,IL}}$ (value not reported).

¹Results of other devices under study have similar trend and magnitude of values (not shown here).

Notice that a metal/oxide/graphene/semiconductor stack is considered within the contact region and that the oxide is isotropic and isometric along the whole device in the direction of the carrier transport including the gated-graphene region under the top-gate [45]. $R_{\text{C},1}$ has been extracted for devices in [45] with identical architectures but different oxide thickness $t_{\text{ox,MG}}$ at the metal-graphene interface: a 10 nm $t_{\text{ox,MG}}$ for the simulated device under study (SDUT) A and a 100 nm $t_{\text{ox,MG}}$ for SDUT-B.

A smaller oxide improves the gate control over the graphene channel and hence the potential barrier is reduced [45]. The latter is the same tendency observed from the extracted smaller $R_{\text{C},1}$ of 342 k Ω for SDUT-A in contrast to the 351 k Ω extracted for SDUT-B. From $R_{\text{C},1} (= R_{\text{C,PB,ref}} + R_{\text{C,IL,ext}})$ on this study, the increase of the interface-layers resistance $R_{\text{C,IL,ext}}$ due to a larger $t_{\text{ox,MG}}$ can be also observed since a 101 k Ω for SDUT-B has been extracted in contrast to the 92 k Ω obtained for SDUT-A. Furthermore, the larger increase of the extracted channel resistance $R_{\text{ch,ext}} (= R_{\text{tot}} - R_{\text{C},1})$, associated to a higher number of scattering events in the thicker device (76 k Ω for SDUT-A, 397 k Ω for SDUT-B), in contrast to the almost similar $R_{\text{C},1}$ in both cases, indicate that the channel phenomena have no impact on the extraction method.

4.2. Fabricated GFET technologies

Contact resistance values have been extracted with the methods discussed above for a wide variety of GFET technologies [2, 3], [8], [14]-[18], [38]-[44], i.e., devices with different footprints, architectures and fabrication processes have been considered. The extractions have been performed here considering the dominant branch of the transfer characteristic in each device. Eq. (1) has been calculated with the extracted parameters, including $R_{\text{C},1}$ or $R_{\text{C},2}$ -depending on the selected method-, for each device under study and the results have been compared to the corresponding experimental data. A good match between such curves validates the parameters within the bias range selected for the extraction. This validation procedure has been applied for all devices. As an example, Fig. 2 shows the good match between experimental data of devices with different gate lengths (60 nm [17] and 1 μm [38]) and Eq. (1) using the corresponding extracted parameters, including the contact resistance. Additional curves for different GFET technologies ([3], [43]), i.e., different geometries, have been presented elsewhere [33] with similar results. Notice that the $I - V$ -based verification procedure presented here has not been performed for the contact resistance values extracted with other methods in the corresponding reference.

In order to further demonstrate the validity of the extraction methods presented above, the experimental transfer characteristics of the different GFET technologies and their corresponding description with Eq. (1) using the extracted parameters, including $R_{\text{C},1}$ and $R_{\text{C},2}$ are shown in Fig. 3 where $|V_{\text{GS},0}|$ is the lowest gate-to-source voltage in which the methods have been applied. Results are shown at the lowest reported $|V_{\text{DS}}|$ in all studies in order to ease the discussion, however, similar accurate descriptions have been also obtained at different $|V_{\text{DS}}|$ in all cases (not shown here).

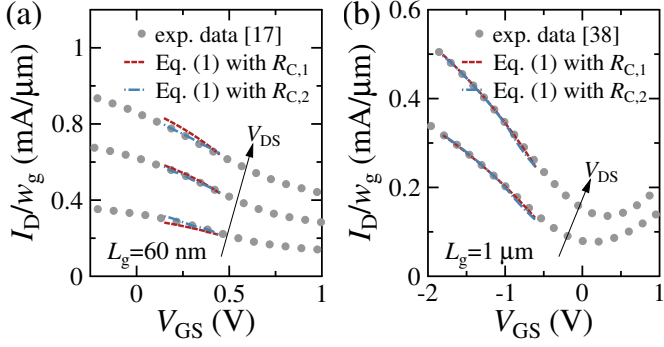


Figure 2: Transfer characteristics of different fabricated GFET technologies: (a) $w_g/L_g = 20/60 \mu\text{m}/\text{nm}$ [17] at V_{DS} equal to 0.1 V, 0.2 V and 0.3 V and (b) $w_g/L_g = 20/1000 \mu\text{m}/\text{nm}$ [38] at V_{DS} equal to 1 V and 1.5 V. Symbols represent experimental data and lines correspond to results with Eq. (1) considering the extracted parameters.

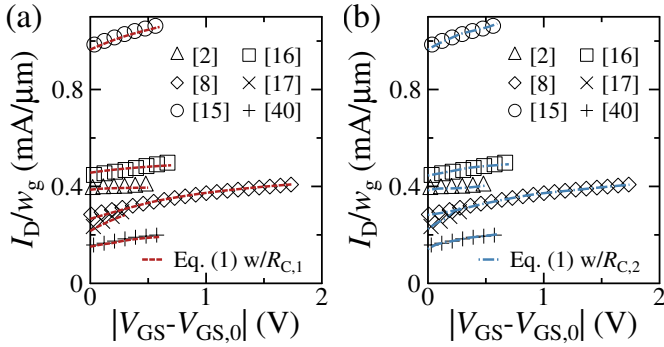


Figure 3: Transfer characteristics within the bias range where the extraction methods have been applied of devices with different gate lengths: 60 nm [17], 150 nm [15], 150 nm [16], 250 nm [2], 300 nm [40] and 2000 nm [8]. Symbols represent experimental data and lines represent Eq. (1) using the extracted (a) $R_{C,1}$ and (b) $R_{C,2}$.

Eq. (1) correctly describes the experimental data of all technologies under study using the extracted values, including $R_{C,1}$ and $R_{C,2}$, from both methodologies. The extraction methods have been applied here within a bias region ($|V_{GS} - V_{GS,0}|$) of interest for HF circuit applications, such as the strong linear regime, i.e., the bias corresponding to the Dirac point has not been considered. Due to noisy data and diverse technology-related effects, the bias range in which Eq. (1) is valid differs from device to device and thus, the extraction methods have been applied accordingly.

The contact resistivity values, extracted using $R_{C,1}$, of the different evaluated technologies [2, 3], [8], [14]-[18], [38]-[44] are listed in Table 1. $R_C \cdot w_g$ values of the same devices reported with test-structured based methods (TLM and 2P) and analytical model (AM) or compact model (CM) calibration are included as well in Table 1 for comparison along with some device geometry parameters of the studied technologies. $R_{C,1}$ has been extracted at a similar bias point at which the reference contact resistance $R_{C,ref}$ value has been reported in the corresponding study. Despite the universality of the methods described above, a scaling study is not feasible here since the studied devices are from different technologies.

The extracted values are close to the reference ones obtained

Table 1: Contact resistivity extracted at a single bias point $R_{C,1} \cdot w_g$, reported values of contact resistivity $R_{C,ref} \cdot w_g$ obtained with other methods and device dimensions of fabricated GFETs.

[ref.]	w_g (μm)	L_g (nm)	$R_{C,ref} \cdot w_g$ ($\text{k}\Omega \mu\text{m}$)	$R_{C,1} \cdot w_g$ ($\text{k}\Omega \mu\text{m}$)
with 2P				
[2]	14	100	0.2	0.2
[2]	14	250	0.2	0.2
with TLM				
[3]	-	100	1.1	1.4
[3]	-	300	1.1	1.4
[14]	80	2000	20 (also w/AM)	22
with AM				
[17]	20	60	0.2	0.2
[8]	10	2000	1.2	1.4
with CM				
[18]	12	100	3.1	3.3
[15]	12	150	0.08	0.2
[16]	24	150	2.4	2.3
[18]	12	300	6.2	6.3
[39]	12	300	4.6 in [13]	4.3
[41]	40	4000	16	20
[43]	25	5000	7 in [11]	10
[44]	5	10000	3 in [12]	3.2
R_C not extracted previously				
[40]	5	300	-	0.5
[38]	20	1000	-	3.4
[42]	20	4000	-	52
[47]	15	6000	-	0.2

by other more intricate and technology-specific methods. The mean relative deviation of $R_{C,1}$ and reference values, excluding the 150 nm-long device [15], is between 6% and 27%. However, not all the reference values are validated in contrast to the procedure included here (see Fig. 3). The difference between the extracted and reference data of the 150 nm-long device [15] can be explained by a strong impact of the Schottky barrier in the device performance which is not considered in the reference parameter in contrast to $R_{C,1}$ (and $R_{C,2}$) here which embraces the Schottky barrier contribution.

In contrast to contact resistance values obtained by fitting certain CMs or AMs, the Y -function based methods presented here work for different technologies without adjusting further parameters. While physics-based models are more accurate to describe the device performance, they result impractical from the characterization point of view since they require information regarding intrinsic physical device values, e.g., charge carrier density [8], [14]. Therefore, the methods discussed here are an alternative for immediate contact resistance extraction.

The same value of $R_{C,1}$ extracted for scattering-affected transistors with identical architecture and materials but different L_g [2], [3], where R_{ch} is expected to differ, indicates that channel phenomena have no impact on the extraction. The latter can be exploited in devices with more sophisticated channel morphology, such as graphene nanoribbons FETs [46], in which

channel and contact improvements can be evaluated independently. E.g., the $R_{C,1}$ of 36 M Ω of such device [46], extracted with Eq. (1), should decrease after a contact engineering but remain the same under only channel pattern treatment. Furthermore, the impact on the contacts quality of an electrostatic doping applied to the 1 μm -long device [38] can be observed in the reduction from 3.4 k $\Omega \cdot \mu\text{m}$, obtained with $R_{C,1}$, of the undoped device, to 1.7 k $\Omega \cdot \mu\text{m}$ of the doped device. The methods presented here are also an effective and immediate tool to evaluate contact engineering techniques in a technology such as the R_C improvement in fabricated GFETs [47] due to an optical lithography treatment ($R_{C,1} = 215 \Omega$) in contrast to non-treated contacts ($R_{C,1} = 450 \Omega$). $R_{C,2}$ can indicate such improvement over bias (not shown here) in contrast to the techniques in [47].

The V_{GS} -dependent contact resistivity, obtained from Eq. (4), of HF GFETs is presented in Fig. 4(a). Considerations for the bias region in which $R_{C,2}$ has been extracted remain the same as above (see discussion of Fig. 3).

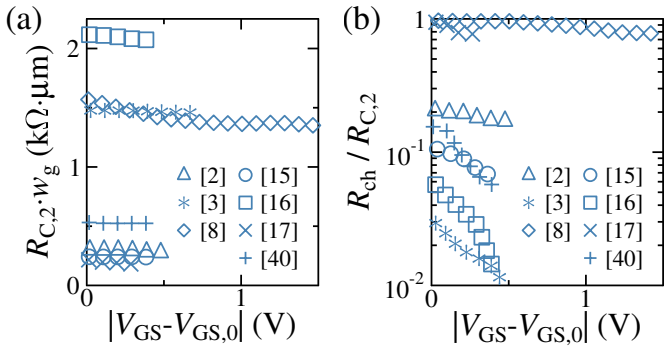


Figure 4: (a) Extracted V_{GS} -dependent contact resistivity (using Eq. (4)) of fabricated GFETs designed for HF applications [2, 3, 8, 15, 16, 17, 40]. (b) Ratio between channel resistance and extracted contact resistance $R_{C,2}$ for the HF devices. All curves correspond to the lowest reported V_{DS} .

A monotonic decrease of $R_{C,2} \cdot w_g$ is observed for an increasing $|V_{GS} - V_{GS,0}|$. This is an expected result in the linear operation regime due to the lowering of the potential barrier between metal and graphene. Low values of $R_{C,2} \cdot w_g$ as well as a linear constant response over certain bias, can indicate a suitable contact transparency for the intended low-power HF applications of carbon-based devices [52], [53]. The device linearity is recommended to be confirmed with trap-free data [35], [36]. The bias-dependent contact resistivity of the other devices under study can be found elsewhere [33].

The channel to contact resistance ratio shown in Fig. 4(b) indicates the impact of these parameters on the device behavior. The high steepness of the curves is due to the V_{GS} -dependence of R_{ch} rather than that of $R_{C,2}$. The contact resistance is extremely dominant for most of the devices [2, 3, 15, 16, 40]. The non-linear response of the curves corresponding to the 150 nm-long device [16] and the 2 μm -long device [8] suggest non-trivial internal mechanisms, e.g., transport through higher subbands, trap-induced current variations, etc., the discussion of which is out of the scope of this work. A ratio close to unity indicates that both channel and contact resistances are relevant for the 2 μm -long device [8] as well as for the 60 nm-long GFET

[17]. The latter reveals a non-intuitive scattering-affected behaviour of short devices.

4.3. R_C -based high-frequency performance projection

GFETs HF performance projection studies over bias are enabled by the $R_{C,2}$ and by a oftenly used small-signal model approximation [1]-[3], [26] where the extrinsic cutoff frequency $f_{t,e}$ and the extrinsic maximum oscillation frequency $f_{max,e}$ are given by

$$f_{t,e} \approx \frac{f_{t,i}}{1 + g_{d,i}R_C + 2\pi f_{t,i}C_{gd,i}R_C}, \quad (5)$$

$$f_{max,e} \approx \frac{f_{t,e}}{2\sqrt{g_{d,i}(R_g + R_C) + 2\pi f_{t,e}R_gC_{gd,i}}}, \quad (6)$$

respectively, where $f_{t,i} \approx g_{m,i}/[2\pi(C_{gs,i} + C_{gd,i})]$ is the intrinsic cutoff frequency, $g_{m,i}$ the intrinsic transconductance, $g_{d,i}$ the intrinsic output conductance, $C_{gs,i/gd,i}$ the intrinsic gate-to-source/gate-to-drain capacitance, R_g the gate resistance and R_C the contact resistance, corresponding here to $R_{C,2}$. For the calculation of $g_{m,i}$ and $g_{d,i}$, the intrinsic gate-to-source voltage $V_{GS,i} \approx V_{GS} - I_D R_C/2$ and the intrinsic drain-to-source voltage $V_{DS,i} \approx V_{DS} - I_D R_C$ have been considered.

The HF figures of merit defined in Eqs. (5) and (6) have been obtained for a 60 nm-long device [17], a 100 nm-long device [3] and a 250 nm-long device [2] from different technologies, using $R_{C,2}$ and the corresponding $C_{gs,i/gd,i}$ and R_g reported in the corresponding reference. $g_{m,i}$ and $g_{d,i}$ vary also with the bias point according to the reference data. Results are shown in Fig. 5. Notice that $f_{t,e}$ and $f_{max,e}$ of the best HF device reported in each work can not be reproduced here due to the lack of information required for the applied YFM, e.g., transfer characteristic not reported or reported at different bias.

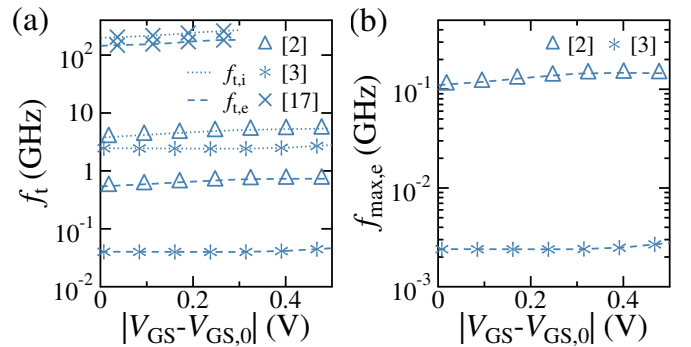


Figure 5: (a) Intrinsic and extrinsic cutoff frequency and (b) extrinsic maximum oscillation frequency within the bias range where $R_{C,2}$ has been extracted for different technologies: 60 nm-long device [17] ($V_{DS} = 0.1 \text{ V}$), 100 nm-long device [3] ($V_{DS} = 0.3 \text{ V}$) and 250 nm-long device [2] ($V_{DS} = 0.5 \text{ V}$).

The impact of R_C can be observed in the difference between intrinsic and extrinsic cutoff frequency: the highest the $R_{C,2}$ values (associated to the device in [3]), the most degraded $f_{t,e}$ with respect to $f_{t,i}$. In addition to electrostatic effects and in contrast to mature technologies, $f_{max,e}$ in HF GFETs is strongly affected not only by $R_{C,2}$ but also by R_g . The latter one can be optimized

by T-type gate architectures [2], [17] while the former requires further optimization which can be evaluated with the extraction methods presented here.

5. Conclusion

Efficient and immediate contact resistance extraction methods, developed within the context of drift-diffusion theory, have been described and applied to graphene FETs from different technologies. In contrast to other technology-specific and more intricate approaches, e.g., AMs, TLM, the extraction methodologies presented here are based on individual and practical transistor static characteristics, i.e., no additional test structures nor a description of internal physical phenomena are required. V_{GS} -independent and V_{GS} -dependent contact resistance values, $R_{C,1}$ and $R_{C,2}$, respectively, can be extracted according to the applied methodology. A drift-diffusion drain current model including the extracted parameters describes the transfer characteristics of the studied devices from different technologies. Extracted values are in good agreement with reference values of different simulation frameworks. Furthermore, the extracted R_{CS} of fabricated GFET technologies are close to the reference values obtained by other less straightforward methods. Immediate evaluation of contacts is enabled by the methods. $R_{C,2}$ enables the evaluation of the contact transparency as well as high-frequency performance projections considering the bias-dependent potential barrier at the metal-channel interface. The methods are expected to be applied to any 2D transistor technology within the bias range in which the carrier transport can be described by a drift-diffusion approach.

Acknowledgements

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreements No GrapheneCore2 785219 and No GrapheneCore3 881603, from Ministerio de Ciencia, Innovación y Universidades under grant agreement RTI 2018-097876-BC21(MCIU/AEI/FEDER, UE), and project 001-P-0011702-GraphCAT: Comunitat Emergent de grafè a Catalunya, co-funded by FEDER within the framework of Programa Operatiu FEDER de Catalunya 2014-2020.

References

- [1] F. Schwierz, "Graphene Transistors: Status, Prospects, and Problems", *Proceedings of the IEEE*, vol. 101, no. 7, pp. 1567-1584, Jul. 2013. DOI: 10.1109/JPROC.2013.2257633
- [2] Z. Guo, R. Dong, P. S. Chakraborty, N. Lourenco, J. Palmer, Y. Hu, M. Ruan, J. Hankinson, J. Kunc, J. D. Cressler, C. Berger, W. A. de Heer, "Record Maximum Oscillation Frequency in C-Face Epitaxial Graphene Transistors", *Nano Letters*, vol. 13, pp. 942-947, Feb. 2013. DOI: 10.1021/nl303587r
- [3] H. Lyu, Q. Lu, J. Liu, X. Wu, J. Zhang, J. Li, J. Niu, Z. Yu, H. Wu, H. Qian, "Deep-submicron graphene field-effect transistors with state-of-art f_{max} ", *Scientific Reports*, vol. 6, 35717, Oct. 2016. DOI: 10.1038/srep35717
- [4] C. Yu, Z. Z. He, X. B. Song, Q. B. Liu, T. T. Han, S. B. Dun, J. J. Wang, C. J. Zhou, J. C. Guo, Y. J. Lv, Z. H. Feng, S. J. Cai, "Improvement of the Frequency Characteristics of Graphene Field-Effect Transistors on SiC Substrate", *IEEE Electron Device Letters*, vol. 38, no. 9, pp. 1339-1342, Sep. 2017. DOI: 10.1109/LED.2017.2734938
- [5] M. Bonmann, M. Asad, X. Yang, A. Generalov, A. Vorobiev, L. Banzerus, C. Stampfer, M. Otto, D. Neumaier, J. Stake, "Graphene Field-Effect Transistors With High Extrinsic f_T and f_{max} ", *IEEE Electron Device Letters*, vol. 40, no. 1, Jan. 2019. DOI: 10.1109/LED.2018.2884054
- [6] P. Peng, Z. Wang, Z. Wei, Z. Tian, M. Li, L. Ren, Y. Fu, "Radio-frequency Power Amplifier Based on CVD Graphene Field-effect Transistor", in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2019. DOI: 10.1109/ISCAS.2019.8702115
- [7] F. Giubileo, A. Di Bartolomeo, "The role of contact resistance in graphene field-effect devices", *Progress in Surface Science*, vol. 92, pp. 143-175, Jun. 2017. DOI: 10.1016/j.progsurf.2017.05.002
- [8] A. Hsu, H. Wang, K. K. Kim, J. Kong, T. Palacios, "Impact of graphene interface quality on contact resistance and RF device performance", *IEEE Electron Device Letters*, vol. 32, no. 8, pp. 1008-1010, Aug., 2011. DOI: 10.1109/LED.2011.2155024
- [9] F. Xia, V. Perebeinos, Y.-M. Lin, Y. Wu, P. Avouris, "The origins and limits of metal-graphene junction resistance", *Nature Nanotechnology*, vol. 6, pp. 179-184, Mar. 2011. DOI: 10.1038/NNANO.2011.6
- [10] F. A. Chaves, D. Jiménez, A. A. Sagade, W. Kim, J. Riihonen, H. Lipsanen, D. Neumaier, "A physics-based model of gate-tunable metal-graphene contact resistance benchmarked against experimental data", *2D Materials*, vol. 2 no. 2, 025006, May 2015. DOI: 10.1088/2053-1583/2/2/025006
- [11] G. M. Landauer, D. Jimenez, J. L. Gonzalez, "An accurate and Verilog-A compatible compact model for graphene field-effect transistors", *IEEE Transactions on Nanotechnology*, vol. 13, no. 5, pp. 895-904, Sep. 2014. DOI: 10.1109/TNANO.2014.2328782
- [12] D. Jimenez, O. Moldovan, "Explicit drain-current model of graphene field-effect transistors targeting analog and radio-frequency applications", *IEEE Transactions on Electron Devices*, vol. 58, no. 11, pp. 4049-4052, Nov. 2011. DOI: 10.1109/TED.2011.2163517
- [13] J. D. Aguirre-Morales, S. Frégone, C. Mukherjee, W. Wei, H. Happy, C. Maneux, T. Zimmer, "A large-signal monolayer graphene field-effect transistor compact model for RF-circuit applications", *IEEE Transactions on Electron Devices*, vol. 64, no. 10, pp. 4302-4309, Oct. 2017. DOI: 10.1109/TED.2017.2736444
- [14] A. D. Smith, S. Vaziri, S. Rodriguez, M. Östling, M. C. Lemme, "Large scale integration of graphene transistors for potential applications in the back end of the line", *Solid-State Electronics*, vol. 108, pp. 61-66, Jan. 2015. DOI: 10.1016/j.sse.2014.12.014
- [15] L. Sang, Y. Xu, Y. Wu, R. Chen, "Device and compact circuit-level modeling of graphene field-effect transistors for RF and microwave applications", *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 8, pp. 2559-2570, Aug. 2018. DOI: 10.1109/TCSI.2018.2793852
- [16] D. Mele, S. Frégone, S. Lepilliet, E. Pichonat, G. Dambrine, H. Happy, "High Frequency Noise Characterisation of Graphene FET device", in *Proc. IEEE MTT-S International Microwave Symposium Digest (MTT)*, Seattle, WA, U.S.A., 2013. DOI: 10.1109/MWSYM.2013.6697561
- [17] Y. Wu, X. Zou, M. Sun, Z. Cao, X. Wang, S. Huo, J. Zhou, Y. Yang, X. Yu, Y. Kong, G. Yu, L. Liao, T. Chen, "200 GHz Maximum Oscillation Frequency in CVD Graphene Radio Frequency Transistors", *ACS Applied Materials & Interfaces*, vol. 8, no. 39, pp. 25645-25649, Sep. 2016. DOI: 10.1021/acsami.6b05791
- [18] N. Mavredakis, W. Wei, E. Pallecchi, D. Vignaud, H. Happy, R. Garcia-Cortadella, A. B. Calia, J. A. Garrido, D. Jimenez, "Velocity Saturation Effect on Low Frequency Noise in Short Channel Single Layer Graphene Field Effect Transistors", *ACS Applied Electronic Materials*, vol. 1, no. 12, pp. 2626-2636, Nov. 2019. DOI: 10.1021/acsaem.9b00604
- [19] K. Nagashio, A. Toriumi, "Density-of-States Limited Contact Resistance in Graphene Field-Effect Transistors", *Japanese Journal of Applied Physics*, vol. 50, 070108, Jul. 2011. DOI: 10.1143/JJAP.50.070108
- [20] K. Nagashio, T. Nishimura, K. Kita, A. Toriumi, "Contact resistivity and current flow path at metal/graphene contact", *Applied Physics Letters*, vol. 97, 143514, Oct. 2010. DOI: 10.1063/1.3491804
- [21] L. Anzi, A. Mansouri, P. Pedrinazzi, E. Guerriero, M. Fiocco, A. Pesquera, A. Centeno, A. Zurutuza, A. Behnam, E. A. Carrion, E. Pop,

- R. Sordan, "Ultra-low contact resistance in graphene devices at the Dirac point", *2D Materials*, vol. 5, no. 2, 025014, Feb. 2018. DOI: 10.1088/2053-1583/aaab96
- [22] S. Venica, F. Driussi, A. Gahoi, S. Kataria, P. Palestri, M. C. Lemme, L. Selmi, "Reliability analysis of the metal-graphene contact resistance extracted by the transfer length method", in Proc. *IEEE International Conference on Microelectronic Test Structures (ICMETS)*, Austin, TX, USA, Mar. 2018. DOI: 10.1109/ICMETS.2018.8383765
- [23] A. D. Smith, S. Wagner, S. Kataria, B. G. Malm, M. C. Lemme, M. Östling, "Wafer-scale statistical analysis of graphene FETs-Part I: wafer-scale fabrication and yield analysis", *IEEE Transactions on Electron Devices*, vol. 64, no. 9, pp. 3919-3926, Sep. 2017. DOI: 10.1109/TED.2017.2727820
- [24] M. König, G. Ruhl, A. Gahoi, S. Wittmann, T. Preis, J.-M. Batke, I. Costina, M. C. Lemme, "Accurate graphene-metal junction characterization", *IEEE Journal of the Electron Devices Society*, vol. 7, pp. 219-226, Jan. 2019. DOI: 10.1109/JEDS.2019.2891516
- [25] I. Meric, M. Y. Han, A. F. Young, B. Ozylmaz, P. Kim, K. L. Shepard, "Current saturation in zero-bandgap, top-gated graphene field-effect transistors", *Nature Nanotechnology*, vol. 3, no. 11, pp. 654-659, Nov. 2008. DOI: 10.1038/nnano.2008.268
- [26] P. C. Feijoo, F. Pasadas, J. M. Iglesias, E. M. Hamham, R. Rengel, D. Jiménez, "Radio Frequency Performance Projection and Stability Tradeoff of h-BN Encapsulated Graphene Field-Effect Transistors", *IEEE Transactions on Electron Devices*, vol. 66, no. 3, pp. 1567-1573, Mar. 2019. DOI: 10.1109/TED.2018.2890192
- [27] M. G. Ancona, "Electron transport in graphene from a diffusion-drift perspective", *IEEE Transactions on Electron Devices*, vol. 57, no. 3, pp. 681-689, Mar. 2010. DOI: 10.1109/TED.2009.2038644
- [28] V. E. Dorgan, M.-H. Bae, E. Pop, "Mobility and saturation velocity in graphene on SiO₂", *Applied Physics Letters*, vol. 91, no. 8, 082112, Aug. 2010. DOI: 10.1063/1.3483130
- [29] S. Wang, Z. Jin, A. Muhammad, S. Peng, X. Huang, D. Zhang, J. Shi, "Intrinsic carrier mobility extraction based on a new quasi-analytical model for graphene field-effect transistors", *Journal of Physics D: Applied Physics*, vol. 49, 425103, Sep. 2016. DOI: 10.1088/0022-3727/49/42/425103
- [30] G. Ghibaudo, "New method for the extraction of MOSFET parameters", *Electronics Letters*, pp. 543-545, vol. 24, no. 9, Apr. 1988. DOI: 10.1049/el:19880369
- [31] A. Pacheco-Sanchez, M. Claus, S. Mothes, M. Schröter, "Contact resistance extraction methods for short- and long-channel carbon nanotube field-effect transistors", *Solid-State Electronics*, vol. 125, pp. 161-166, 2016. DOI: 10.1016/j.sse.2016.07.011
- [32] A. Pacheco-Sanchez, M. Claus, "Bias-Dependent Contact Resistance Characterization of Carbon Nanotube FETs", *IEEE Transactions on Nanotechnology*, vol. 19, no. 1, pp. 47-51, Jan. 2020. DOI: 10.1109/TNANO.2019.2958677
- [33] A. Pacheco-Sanchez, D. Jiménez, "Efficient contact resistance extraction from individual device characteristics of graphene FETs", in Proc. *IEEE Nanotechnology Materials and Devices Conference*, Stockholm, Sweden, Oct. 2019.
- [34] C. Hao, B. Cabon-Till, S. Cristoloveanu, G. Ghibaudo, "Experimental determination of short-channel MOSFET parameters", *Solid-State Electronics*, vol. 28, no. 10, pp. 1025-1030, Jan. 1985. DOI: 10.1016/0038-1101(85)90034-6
- [35] M. Haferlach, A. Pacheco, P. Sakalas, M. Alexandru, S. Hermann, T. Nardmann, M. Schröter, M. Claus, "Electrical characterization of emerging transistor technologies: issues and challenges", *IEEE Transactions on Nanotechnology*, vol. 15, no. 4, pp. 619-626, 2016. DOI: 10.1109/TNANO.2016.2564925
- [36] E. A. Carrion, A. Y. Serov, S. Islam, A. Behnam, A. Malik, F. Xiong, M. Bianchi, R. Sordan, E. Pop, "Hysteresis-Free Nanosecond Pulsed Electrical Characterization of Top-Gated Graphene Transistors", *IEEE Transactions on Electron Devices*, vol. 61, no. 5, pp. 1583-1589, May 2014. DOI: 10.1109/TED.2014.2309651
- [37] F. Urban, G. Lupina, A. Grillo, N. Martucciello, A. Di Bartolomeo, "Contact resistance and mobility in back-gate graphene transistors", *Nano Express*, vol. 1, 010001, Mar. 2020. DOI: 10.1088/2632-959X/ab7055
- [38] M. Tian, X. Li, T. Li, Q. Gao, X. Xiong, Q. Hu, M. Wang, X. Wang, Y. Wu, "High-Performance CVD Bernal-Stacked Bilayer Graphene Transistors for Amplifying and Mixing Signals at High Frequencies", *ACS Applied Materials & Interfaces*, vol. 10, no. 24, pp. 20219-20224, May 2018. DOI: 10.1021/acsami.8b04065
- [39] W. Wei, G. Deokar, M. Belhaj, D. Mele, E. Pallecchi, E. Pichonat, D. Vignaud, H. Happy, "Fabrication and characterization of CVD-grown graphene based field-effect transistor", in Proc. *IEEE 44th European Microwave Conference (EuMC)*, pp. 367-370., Rome, Italy, Oct. 2014. DOI: 10.1109/EuMC.2014.6986446
- [40] R. Cheng, J. Bai, L. Liao, H. Zhou, Y. Chen, L. Liu, Y.-C. Lin, S. Jiang, Y. Huang, X. Duan, "High-frequency self-aligned graphene transistors with transferred gate stacks", *Proceedings of the National Academy of Sciences of the United States of America*, vol. 109, no. 29, pp. 11588-11592, Jul. 2012.
- [41] M. Iannazzo, V. L. Muzzo, S. Rodriguez, H. Pandey, A. Rusu, M. Lemme, E. Alarcon, "Optimization of a compact I-V model for graphene FETs: extending parameter scalability for circuit design exploration", *IEEE Transactions on Electron Devices*, vol. 62, no. 11, pp.3870-3875, Nov. 2015. DOI: 10.1109/TED.2015.2479036
- [42] A. D. Smith, S. Wagner, S. Kataria, B. G. Malm, M. C. Lemme, M. Östling, "Wafer-scale statistical analysis of graphene field-effect transistors—Part II: analysis of device properties", *IEEE Transactions on Electron Devices*, vol. 64, no. 9, pp. 3927-3933, Sep. 2017. DOI: 10.1109/TED.2017.2727823
- [43] H. Wang, A. Hsu, J. Kong, D. A. Antoniadis, T. Palacios, "Compact virtual-source current-voltage model for top- and back-gated graphene field-effect transistors", *IEEE Transactions on Electron Devices*, vol. 58, no. 5, pp. 1523-1533, May 2011. DOI: 10.1109/TED.2011.2118759
- [44] J. Kedzierski, P.-L. Hsu, A. Reina, J. Kong, P. Healey, P. Wyatt, C. Keast, "Graphene-on-insulator transistors made using C on Ni chemical-vapor deposition", *IEEE Electron Device Letters*, vol. 30, no. 7, pp. 745-747, Jul. 2009. DOI: 10.1109/LED.2009.2020615
- [45] F. A. Chaves, D. Jimenez, "The Role of the Fermi Level Pinning in Gate Tunable Graphene-Semiconductor Junctions", *IEEE Transactions on Electron Devices*, vol. 63, no. 11, pp. 4521-4526, Nov. 2016. DOI: 10.1109/TED.2016.2606139
- [46] V. Passi, A. Gahoi, B. V. Senkovskiy, D. Haberer, F. R. Fischer, A. Grüneis, M. C. Lemme, "Field-effect transistors based on networks of highly aligned, chemically synthesized N = 7 armchair graphene nanoribbons", *ACS Applied Materials & Interfaces*, vol. 10, no. 12, pp. 9900-9903, Mar. 2018. DOI: 10.1021/acsami.8b01116
- [47] Q. Kong, X. Wang, L. Xia, C. Wu, Z. Feng, M. Wang, J. Zhao, "Achieving low contact resistance by engineering a metal-graphene interface simply with optical lithography", *ACS Applied Materials & Interfaces*, vol. 9, no. 25, pp. 21573-21578, Jun. 2017. DOI: 10.1021/acsami.7b04993
- [48] D. Schroder, "Semiconductor Material and Device Characterization", Hoboken, NJ, USA: Wiley, 2006.
- [49] A. Pacheco-Sanchez, D. Jiménez, "Accuracy of Y-function methods for parameters extraction of two-dimensional FETs across different technologies", *Electronics Letters*, 2020. DOI: 10.1049/el.2020.1502
- [50] P. C. Feijoo, D. Jiménez, X. Cartoixa, "Short channel effects in graphene-based field effect transistors targeting radio-frequency applications", *2D Materials*, vol. 3, 025036, Jun. 2016. DOI: 10.1088/2053-1583/3/2/025036
- [51] P. C. Feijoo, F. Pasadas, M. Bonmann, M. Asad, X. Yang, A. Generalov, A. Vorobiev, L. Banszerus, C. Stampfer, M. Otto, D. Neumaier, J. Stake, D. Jiménez, "Does carrier velocity saturation help to enhance f_{max} in graphene field-effect transistors?", *Nanoscale Advances*, Jul. 2020. DOI: 10.1039/C9NA00733D
- [52] K. N. Parrish, D. Akinwade, "Impact of contact resistance on the transconductance and linearity of graphene transistors", *Applied Physics Letters*, vol. 98, 183505, May 2011. DOI: 10.1063/1.3582613
- [53] S. Mothes, M. Claus, M. Schröter, "Toward linearity in Schottky barrier CNTFETs", *IEEE Transactions on Nanotechnology*, vol. 14, no. 2, pp. 372-378, Mar. 2015. DOI: 10.1109/TNANO.2015.2397696