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Experimental observation and modeling of the impact of traps on static and analog/HF performance of graphene transistors

Anibal Pacheco-Sanchez, Nikolaos Mavredakis, Pedro C. Feijoo, Wei Wei, Emiliano Pallecchi, Henri Happy, David Jiménez

***Abstract*—The trap-induced hysteresis on the performance of a graphene field-effect transistor is experimentally diminished here by applying consecutive gate-to-source voltage pulses of opposing polarity. This measurement scheme is a practical and suitable approach to obtain reproducible device characteristics. Trap-affected and trap-reduced experimental data enable a discussion regarding the impact of traps on static and dynamic device performance. An analytical drain current model calibrated with the experimental data enables the study of the traps effects on the channel potential within the device. High-frequency figures of merit and the intrinsic gain of the device obtained from both experimental and synthetic data with and without hysteresis show the importance of considering the generally overlooked impact of traps for analog and high-frequency applications.**

***Index Terms*—GFET, traps, hysteresis, opposing pulses, channel potential, analytical model, high-frequency performance.**

I. Introduction

Reproducible graphene field-effect transistor (GFETs) characteristics are required in order to boost the use of circuits based on this emerging technology, specially on the low-power high-frequency (HF) applications scenario where its extraordinary intrinsic characteristics, e.g., high carrier mobility, can be exploited [1]. In GFETs, traps within the channel, substrate and high-κ oxide materials, as well as at the interfaces between them, are one of the major issues affecting the device performance, i.e., in order to obtain hysteresis-free reproducible characteristics, the impact of traps should be diminished [2], [3]. Technological efforts towards reducing the presence of traps in graphene-based technologies have shown a discrete success on individual devices [3]-[5]. For wafer-scale integration however, defect-induced traps within the channel associated to the graphene transfer process, as well as oxide traps, still affect the device behavior [6], [7]. The characterization of traps in GFETs is therefore required at this stage of the technology in order to enhance device and circuit reproducibility by finding the adequate bias conditions to diminish their impact on the overall device performance.

Trap mechanisms within GFET architectures have been experimentally characterized by observing the electrical device characteristics obtained with time-dependent-voltage pulses [2]-[5], [8]-[12]. Different time constants related to trapping and detrapping processes have been identified for different graphene technologies ranging over a large span of time, depending on the location of the traps (bulk, oxide, channel, interfaces) [2], [8]-[11]. In most of the GFETs trap studies, the drain-to-source voltage V_{DS} signal has been varied over time while keeping the gate-to-source V_{GS} constant [3], [5], [8], [11], [12] i.e., V_{DS}-induced hysteresis has been the main focus of such investigations rather than the trap impact on the device performance due to vertical fields applied to the channel. The latter effect has been studied for a global-back-gate device with SiO_2 dielectric [10] and for top-gate devices with high-κ gate oxides [2] in order to obtain the trapping time constants of such specific technologies.

The impact of traps on analog/HF performance of GFETs has been rarely discussed. Some trapping processes can be too slow in comparison to the targeted operation frequency ($\sim$GHz), i.e., their impact is generally neglected based on this assumption [9]. However, the DC bias point, required to activate the transistor for its dynamic operation, is still affected by traps, i.e., the drift of this point due to traps can induce reproducibility issues in GFET-based HF applications, as demonstrated for other emerging transistor technologies [13], [14]. HF figures of merit (FoM) have been reported for GFETs measured under pulsed bias conditions [3], [15], however, no trap-affected data have been shown in order to understand the difference in the dynamic performance with and without hysteresis. As an alternative to overcome the challenging measurement setup required for pulsed HF characterization [3], [13], the HF FoM of GFETs can be measured by considering a non-quiescent holding time large enough for the traps to be inactive [16]-[18]. The latter is a useful approach to understand the internal device mechanisms after removing the impact of traps. However, such holding time for trap-reduced characterization varies between technologies and depends on the measurement history [2], [8]-[11]. Furthermore, in a practical HF scenario, GFET-based circuits should work under rapid pulsed biasing schemes rather than on a holding time-based scheme in order to compete with incumbent technologies, e.g., in applications involving high-data rate communications with different pulse-based modulation schemes [19], [20]. Hence, an alternative practical biasing method to achieve trap-reduced GFET performance for its use in HF applications is required.

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The aims of this work are to show experimentally the impact of traps on the GFET static and dynamic performance and to provide a straightforward model of trap-related effects. For the first goal, the trap-affected and trap-reduced performance of a buried-gate GFET technology are characterized with a standard V_{GS}-staircase sweep and with an opposing-pulse sweep of V_{GS}, respectively. The opposing-pulse sweep allows to determine the impact of traps on transistor performance indicators and it is a practical measurement approach to obtain reproducible characteristics. In second place, this paper successfully describes the impact of traps on the net charge within the device via an analytical compact model. Typical models only consider traps activated by vertical electrical fields caused by the gate voltage stress, but our model also include traps activated by hot-carriers, which result in a V_{DS}-dependence of trapped charge. Our compact model thus allows calculation of traps densities and enables the study of GFET-based circuits considering devices affected by traps at different bias points. This work projects the dynamic performance via HF/analog FoM, including cutoff frequency, maximum oscillation frequency and intrinsic gain. Additionally, it provides an insight on the generally neglected fact that traps affect not only the static device performance but also the dynamic response at different bias.

II. Device description and measurement techniques

A two-finger aluminium back-gated GFET fabricated on a SiO_2 ($300\,\mathrm{nm}$)/Si (high resistivity silicon substrate) has been characterized in this study. The device gate width w_{g} and gate length are $12\times2\,\mu\mathrm{m}$ and $300\,\mathrm{nm}$, respectively (the transistor is a dual gate of 12 microns each). The single graphene layer has been grown via chemical vapor deposition in a host substrate (a copper foil) and transferred on the top of previously patterned bottom Al gate fingers via a wet chemical transfer technique. The natural oxidation of the Al back-gate has been obtained prior the transfer of monolayer of graphene. A $\sim4\,\mathrm{nm}$ thick Al_2O_3 dielectric layer (ellipsometry measurement) is then obtained which separates graphene and gate. The Ni/Au source and drain contacts are separated by a distance of $1\,\mu\mathrm{m}$. The gate is located at the same distance from source and drain contacts. More details on the graphene transfer process and on the device fabrication process as well as the device layout have been discussed elsewhere [21].

Two different measurement techniques have been used for the experimental device characterization: staircase voltage sweep and opposing voltage sweep. Fig. 1(a) shows a sketch of the V_{GS} and V_{DS} for the staircase sweep characterization. This standard characterization scheme usually acquires the current data at the end of the pulse where a steady-state current is expected. This steady-state in graphene devices however, depends on the technology and measurement history as elucidated by the wide span of trap-time constants reported in different studies (from ns to s) [2], [5], [8]-[12], [18].

The opposing sweep technique sketched in Fig. 1(b) diminishes the trap-effects since the measurement history is compensated by the consecutive opposite bias pulses, i.e., in time-symmetric trapping and detrapping processes, the effects related to remaining carriers trapped at the end of a positive or negative V_{GS} pulse, if any, are counterbalanced by trapped carriers at the consecutive pulse of similar magnitude but opposite bias. This reversible trapping effects technique has been previously reported for devices with high-κ oxides [13], [22]-[24] but not exploited before for GFETs. Furthermore, this bias scheme is less challenging to implement in contrast to a pulsed characterization technique and more practical in circuit applications than a holding-time bias approach, e.g., in modulators required for high-data rate communications [19], [20].

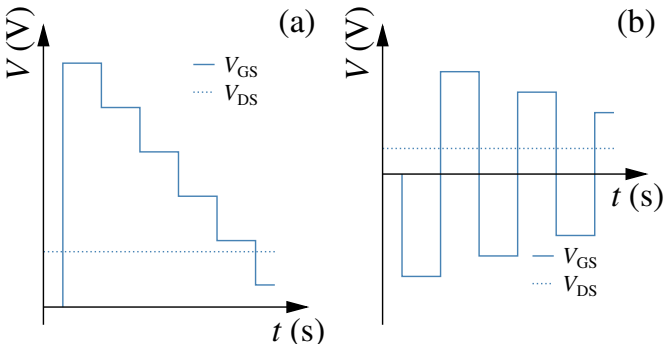


Fig. 1. Sketch of the applied voltage signals over time for (a) staircase sweep and (b) opposing pulses sweep measurements.

Measurements with both techniques described above have been performed with a K4200 semiconductor characterization system by applying consecutive forward and backward V_{GS}-sweeps at room temperature. V_{DS} has been kept constant. The duration of the applied V_{GS} signal is of $\sim0.9\,\mathrm{s}$ which is large enough to consider trapping processes to be active according to time constants in the same range obtained for GFETs [10], [11]. This is confirmed by the hysteresis observed in the experimental section. Self-heating effects are expected to be much faster [11], [12] than the trapping processes characterized with this pulse width. Notice that in contrast to other studies [3], [5], [8], [11], [12], the gate oxide traps are directly affected by transitions of the applied vertical fields here.

III. Experimental investigation

The channel potential of the device can be modified by interface or oxide traps capturing or releasing carriers since these processes reduce the gate control, i.e., traps shield the channel potential from the applied voltage [25]. These trap effects have a different impact on the device performance depending on the measurement technique. The transfer characteristics of the device obtained via consecutive forward-backward sweeps with the staircase and opposing measurement techniques are shown in Fig. 2. The typical ambipolar behavior of GFETs, separated by a charged neutrality voltage point identified as the Dirac voltage $V_{\mathrm{Dirac}} = V_{\mathrm{GS}}|_{\mathrm{min}(I_{\mathrm{D}})}$, can be observed.

The hysteresis in the experimental characteristics measured with forward and backward sweeps using the staircase technique (Fig. 2(a)) is induced by trapping processes started during the forward sweep and continued during the change of sweep direction. This leads to lower I_{D} and higher V_{Dirac} in the backward sweep compared to the forward sweep at $V_{\mathrm{GS}} > V_{\mathrm{Dirac}}$. The release of trapped carriers at $V_{\mathrm{GS}} < V_{\mathrm{Dirac}}$ during the backward sweep affects positively the channel potential [8], i.e., higher I_{D} is observed in contrast to the acquired during the former sweep. The reduced hysteresis

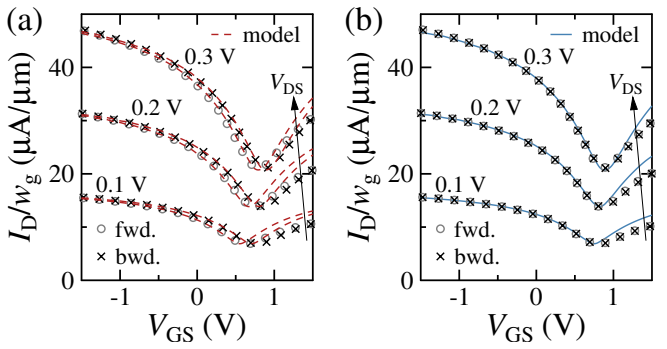


Fig. 2. Transfer characteristics of the 300 nm-long GFET with (a) staircase sweep and (b) opposing pulse sweep characterization. Markers are experimental data and lines represent modeling results.

observed at more negative V_{GS} can be associated to the device reaching a steady-like-state.

The almost negligible hysteresis observed in the transfer characteristic measured with the opposing pulse technique, as observed in Fig. 2(b), can be explained by trapping and detrapping processes with quasi-symmetrical time constants and by the compensating effect due to opposing polarity pulses as mentioned in Section II. The transconductance ($g_m = \partial I_D/\partial V_{GS}$) and output conductance ($g_d = \partial I_D/\partial V_{DS}$) plots in Figs. 3 and 4, make the hysteresis in the staircase sweeps more evident. The slight observed hysteresis in the opposing sweep data at high V_{DS} can be related to hot carriers-induced [2] asymmetric trapping processes which can not be counterbalanced with this technique.

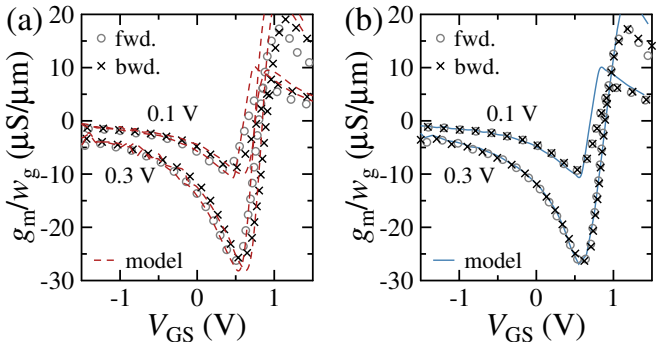


Fig. 3. Transconductance versus V_{GS} at different V_{DS} of a 300 nm-long GFET with (a) stair-case sweep and (b) opposing pulse sweep characterization. Markers are experimental data and lines represent modeling results.

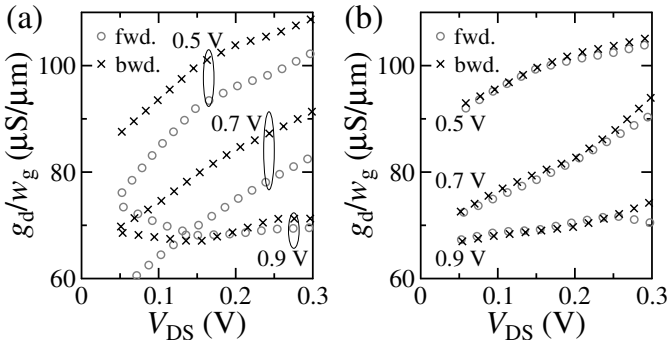


Fig. 4. Output conductance versus V_{DS} at different V_{GS} of a 300 nm-long GFET with (a) stair-case sweep and (b) opposing pulse sweep characterization.

Transistor performance indicators oftenly used to project the device HF performance are the maximum point of the transconductance $g_{m,max}$ and a low value of g_d. Due to traps, however, the bias-point and the magnitude of each of these parameters differ in each measurement run. E.g., by analyzing the sweeps with the staircase technique, $|g_{m,max}|$ is found at different V_{GS} and its magnitude differ in comparison to the same metric obtained with both sweeps using the opposing pulse technique. Furthermore, a $|g_{m,max}|$ equal to 634 μS at the highest V_{DS} obtained with trap-affected data is ∼21 μS lower than the same metric observed at the same V_{DS} with trap-reduced data. A large difference between trap-affected and trap-reduced data is observed for the output conductance (Fig. 4). In addition to the distinct values obtained in each case, the bias dependence of trap-affected data is notoriously different between different sweeps. Variations in the operating bias point and magnitude of g_m and g_d can mislead the expected analog/HF performance projections based on this parameter such as the maximum oscillation frequency.

In order to explicitly show the impact of traps on analog/HF FoMs, the intrinsic/extrinsic cutoff frequency $f_{t,i/e}$ and the extrinsic maximum oscillation frequency $f_{max,e}$ have been estimated from the trap-affected and trap-reduced data of the device by an approximation based on a small-signal model of GFETs [1], [27], [28]. An average gate capacitance of 42 fF obtained elsewhere [21] for the device used here has been considered. An effective physical gate resistance [26] of 4.9 Ω has been calculated. A contact resistance value (see Table I), required for the intrinsic transconductance and intrinsic output conductance, has been extracted from the experimental data with a method presented elsewhere [27]. The obtained HF FoM have been shown in Fig. 5 for the forward sweep of each technique.

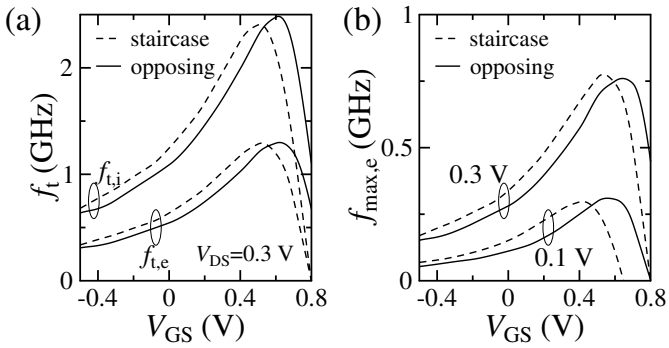


Fig. 5. Trap-affected (staircase sweep) and trap-reduced (opposing sweep) calculated (a) intrinsic and extrinsic cutoff frequency and (b) extrinsic maximum oscillation frequency versus V_{GS} of the device under study.

The magnitude and bias-dependence of the HF FoMs differ due to traps affecting differently the channel potential. The trap-induced bias drift and the value of $f_{t,e}$ and $f_{max,e}$ can affect critically GFET-based HF circuits performance, e.g., by misleading the design for a specific bias point of matching or stability networks connecting the device with other stages of a monolithic circuit [29].

Other transistor performance indicators obtained with the different characterization techniques are shown in Table I at the highest V_{DS} used here. For comparison purposes, V_{Dirac} has been taken as a reference point, i.e., $I_{D,p/n} = I_D|_{V_{GS}=V_{Dirac}\mp 0.5\,V}$, where the subindexes p and n indicate that the data is taken at the p-type ($V_{GS} < V_{Dirac}$) or n-type ($V_{GS} > V_{Dirac}$) part of the transfer curve. The contact

resistance R_{C} has been extracted [27] at the corresponding linear unipolar region of the transistor operation.

TABLE I
TRANSISTOR PERFORMANCE INDICATORS AT $V_{\mathrm{DS}} = 0.3\,\mathrm{V}$ OF THE 300 nm GFET USING DIFFERENT CHARACTERIZATION TECHNIQUES

param.	staircase		opposing	
	forward sweep	backward sweep	forward sweep	backward sweep
V_{Dirac} (V)	0.8	0.9	0.9	0.9
$I_{\mathrm{D,p}}/w_{\mathrm{g}}$ (µA/µm)	31.45	31.41	29.04	29.25
$R_{\mathrm{C,p}} \cdot w_{\mathrm{g}}$ (kΩ · µm)	6.61	7.57	6.97	6.71
$I_{\mathrm{D,n}}/w_{\mathrm{g}}$ (µA/µm)	28.28	29	28.53	28.36
$R_{\mathrm{C,n}} \cdot w_{\mathrm{g}}$ (kΩ · µm)	12.35	13.89	13.5	13.1

The shielding of the channel potential due to traps leads to an offset in V_{GS}, i.e., the same current level is obtained at different applied vertical fields in staircase sweeps. Trap-reduced data enables the reproducibility of these carrier current levels despite the measurement history. Larger differences in the contact resistivity from trap-affected data in comparison to the same parameter obtained with opposing pulses are due to the consideration of a bias range rather than a bias point related to the R_{C}-extraction method [27], i.e., hysteresis in this value is scaled up. A wrong estimation of this parameter could mislead the technology development.

IV. MODELING-ENABLED ANALOG PERFORMANCE ASSESSMENT

The need for an analytical current-voltage (*IV*) model that will accurately predict the behavior of both trap-reduced and trap-affected data is crucial for better comprehending these phenomena. Such a model is proposed in this section based on the one derived in [30] and on the experimental empirical observations presented above. The basic electrostatic equation of a one-gated graphene transistor without the impact of traps leads to an expression for the net charge in graphene given by [30], [31]

$$Q_{\mathrm{net}}(x) = C_{\mathrm{ox}}\left(V_{\mathrm{GS}} - V_{\mathrm{GSO}} - V_{\mathrm{c}}(x) - V_{\mathrm{ch}}(x)\right), \quad (1)$$

where V_{c} and V_{ch} are the chemical and the channel potential at channel position x, respectively. The chemical potential accounts for the voltage drop across the quantum capacitance along the channel. $V_{\mathrm{GS}} - V_{\mathrm{GSO}}$ is the gate voltage overdrive with V_{GSO} used as a model parameter and C_{ox} is the oxide capacitance per unit area. By considering a straightforward approach [30] in which Q_{net} approaches to 0 at the charge neutrality point and the channel potential is averaged over the channel such as $V_{\mathrm{ch}} \sim V_{\mathrm{DS}}/2$, the Dirac voltage is calculated here as $V_{\mathrm{Dirac}} \approx V_{\mathrm{GSO}} + V_{\mathrm{DS}}/2$ [30].

At the presence of traps, Eq. (1) is modified as

$$Q_{\mathrm{net,tr}}(x) = C_{\mathrm{ox}}\left(V_{\mathrm{GS}} - V_{\mathrm{GSO,tr}} - V_{\mathrm{c}}(x) - V_{\mathrm{ch}}(x)\right), \quad (2)$$

with $V_{\mathrm{GSO,tr}} = V_{\mathrm{GSO}} - DV_{\mathrm{tr}} + K_{\mathrm{tr}}V_{\mathrm{DS}}/2$. The term $DV_{\mathrm{tr}} - K_{\mathrm{tr}}V_{\mathrm{DS}}/2$ corresponds to the induced potential due to trap density[1] $N_{\mathrm{tr}} = C_{\mathrm{ox}}(DV_{\mathrm{tr}} - K_{\mathrm{tr}}V_{\mathrm{DS}}/2)/q$ with q as the electron charge. DV_{tr} and K_{tr} are the new defined model parameters where the first corresponds to the shift of V_{Dirac} due to trap impact while the latter embraces the V_{DS} dependence of this shift. Trap-affected V_{Dirac} is now calculated as $V_{\mathrm{Dirac,tr}} = V_{\mathrm{GSO}} - DV_{\mathrm{tr}} + (K_{\mathrm{tr}} + 1)V_{\mathrm{DS}}/2$. In order to incorporate the above effects in the I_{D} model, $V_{\mathrm{GSO,tr}}$ is used instead of V_{GSO} in Eqs. (1) and (4) of [30] for the potential calculation. In contrast to other compact GFET model including the impact of traps [32], a straightforward implementation of the V_{DS}-dependence of a trap-affected Dirac voltage related to hot carriers [2], [33] has been considered here. The latter is an attractive feature to describe the impact of traps in GFET-based circuits at different bias.

The model accurately captures experimental I_{D} and g_{m} data as illustrated in Figs. 2 and 3 for all available sweeps in the p-type region. The asymmetric experimental n-type behavior with respect to the p-type region is not described by the model due to an inherent symmetric condition as discussed elsewhere [17]. In the following, the discussion is for the transistor operating in the p-type region. The extracted model parameters are shown in Table II where μ is the mobility, ρ_0 the residual charge density and $\hbar\Omega$ the phonon energy. The impact of the traps mostly contributes to the shift of the V_{Dirac} through DV_{tr} and K_{tr} parameters which is more intense at the forward sweep while the rest of the model parameters are the same for both trap-reduced and trap-affected data. Having both data sets available, permits a reliable parameter extraction procedure. In more detail, from the opposing sweep all the model parameters apart from $\hbar\Omega$ can be extracted from low V_{DS} regime while the precise fitting of the data at high V_{DS} by just adjusting $\hbar\Omega$ is a good indicator that impact of the traps is negligible; in such case DV_{tr} and K_{tr} are deactivated. The latter are extracted afterwards in forward and backward sweeps.

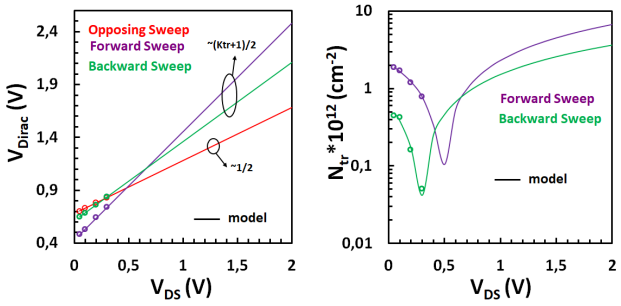
TABLE II
MODEL PARAMETERS FOR DIFFERENT MEASUREMENT SWEEPS

parameter	forward	backward	opposing
μ ($\mathrm{cm^2V^{-1}s^{-1}}$)	135	135	135
V_{GSO} (V)	0.68	0.68	0.68
ρ_0 ($\mathrm{cm^{-2}}$)	1.55×10^{12}	1.55×10^{12}	1.55×10^{12}
$R_{\mathrm{C}}/2$ (Ω)	116	116	116
$\hbar\Omega$ (meV)	10	10	10
DV_{tr} (mV)	250	70	0
K_{tr}	1.05	0.5	0

Fig. 6(a) depicts both experimental and simulated V_{Dirac} for trap-reduced and trap-affected cases versus V_{DS}. The model is extended to higher V_{DS} values where after a point, V_{Dirac} of forward and backward sweeps become larger than the one of opposing case. This can be justified in terms of the different V_{DS} dependence of trap-reduced and trap-affected channel potential. When traps are present, this dependence is $(K_{\mathrm{tr}}+1)V_{\mathrm{DS}}/2$ instead of $V_{\mathrm{DS}}/2$ in the case they are not there, as shown before. Experimental trap density is calculated as $N_{\mathrm{tr}} = \Delta V_{\mathrm{Dirac}} C_{\mathrm{ox}}/q$ where $\Delta V_{\mathrm{Dirac}}$ is the shift of the measured V_{Dirac} such as $\Delta V_{\mathrm{Dirac}} = V_{\mathrm{Dirac-opp}} - V_{\mathrm{Dirac-fwd/bwd}}$, respectively while N_{tr} can be also calculated by the model as mentioned previously. Both are illustrated in Fig. 6(b) versus V_{DS} where the trapping and detrapping processes can be elucidated for voltages lower and higher than the minimum point of the curve, respectively. The minimum point of the $N_{\mathrm{tr}}(V_{\mathrm{DS}})$ plot corresponds to a change of polarity of the term $DV_{\mathrm{tr}} - K_{\mathrm{tr}}V_{\mathrm{DS}}/2$.

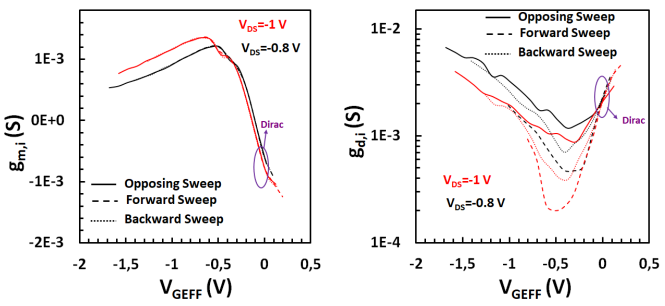
The model results in Fig. 6 confirm the increasing impact of traps with V_{DS} on device performance ellucidated by experimental data, specially on g_{d} (see Fig. 4). Trapping and detrapping processes can be simultaneously enabled at the

[1] Absolute values are considered. See results and discussions of Fig. 6(b)



(a) (b)

Fig. 6. Measured and simulated Dirac voltage (a) and absolute value of the trap density (b) versus V_{DS} for all available sweeps. Markers: data, lines: model. The different slopes of the plots in (a) are pointed out.



(a) (b)

Fig. 8. Simulated intrinsic (a) transconductance and (b) output conductance versus an effective gate voltage V_{GEFF}.

same V_{DS}, e.g., at 0.4 V, where traps are still being filled during a forward V_{GS} sweep while in the backward sweep other traps can either start to release carriers or been enhanced by hot carriers [2], [33] as suggested by the increase of the modeled N_{tr} at this bias point. An accurate calculation and projection over bias of N_{tr} such as the one provided by this model (cf. Fig. 6(b)), is an important information towards improved insights in the device physics, e.g., on the low-frequency noise characterization of GFETs [17].

Synthetic intrinsic gain $G = g_{\mathrm{m,i}}/g_{\mathrm{d,i}}$, calculated with the simulated data[2], is depicted in Fig. 7 for different V_{GS} at the p-type region for two high negative V_{DS} values in order to ensure both the p-type operation of the device and that G exceeds unity. It is evident that traps can affect tremendously this important analog FoM as well by affecting the DC bias point and consequently resulting in a *false-positive* result, i.e., an overestimated trap-affected G that can not be exploited in circuit applications since it depends on the measurement history of the device. A more reliable result is the one obtained with the diminished impact of traps which can be reproduced and used in circuits by using an appropiate biasing scheme.

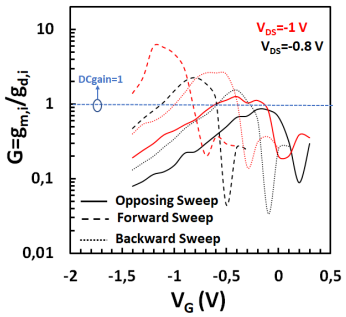


Fig. 7. Simulated intrinsic gain at different bias for all available sweeps.

The higher impact of traps on g_{d} observed in the experiments (cf. Fig. 4) is also confirmed with the model since the larger the V_{DS}, the more trapping/detrapping mechanisms can be enabled (higher N_{tr}). In contrast, the trap-affected I_{D} changes slowly with the vertical applied fields, i.e., g_{m} is mainly shifted in V_{GS} but not in magnitude (N_{tr} shifted in V_{GS}). This is confirmed with the simulated $g_{\mathrm{m,i}}$ and $g_{\mathrm{d,i}}$ plots at different bias shown in Fig. 8.

[2] $V_{\mathrm{GS,i}} = V_{\mathrm{GS}} - I_{\mathrm{D}}R_{\mathrm{C}}/2$ and $V_{\mathrm{DS,i}} = V_{\mathrm{DS}} - I_{\mathrm{D}}R_{\mathrm{C}}$ with R_{C} values of Table II.

The effect of traps can be claimed to be diminished regardless the characterization technique if the difference of V_{Dirac} with V_{GS} is compensated, i.e., by a $V_{\mathrm{GEFF}} = V_{\mathrm{GS}} - V_{\mathrm{Dirac,tr}}$ for the staircase sweeps and $V_{\mathrm{GEFF}} = V_{\mathrm{GS}} - V_{\mathrm{Dirac}}$ for the opposing sweeps. At $V_{\mathrm{GEFF}} = 0$ V the values of the simulated $g_{\mathrm{m,i}}$ and $g_{\mathrm{d,i}}$ are the same for all sweeps at the same V_{DS} as shown in Fig. 8. This implies similar G at such bias. However, the condition of identical trap-affected characteristics required to exploit this feature is challenging to reproduce in practical scenarios since they are strongly affected by the measurement history. Hence, trap-reduced data should be always considered for feasible and reproducible device characteristics.

V. Conclusion

Consecutive opposite bias pulses applied to a fabricated graphene transistor have been used here in order to diminish the impact of trapping processes on the device performance. This biasing scheme is more practical than the holding time approach generally used to obtain trap-reduced data. In contrast to other GFET studies focused on the device response to varying lateral field in the channel, the opposing pulses stressing the gate of the device here have enabled the observation of trapping effects due mainly to available states in the oxide, i.e., the channel potential is shielded from the applied vertical field due to traps. Trap-affected and trap-reduced static characteristics have been experimentally observed and qualitatively discussed. The oftenly overlooked impact of traps in analog/HF figures of merit has been shown here with calculations of the cutoff frequency and maximum oscillation frequency based on experimental data. The dynamic response can differ from the expected due to the DC bias-point drift induced by trapping processes. Trap-reduced data obtained with practical bias schemes, e.g., by the opposing pulse technique, can ease the design of matching networks for GFETs in high-frequency circuits by providing reproducible characteristics.

An analytical drain current model has been able to reproduce trap-reduced and trap-affected data by considering the impact of traps on the device electrostatics. Two empirical factors have been obtained to describe the V_{Dirac} shift and its V_{DS} dependence for the trap-affected data. The straightforward implementation of the latter effect in the compact model enables the study of GFET-based circuits including the trap-affected device performance. The trap density obtained from experimental data has been also reproduced by using the model parameters. The synthetic trap density over bias

reveals also the effect of trapping and detrapping processes. An important analog figure of merit such as the intrinsic gain has been obtained here from the simulated data. Similarly to the HF FoMs (f_{t} and f_{max}), an important difference is observed for this analog metric between trap-affected and trap-reduced results. Traps affect not only the biasing point but the magnitude of the intrinsic gain.

The impact of traps should be considered in both static and dynamic scenarios in order not to spoil the analog/HF performance of GFETs. A practical and straightforward biasing scheme as the one used here as well as the modeling approach presented in this work are convenient for both obtaining the trap-reduced device performance and exploiting the device dynamic characteristics in circuits.

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