Power-efficient Noise-Induced Reduction of ReRAM Cell's Temporal Variability Effects

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***Abstract*—Resistive Random Access Memory (ReRAM) is a promising novel memory technology for non-volatile storing, with low-power operation and ultra-high area density. However, ReRAM memories still face issues through commercialization, mainly owing to the fact that the high fabrication variations and the stochastic switching of the manufactured ReRAM devices cause high Bit Error Rate (BER). Given that ReRAM devices are nonlinear elements, the nonlinear phenomenon of Stochastic Resonance (SR), which defines that an input disturbance with specific characteristics can improve the total performance of the nonlinear system, is used to reduce the ReRAM cell's BER. Thus, in this work, the BER of a single ReRAM cell is explored, using the Stanford PKU model, and is improved after the application of specific additive input noise. The power dissipation of the proposed approach is also evaluated and compared with the consideration of higher amplitude writing pulses in the lack of noise, showing that the proposed noise-induced technique can decrease the BER without the excessive increase of the power dissipation. As a first step, towards the experimental verification of the proposed method, noise-induced measurements on a single fabricated ReRAM device are also performed. Overall, the presented results of the BER reduction with low power dissipation, reaching up to $3.26\times$ less power consumption considering 100 ns writing pulses, are encouraging for ReRAM designers, delivering a circuit-level solution against the device-level problem.**

***Index Terms*—ReRAM devices, Memristor, Variability, Stochastic Resonance, Emerging Memories**

I. Introduction

Internet-of-Things, Big Data, and Artificial Intelligence constitute a great share of the demanding applications that are pushing today's computing systems to their limits [1]. Today's computer capabilities need further scaling up to cover the rapidly increasing demand for information storing and processing. Aiming to continue the scaling up of computers' performance, novel memory technologies are under development to extend the memory capabilities nearby or within the processing units by their ultra-dense packing, re-programmability, and by bringing non-volatile storage inside the chip [2]. In particular, among the emerging memory candidates, the Metal-Oxide Bipolar Filamentary Resistive RAM (ReRAM) stands out, since it presents high scalability and low fabrication cost, long retention and compatibility with 3D-integration, while it performs adequately in terms of latency, energy consumption, endurance, and multi-level computing [3]. However, as indicated in [3], the unique problematic aspect for this category of emerging devices is their variability [4]–[6]. As a result, this major issue of the ReRAM devices affects heavily the commercialization of ReRAM-based products, due to the reduced robustness of such systems.

In this letter, the nonlinear phenomenon that is known as Stochastic Resonance (SR) [7] is utilized against the negative effects of the device's stochasticity on memory applications. In particular, a single ReRAM cell's temporal (cycle-to-cycle) variability, which strongly affects the Bit Error Rate (BER) of ReRAM memories, is exposed to a noise-induced SR-based writing method, showing rather interesting reduction of BER and resulting to an increased system's performance. More specifically, SR describes how a noisy input excitation can achieve better output performance compared to the original non-noisy input. The concept of exploiting SR on memristor's switching enhancement was, firstly, explored in [8] by introducing internal stochasticity to the memristor model, as well as in [9], where the external application of additive noise was investigated, showing that memristor's maximum to minimum resistance ratio can be enhanced. Given that the aforementioned ratio affects the read margins of a ReRAM-based memory and that the ReRAM-device switching is attributed to highly nonlinear physical mechanisms, this work focuses on the Bit Error Rate (BER) of single variability-aware ReRAM cell and utilizes SR on the BER's reduction with additive noise along with the writing pulses, reaching up to $3.26\times$ less power consumption. Likewise, for the first time, the power consumption of the noise-induced approach is investigated as a practical advantage of the method and is bench-marked against the sweep of the writing pulses' amplitude without the presence of input noise. As a proof of concept, the noise-induced approach is tested on a standalone fabricated Hafnium Oxide device, illustrating the beneficial effect of the additive input noise on actual Metal-Oxide ReRAM devices.

II. ReRAM Cell and Bit Error Rate

The modeling of two-terminal thin-film devices like ReRAMs, is yet a non-trivial procedure; thus, currently, there is a vast amount of various models in the literature [10], [11]. In this work, the Stanford-PKU ReRAM device model [12] has been utilized because it is a physics-based model, which can accurately describe the behavior of actual oxide-based

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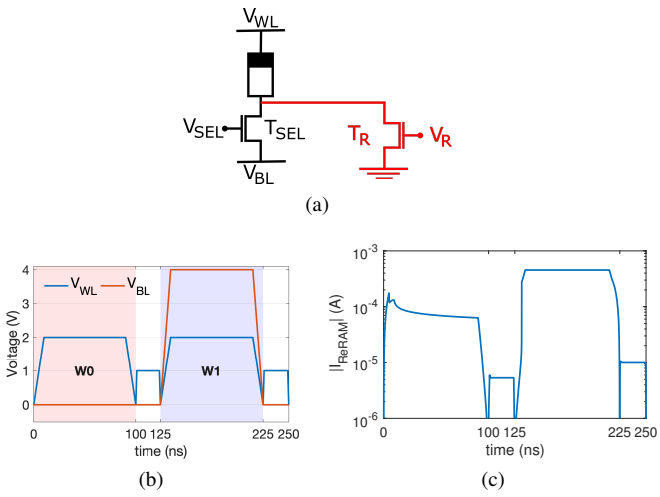


Fig. 1. (a) ReRAM cell circuit. (b) V_{WL}, V_{BL}, and (c) $|I_{ReRAM}|$ during a $W_0 - R_0 - W_1 - R_1$ cycle.

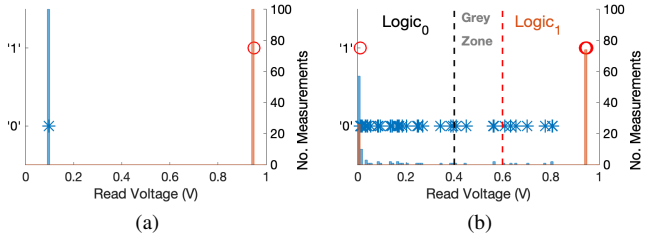


Fig. 2. Distribution of read values for a benchmark scheme using the Stanford-PKU ReRAM model without (a) and with (b) temporal variability. The symbols correspond to R_0 (stars) and R_1 (circles) readings, while the bars to the R_0 (blue) and R_1 (orange) distributions (right axis).

ReRAM devices by modeling the conductive filament's (CF) growth within the insulating layer of the device. Furthermore, the Stanford-PKU ReRAM device model has been developed on Hafnium Oxide Metal-Insulator-Metal devices [13] exactly like the experimental device employed in Section V, enabling a good estimation of the behavior of the fabricated devices. In addition, one of the most significant features of this model is its ability to incorporate the device's current fluctuations by employing stochastic processes in the growth of the CF, causing the temporal variation of the device that results in the increased BER of the ReRAM-based memory cells.

Using this ReRAM device model, the functionality and the circuitry of a ReRAM memory cell is now explored. More specifically, logical '0' (logical '1') is mapped to the device's high (low) resistive state, which can be written to the cell by the application of a strong negative (positive) voltage. Since the resistance value cannot be read directly, the reading process comprises a short-amplitude positive pulse that maps the resistive state to voltage with the assistance of a properly-gated reference read transistor T_R, based on the voltage divider between the ReRAM device and the resistance of T_R (Fig. 1(a)). The circuit configuration of such a cell is rather simple due to the memory capabilities of the ReRAM device which can maintain its resistive state without the need for any refresh voltage. So, the cell's circuit (Fig. 1(a)) is composed of the ReRAM device in series with a transistor-selector T_{SEL} that also performs a protective current-limiter, while the write and read signals are applied through the Bitline (V_{BL}) and the Wordline (V_{WL}), respectively. For performing the reading process, T_R is mainly used like here, i.e. inside the cell, to implement the necessary voltage divider able to distinguish the two states. However, in a large array, T_R will be modified according to the corresponding reading scheme. The stored cell bit is read at the intermediate node, during the reading process when T_{SEL} is open and T_R is closed.

In Stanford-PKU model, the RESET (W_0) and SET (W_1) processes can be performed by applying negative and positive pulses, accordingly, with amplitude $V_W = |2|$ V and pulse width $\tau = 80$ ns. Also, the rising and falling edge duration of each pulse is $\tau_{r/f} = 10$ ns, resulting in a total of 100 ns per writing pulse [12]. Figs. 1(b)-(c) illustrate a cycle of ReRAM cell programming, consisting of a W_0 and a W_1 pulse and a corresponding R pulse, with $V_R = 1$ V and shorter duration $t_{read} = 25$ ns, after each writing pulse, defined as a $W_0 - R_0 - W_1 - R_1$ cycle. Fig. 1(b) shows the applied Word-Line voltage V_{WL} (blue) and Bit-Line voltage V_{BL} (orange), while Fig. 1(c) illustrates the modulus of current through the ReRAM device in log-scale. All the simulations have been performed with the SPECTRE simulator in the Cadence Virtuoso platform.

For memory devices, the BER is an essential metric to evaluate the robustness of the system. The BER is calculated as the percentage of wrongly written bits out of the total amount of writing processes. To further investigate the effect of the ReRAM device's temporal variability to the BER, the Stanford-PKU model's feature for stochastic fluctuations of the CF's growth is utilized. In particular, by adjusting the values for the intensity of CF's gap and width fluctuations ($\{\delta_g, \delta_r\}$) of the model [14], the ReRAM cell's BER is modified.

To measure the ReRAM cell's BER, a benchmark scheme has been set up. In detail, this benchmark scheme is a set of 100 $W_0 - R_0 - W_1 - R_1$ cycles applied to the ReRAM cell and the voltage across the reading transistor T_R in the middle of the reading pulses is used to evaluate the correctness of the previously applied writing process. By measuring the voltage across the reading transistor, the current resistance value of the ReRAM device can be extracted using the formula of the voltage divider. Practically, this benchmark scheme succeeds to measure the BER of each of W_0 and W_1 processes with 1% accuracy, while the alternation between them stresses the device's switching dynamics and amplifies the effect of variability. Figs. 2(a) and (b) present the distribution of the read voltages during R_0 and R_1 of one paradigmatic benchmark simulation without and with CF fluctuations, accordingly.

In the lack of fluctuations, it is clear that there is no temporal variability, so the read voltage after every writing process is fixed. On the contrary, the results in the case with fluctuations are scattered. Firstly, the read voltage after W_0 is distributed throughout almost all the range of possible values, with higher number of occurrences on the lower part of this range. On the other hand, after W_1 the read voltage is mostly at the same value as in the no-fluctuations case. However, there is a considerable number of cases that the writing pulse was not able to SET the ReRAM device due to its previously achieved very high resistance state. To calculate the BER of the performed simulations, the erroneous bits of W_0 (W_1)

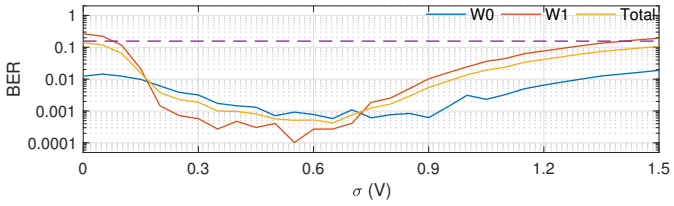


Fig. 3. BER scaling for W_0, W_1 and Total BER of the ReRAM cell with additive noise for 300 benchmark schemes per σ value. The purple dashed line depicts the average BER without external noise source.

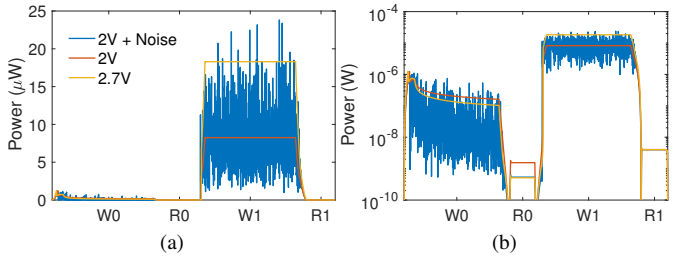


Fig. 4. Power dissipation during a benchmark cycle $W_0 - R_0 - W_1 - R_1$ with ($\sigma = 0.35$V) and without noise in (a) linear and (b) logarithmic scale.

processes are identified when the reading value belongs either to the Logic$_1$ (Logic$_0$) area or the Grey zone area, i.e. for a read voltage higher than 0.4 V (lower than 0.6 V). These limits are depicted in Fig. 2(b) by the vertical black and red dashed lines that were selected appropriately to define a Grey zone where the cell's logic state is unidentifiable.

The presented simulation results for the fluctuations case were acquired with $\{\delta_g, \delta_r\} = \{1, 5\}$, which are much higher than the values originally proposed in the Stanford-PKU model [14]. However, the selected values enable the successful study of the temporal variability without the need for long and time-consuming simulations with thousands of pulses.

III. Stochastic Resonance Approach

To study the potential improvement of the ReRAM cell's BER, the writing pulses, both W_0 and W_1, have been enriched with additive white Gaussian noise to assist on the activation of RESET and SET processes. White noise signals, theoretically, cover all the frequency spectrum, so they contain a small portion of every frequency; however, during the simulations, the maximum achievable frequency is constrained by the simulation step. Nevertheless, the ReRAM devices are less affected by signals with higher frequency than their operational frequency because their switching capabilities are diminishing with the increase of frequency and they act as a regular fixed-value resistor. Albeit, in this study, the white noise signal functions in an auxiliary way to the writing signal by assisting to the activation of the device switching; while, the additive noise signals are generated by a zero-mean Gaussian Process ($<\xi>= 0$) with covariance function $<\xi(t)\xi(t')>= \sigma^2\delta(t-t')$. Preliminary results on a small crossbar array [15] revealed that this kind of noise can be beneficial.

Using the benchmark scheme to evaluate the BER, a set of simulations with the same parameters of the temporal variability example of Fig. 2(b) has been executed, with the integration of additive noise in the V_{WL}. In specific, the additive Gaussian noise has a mean value of $\mu = 0$ V, while the

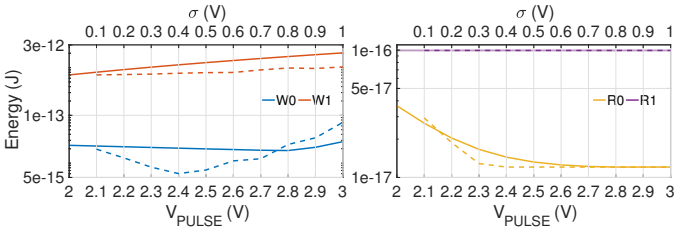


Fig. 5. Total energy consumption for each pulse of the $W_0 - R_0 - W_1 - R_1$ cycle for varying V_{PULSE} and σ. Full (dashed) line corresponds to the amplitude (noise intensity) sweep and is mapped to the bottom (top) x-axis.

standard deviation σ is varying. Fig. 3 presents the evaluated BER of W_0, W_1 and the Total BER in regards to the value of σ in each simulation, in the range $\sigma = [0.05, 0.1, ..., 1.5]$ V. For each value of σ, 300 benchmark simulations are performed and the average is illustrated in Fig. 3, whilst the average BER without additive noise is indicated by the purple dashed line.

The acquired results indicate a positive impact of the additive noise against the BER. In details, the BER of W_1 processes was reduced to zero, using $\sigma > 0.2$ V, which indicates that the noise assisted to the activation of the SET process of the ReRAM device and the "stuck-at-zero" cases of Fig. 2(b) (orange circles at Logic$_0$ regime) were diminished. On the other hand, the BER's improvement for the W_0 processes is lower but stronger noise signals are required to achieve zero BER values. In total, as it is anticipated by the SR theory, the noise-induced performance improvement follows a curve that exhibits a peak value for a specific noise's intensity, corresponding to the value of σ, and beyond that peak the improvement is reduced, leading to a detrimental effect of noise on the performance, as illustrated in Fig. 3.

IV. Power Dissipation

While the use of additive noise to reduce the ReRAM cell's BER presents positive results against temporal variability, it is not the only method to tackle with it. A more common way to counterbalance the negative effect of temporal variability and decrease the BER of memory is to increase the amplitude of the writing pulses [16]. As long as the ReRAM device is a resistive element, the amplitude increase of the applied voltage V results to the ReRAM cell's power dissipation increase in a nonlinear way, following the formula $P = V^2/R$, where P is the dissipated power and R the resistance of resistive element.

Thus, in this Section, the power dissipation of the proposed approach is under study. In particular, the proposed approach is compared with the increase of writing pulse amplitude without noise, taking into account both the power consumption and the BER of each case. First of all, the power dissipation of a sole $W_0 - R_0 - W_1 - R_1$ cycle without device variability is studied, in order to evaluate the power dissipation of each pulse of the cycle, individually. In Fig. 4, the power dissipation for the original writing pulse amplitude $V_{PULSE} = |2|$ V is illustrated in comparison with the power dissipation of a no-noise pulse with $V_{PULSE} = |2.7|$ V and a noisy one with $V_{PULSE} = |2|$ V and $\sigma = 0.35$ V, as an example. It is clear that the most power-hungry processes are the W_1 and R_1, because the ReRAM device is driven towards the low resistance state and the current through the device is

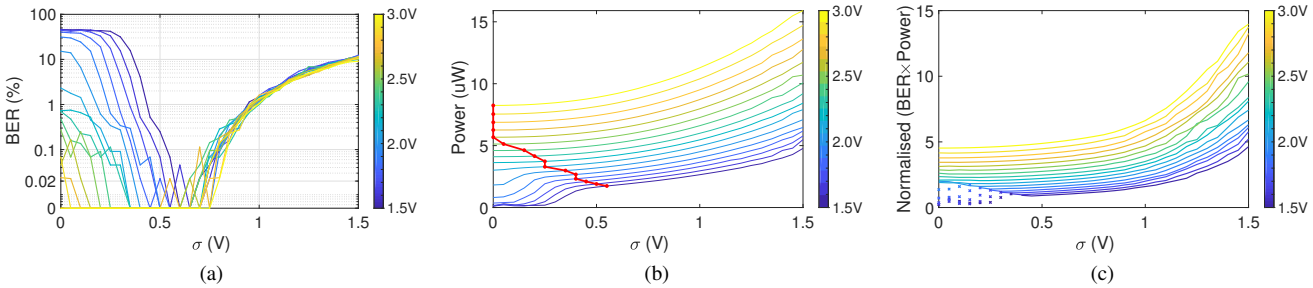


Fig. 6. (a) BER, (b) Power dissipation and (c) normalized BER×Power product for all the V_{PULSE} and σ combinations. The red line in (b) depicts the minimum power dissipation case per V_{PULSE} with minimum BER.

higher. Between the different applied signals, during the W_0 and R_0, the original signal is not able to drive the ReRAM device to very high resistance value and, as a result, the power consumption is higher than the other two signals. During the W_1, all the signals can achieve the lower resistance state, so the more voltage is applied, the more power is dissipated. Moreover, the noisy signal has a mean value of $\mu = 0V$, and, as a result, the applied voltage is fluctuating around the V_{PULSE}, maintaining the power dissipation close to the original case. Finally, during the R_0, the current through the device is limited by T_R, and, consequently, all the signals exhibit the same amount of dissipated power.

In a more detailed illustration of the power dissipation, Fig. 5 shows how the amount of dissipated power is scaling with the increase of the V_{PULSE} and compares it with the increase of σ with fixed $V_{PULSE} = 2$ V (dashed lines corresponding to the top x-axis) for each pulse of the $W_0 - R_0 - W_1 - R_1$ cycle. The power dissipation in Fig. 5 is presented in the logarithmic scale and the superiority of the additive noise approach is clear in the W_1 process, the most power-hungry case. For the W_0 process, the additive noise approach can achieve the maximum resistance state before the other case, as it can be deducted from the corresponding R_0 line; however, for higher σ it consumes more power. Overall, the additive noise approach can achieve lower power dissipation than the case with increasing V_{PULSE}.

In the following, further exploration of power dissipation is performed for different values of V_{PULSE} within all the range of σ. For reasons of comparison, the benchmark scheme is utilized and the BER for every simulation is evaluated along with the total power dissipation during the scheme. As long as both the intrinsic current fluctuations of the ReRAM devices and the external additive noise are generated through stochastic processes, a single simulation cannot illustrate sufficiently the performance of the system for a specific set of V_{PULSE} and σ. Thus, 20 simulations per $\{V_{PULSE}, \sigma\}$ pair are performed to evaluate the average BER and average power dissipation of each pair, which are presented in Figs. 6(a) and (b), respectively. More particularly, the value of σ is shown in the x-axis, while the various V_{PULSE} values are mapped to the line color, corresponding to the right-side colorbars.

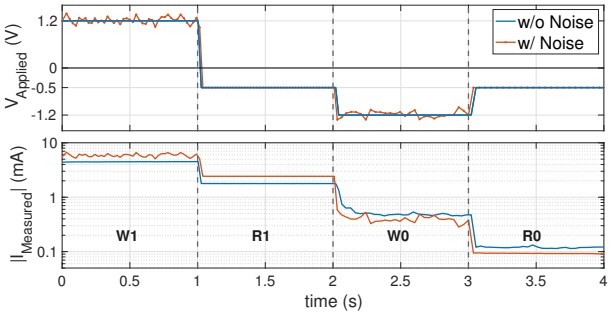
Focusing on the Fig. 6(a), one can observe the significant reduction of BER for a specific range of σ, in full agreement with the results of the previous section, for every V_{PULSE} value. Nevertheless, out of this range, either a higher V_{PULSE} is required (for $\sigma < 0.5$ V) or the noise signal is strong enough to corrupt the writing process (for $\sigma > 0.9$ V). Although the BER's reduction can be achieved by both approaches, the additive noise one is lower on power dissipation, as shown in Fig. 6(b). In particular, even for high σ values, the power dissipation of the noisy signals with low V_{PULSE} is half compared to the no-noisy cases with high V_{PULSE}. However, low power dissipation is also shown in the case with increased BER because the ReRAM devices stuck at the high resistance state. The red line in Fig. 6(b), which illustrates the minimum BER cases with the lowest dissipated power per V_{PULSE}, clarifies the power-efficiency of the proposed method as the ratio between the optimum no-noise ($\{2.6\text{V}, 0\text{V}\}$) and noise-induced ($\{1.5\text{V}, 0.55\text{V}\}$) case for 100 ns writing pulses is $k = P_{\{2.6\text{V},0\text{V}\}}/P_{\{1.5\text{V},0.55\text{V}\}} = 5.68\mu\text{W}/1.74\mu\text{W} = 3.26$.

Additionally, the combination of the BER and the power dissipation is illustrated in Fig. 6(c) through the product BER×Power. As long as the increase in either of those two metrics is affecting negatively the quality of the system, their product can depict the aggregate improvement in regards to $\{V_{PULSE}, \sigma\}$. The values in Fig. 6(c) are normalized by the value of the nominal case {2V, 0V} and the value of BER is used as "1+BER" for the better comparison of the zero-BER cases. The points with low power dissipation but higher BER than the nominal, are discarded (i.e. dots in Fig. 6(c)) because their low power is attributed to the insufficient W_1 process, so the ReRAM device is stuck at low current state.

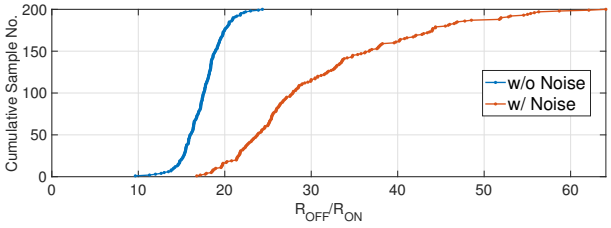
V. SR on Experimental Devices

In order to show a proof-of-concept of the noise-induced SR benefits on the advantageous Filamentary ReRAM devices, a set of experiments on a Hf-based ReRAM device is held. Moreover, the pulse programming scheme of the previous sections is adopted, targeting an actual application of SR in ReRAM-based memories. To do so, the SPA Agilent 4156C is utilized to both apply voltage on and measure the current through a tested ReRAM device, which consists of a 5×5 μm^2 TiN/Ti/10nm HfO_2/W structure. The applied voltage and the measured current for a $W_1 - R_1 - W_0 - R_0$ programming cycle are illustrated in Fig. 7(a) for both cases, namely without and with noise. In the experimental setup, the tested ReRAM sample is forward polarized, thus a positive (negative) voltage results to the SET (RESET) of the device.

Investigating the presence of SR in such devices, the same ReRAM sample is exposed to a set of 400 consecutive



(a)



(b)

Fig. 7. (a) Applied voltage and measured current during a $W_1 - R_1 - W_0 - R_0$ cycle. The blue lines show a case without noise and the orange lines represent one stochastic realization of the noisy cases. (b) Cumulative distribution function plot of the R_{OFF}/R_{ON} ratio without (blue) and with (orange) additive input noise.

programming cycles, half of them without noise and the rest with additive noise during the writing pulses. Restricted by the sampling capabilities of the instrumentation, long-width (1s) and low-voltage ($\pm$1.2V) writing pulses are applied, as well as, for the noisy cases, while the additive noise is produced by zero-mean Gaussian process through Matlab with $\sigma = 75$mV and sampling time ≈ 10ms. As a figure of merit, the R_{OFF}/R_{ON} ratio is calculated for every single programming cycle using the values of the measured current during the reading pulses. The cumulative distribution functions are illustrated in Fig. 7(b), where the blue line represents the part without noise and the orange line the results of the noisy part. It is evident that noise-induced programming achieves a higher ratio. A complementary in-depth investigation of experimental part is subject to further on-going research, aiming to enhance method's application to ReRAM crossbar arrays.

VI. Conclusions

In this work, the Bit Error Rate (BER) of a ReRAM-based memory cell is explored and a power-efficient method based on the Stochastic Resonance (SR) phenomenon is proposed for BER reduction. More specifically, ReRAM devices exhibit inherent stochastic switching that results in the high BER of ReRAM-based cells. Aiming to tackle this issue, a noise-induced method for the successful writing of ReRAM-based cells is proposed, where additive white Gaussian noise is integrated to the writing pulses, following the principles of SR. Even though the external additive noise can be considered as nuisance, the performance of the system, evaluated by the BER, is subject to improvement for a specific range of the noise intensity. Moreover, the proposed method is compared with the amplification of the writing pulses without the presence of additive noise, which can also achieve BER reduction. However, the efficiency of the proposed method becomes prominent when the effect on the combination of BER and Power dissipation is considered, showing that it is able to reduce the BER with low power dissipation, reaching up to 3.26$\times$ less power consumption at minimum BER for a 100 ns pulse width consideration. Moreover, an early proof of concept of the proposed technique is provided through fabricated experimental devices. Thus, throughout this manuscript, a circuit-level method is presented, both through experiments and simulations, to provide a solution to the device-level problem of the temporal variability that still affects the commercialization of the ReRAM-based memories. The proposed scheme can be conveniently adopted by ReRAM arrays with a single noise generator circuit in array's periphery, shared row/column-wise throughout the array during the writing process. The next immediate steps of this work comprise addressing of potential implementation constrains of noise scheme, enhancement of the proposed scheme using optimized pulse width, and in-depth experimental investigation.

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