Modeling of the degradation of CMOS inverters under pulsed stress conditions from 'on-the-fly' measurements

A. Crespo-Yepes[1*], R. Ramos[1], E. Barajas[2], X. Aragones[2], D. Mateo[2], J. Martin-Martinez[1], R. Rodriguez[1], and M. Nafria[1].

[1]Dept. of Electronic Engineering, Autonomous University of Barcelona (UAB) Bellaterra, Spain.

[2]Dept. of Electronic Engineering, Polytechnic University of Catalunya (UPC), 08034, Barcelona, Spain.

* albert.crespo@uab.cat / albert.crespo@uab.es

***Abstract*— In this work, an 'on-the-fly' measurement technique for the monitoring of CMOS inverters performance degradation is presented. This technique allows the characterization of the circuit degradation simultaneously with the applications of the stress. In our experiments, the inversion voltage (V_{INV}) shifts measured during the application of pulsed voltage stresses at the input. It is demonstrated that the shifts can be described by a power law that accounts for the stress time and voltage dependences. Moreover, the circuit degradation has been correlated to the NMOS and PMOS degradations. The results show that the degradation of the CMOS inverter can be evaluated from an analytical equation that considers only the shifts of two parameters (threshold voltage V_{TH}, and mobility μ) of the two transistors in the inverter.**

Keywords*— CMOS technology; 'On-the-fly' stress characterization; circuit performance degradation; transistor aging; CMOS inverters; measurement technique; analytical modelling.

I. INTRODUCTION

Reliability issues are of great concern in ultra-scaled CMOS technologies.[1]. Aging mechanisms activated depending on the biasing applied at transistor's terminals, such as Bias Temperature Instabilities (BTI) and Hot Carrier Degradation (HC), have been largely studied and characterized, and different techniques have been designed for an accurate monitoring of the degradation at device level [2-3]. However, works devoted to the measurement of circuit aging are much more limited [4], probably because of the intrinsic experimental complexity and the difficulty in stablishing device-circuit data correlations. Moreover, aging under dynamic stresses should be addressed, because they are closer to circuit operation [5], although this implies the use of convoluted set-ups, which increases the complexity of the experiments and data analysis. In this regard, since inverters are fundamental blocks in many other complex circuits, the study of their reliability is of great interest and must be understood [5-7]. Besides, because of their much simpler structure, the analysis of CMOS inverters performance after aging allows evaluating correlations between circuit and device parameters [8].

In this work, the degradation of CMOS inverters is experimentally studied under pulsed stress conditions. With this purpose, an 'on- the- fly' type technique is proposed to measure the CMOS inverter performance shifts under these conditions. This technique allows obtaining the inversion voltage (V_{INV}) of the CMOS inverter simultaneously with the application of the stress, avoiding the necessity of stopping the stress to characterize the circuit performance. It is thanks to the application of pulses at the input which produce variations of V_{IN} and V_{OUT} from a low to a high voltage. This fact allows a more accurate time dependence modeling of the performance variation since the V_{INV} is continuously recorded during the stress application. In this regard, it is shown that the aging of the inverters can be described using a power law model, which is used to predict the circuit lifetime at operating conditions. Therefore, the on-the-fly technique proposed in this work provides larger time resolution than conventional setups, where the characterization of the circuit performance requires the interruption of the stress.

In addition, it is demonstrated that the performance degradation of this circuit can be also described using a well-stablished CMOS inverter analytical model. This model describes the circuit aging from the MOS transistor equations in the saturation regime, taking into account the devices aging, given by the variation of the threshold voltages and mobilities of the two transistors, for different stress voltage conditions.

II. Experimental setup and Samples

The inverters were manufactured in a commercial 65nm CMOS technology, with *W/L*=180µm/60nm (W split in 45 fingers). The nominal operating voltage of this technology is 1.2V. By adding some elements, these inverters were configured as Linear Power Amplifiers [9], whose aging under mixed DC and RF conditions was described elsewhere [10]. The performance of these inverters has been characterized using as metrics the inversion Voltage (V_{INV}), i.e., the voltage at which $V_{OUT} = V_{IN}$, and the Driving Current (I_{DD}) [10]. In this work, we mostly focus the attention on the shift of V_{INV} because it can be measured using standard equipment, when considering pulsed stress conditions.

A specific set-up has been implemented for the 'on-the-fly' type characterization of the inverter degradation, i.e., the performance of the circuit (V_{INV}) is simultaneously and periodically measured during the application of the pulsed stress. Thanks to the pulsed waveforms applied at the input during the stress, transitions from low to high voltage in the input and output of the CMOS inverter are used to obtain the V_{INV} (i.e., V_{IN}=V_{OUT}). A Pulse Generator (PG) is used to apply the pulsed stress to the inverter input and a Digital Storage Oscilloscope (DSO) to measure the inverter output (Fig. 1A). With this set-up, the inverters were stressed using pulsed voltages (with V_{IN}=V_{DD}, i.e., the amplitude of the pulse is set to V_{DD}). Different pulse amplitudes (2.3, 2.4, 2.5 and 2.6V) were analyzed, to study the effect of this magnitude on the aging. It must be considered that to be able to measure V_{INV} with a high resolution, suitable times for the voltage transitions (i.e., rise and fall time of the pulse) must be selected. In this work, results corresponding to f=200Hz, t_{rise}= 2.2ms and t_{fall}=2.2ms are shown, as an example of the typical observed behavior. A typical input waveform is shown in Fig. 3 (left) (blue curve). The total stress time was 3600s. With this set-up, V_{INV} is continuously monitored during the stress of the circuit, so that the temporal evolution of this parameter can be evaluated.

A Semiconductor Parameter Analyzer (SPA, Keithley 4200, with four Source Measure Units, SMUs) was used to register the electrical characteristics of the fresh inverters and transistors (that is, before any stress), and also at the end of the pulsed stresses, as shown in Figure 1B. In particular, the transfer curves and I_{DD} of the inverters and the I_D-V_G curves

of the NMOS and PMOS transistors were measured. From the differences between the performances measured before and after the stress, the aging of the circuits was evaluated, from the variation of V_{INV} (ΔV_{INV}) and I_{DD}, and also the aging of the devices, using the Threshold Voltage (V_{TH}) and Mobility (μ) as parameters. In some cases, the pulsed stress was interrupted (at intervals of 900s) and the device aging was measured with the second set-up (Fig. 1B), to evaluate the temporal evolution of the device and inverter degradations.

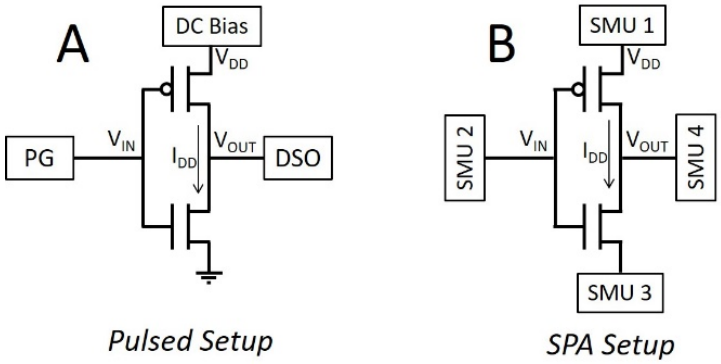

Figure 1: Measurement scheme for: (A) 'On-the-fly' type pulsed stress and measurement set-up of the inverters and (B) SPA set-up for circuit and device aging characterization.

III. Experimental Results

Figure 2 shows the typical evolution of the circuit and device degradations with the stress time, after a pulsed stress. At circuit level, the degradation is observed as a shift of the transfer curves (V_{OUT}-V_{IN}) and the Driving Current (I_{DD}) of the inverter (figures 2A and 2B, respectively). These figures show that V_{INV} progressively increases and I_{DD} decreases with the stress time.

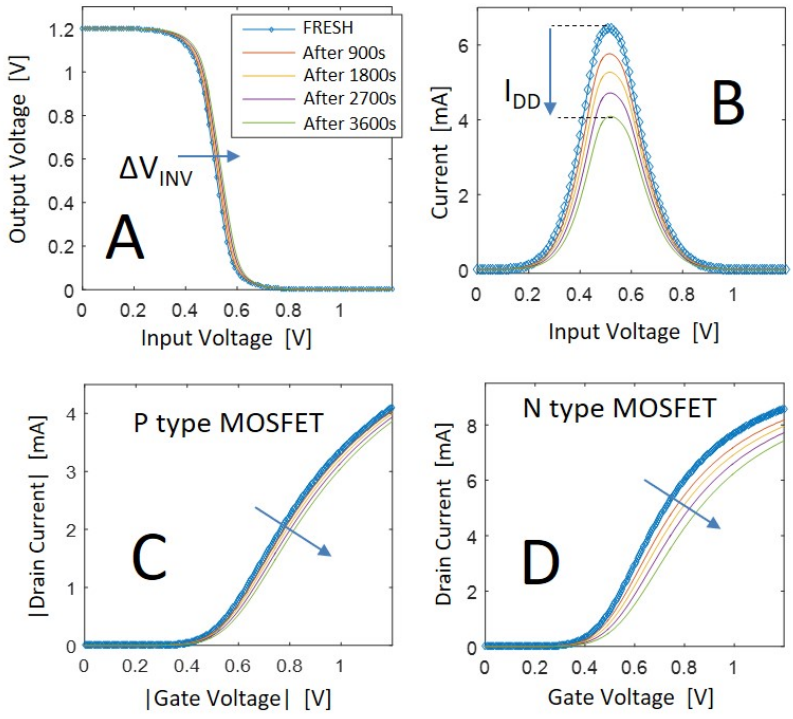

Figure 2: Shifts of the (A) transfer curve and (B) I_{DD}-V_{IN} characteristics of the CMOS inverter, and (C) PMOS and (D) NMOS I_D-V_{GS} characteristics. The curves were measured with the setup in Figure 1.B, when the pulsed stress was interrupted.

The degradation of the circuit performance is caused by the aging suffered by the MOS transistors in the inverter. In this regard, Figures 2C and 2D show the I_D-V_{GS} characteristics of the PMOS and NMOS transistor, respectively, of the fresh device (blue circles) and degraded (colored lines). Note that the fresh V_{TH} is 0.4V and 0.45V approximately for the nMOS and the pMOS, respectively. Because of the degradation, an increase of V_{TH} (in absolute value) and a decrease of μ are observed [11]. These aging effects are related to the generation of defects in the device dielectric [12]. Note that larger shifts of the NMOS V_{TH} and μ are detected, suggesting that, in this technology and under these pulsed conditions, NMOS aging is more relevant than that of the PMOS. Although in a circuit, several aging mechanisms are combined, the experimental results suggest that HCI is probably the dominant degradation mechanism in this circuit [11].

Examples of the input voltage applied (blue line) and of the output voltage measured during one stress period (red line) using the set-up in Fig. 1 A are shown in Figure 3 (left). As it can be seen, when the input voltage progressively approaches V_{INV}, a fast switch of the output voltage is registered. In Figure 3 (right), these transitions before (blue circles) and after 900s of 2.6V pulsed stress (red circles) are compared. An appreciable increment of V_{INV} can be observed (Fig. 3 right), in agreement with the measurements obtained with the SPA (Fig. 2A).

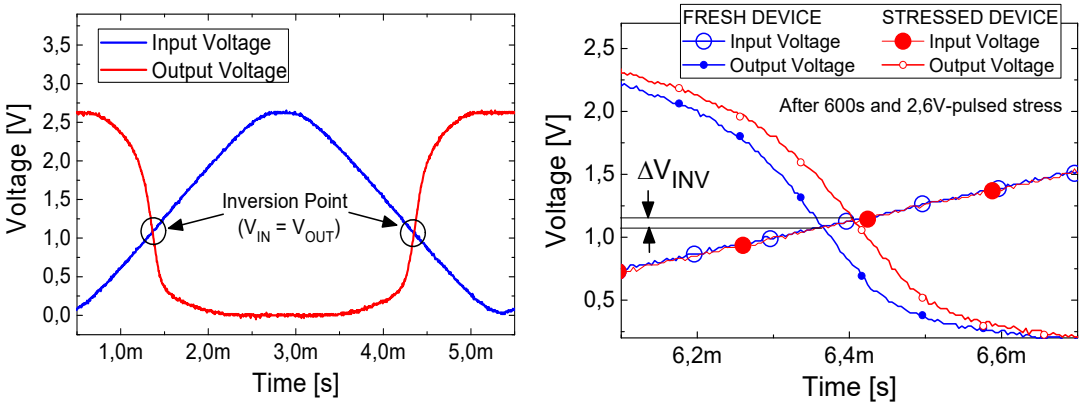

Figure 3: (left) Input (blue line) and Output (red line) voltages captured by the DSO during a 2.6V pulsed stress. (right) Input (solid circles) and Output (open circles) voltages captured before (blue circles) and after (red circles) 900s of 2.6V pulsed stress (with V_{DD} = 2.6V).

Figure 4 shows the evolution of the increment of the inversion voltages (ΔV_{INV}), with respect to the pristine device, when measured simultaneously to the application of the stress (as shown in the example of Fig. 3 right) for the studied pulse amplitudes. Note that a noisy evolution of the inversion voltage is obtained, that can be attributed to the intrinsic noise of the set-up and the DSO resolution. In the range of stress times considered (approx. 1 hour), the degradation progressively increases, being larger for the larger stress magnitudes, as expected. The experimental data in Fig 4 (left) has been fitted to a double power law function (equation 1) which simultaneously accounts for the stress voltage (V_{stress}) and stress time dependences. All the curves have been fitted simultaneously, so that a unique set of parameters A, B and C is able to describe the experimental data. In our case, A= $4.0565 \cdot 10^{-6}$, B=0.3766 and C= 6.434.

$$\Delta V_{INV} = A \cdot t^{B} \cdot V_{STRESS}^{C} \qquad \text{Eq. 1}$$

The equation 1 can be used to extrapolate the inverters degradation at other operating conditions (voltage and time). As an example, Figure 4-right shows the colored map of the variation of V_{INV}, represented as a function of the stress voltage and the stress time, as evaluated from equation 1, with the obtained parameter set. The voltage dependence allows extrapolating the degradation to operating conditions (i.e., 1.2Volts), while the time dependence allows analyzing the circuit lifetime given a failure criterion, for example 100mV of V_{INV} variation. In the figure, the red line indicates the arbitrarily considered failure criterion of the circuit (100mV in our example). Note that at 1.2V, the V_{INV} shift (~20mV) is far below the failure criterion within a 10 years of operation period (as one should expect for a commercial technology). Note that the circuit lifetime exponentially decreases with the applied voltage. However, the circuit can stand voltages as large as 1.5V, maintaining the expected lifetime of 10 years.

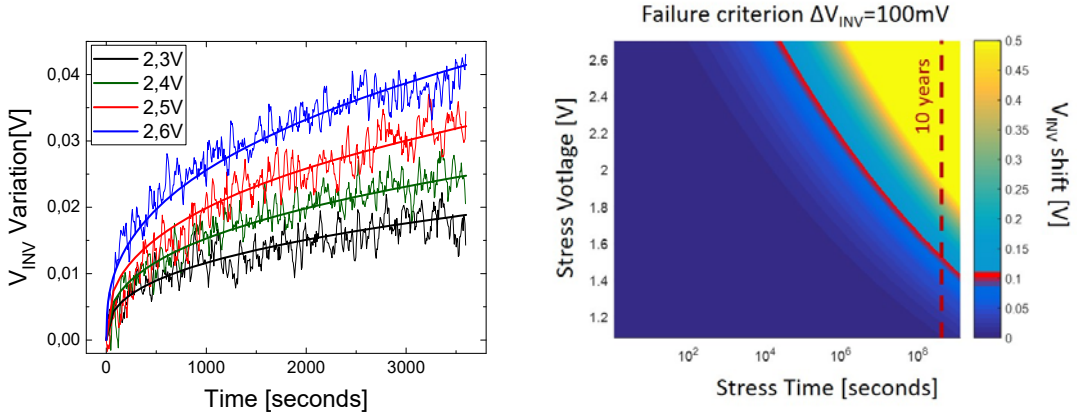

Figure 4: (left) Evolution of the CMOS Inverter inversion voltage (ΔV_{INV}) measured simultaneously to the pulsed stress (setup in figure 1A), for different stress voltages (from 2.3 to 2.6V). The noisy curves correspond to the experimental data and continuous lines to their fitting to eq. 1. (Right) Colored map of the V_{INV} degradation as a function of the stress voltage and stress time, evaluated using Equation 1. The red continuous line corresponds to the considered failure criterion (V_{INV} shift of 100mV) and dashed line to the expected 10 years lifetime.

To correlate the circuit and device degradations, the dependences of the circuit and device performance metrics on the stress voltage and time have been evaluated. To analyze the voltage dependences, the degradations of the circuit and transistors at the end of the pulsed stress (measured with the SPA) have been plotted in Figure 5 and 6, respectively. Figure 5 shows a larger dependence of the I_{DD} shifts on the pulse amplitude than ΔV_{INV}, which results in a change of ~5% for ΔV_{INV} versus ~30% for ΔI_{DD} at 2.6V.

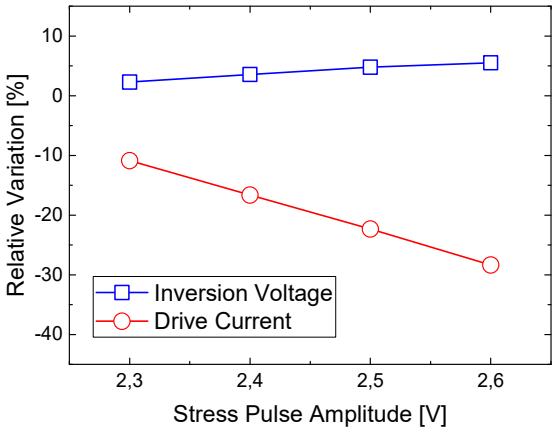

Figure 5: V_{INV} variation (blue squares) and drive current reduction (red circles) as a function of the stress pulse amplitude, after 1 hour of stress.

The transistors degradation is evaluated from the relative variations of V_{TH} and μ obtained from the I_D-V_G curves measured at the end of the stresses. Figures 6 A and B show that larger relative variations of V_{TH} and μ are observed in the case of the NMOS, being the μ of the NMOS the most affected parameter. These figures suggest that ΔV_{INV} is mainly related to the NMOS V_{TH} shifts, while the relative decrease of I_{DD} seems to be related with the NMOS μ reduction. In addition, the degradations of both transistor parameters present an almost linear dependence with the pulse amplitude (in the analyzed range), as the circuit parameter shifts do, which indicates a clear correlation between the shifts of the circuit/transistor parameters.

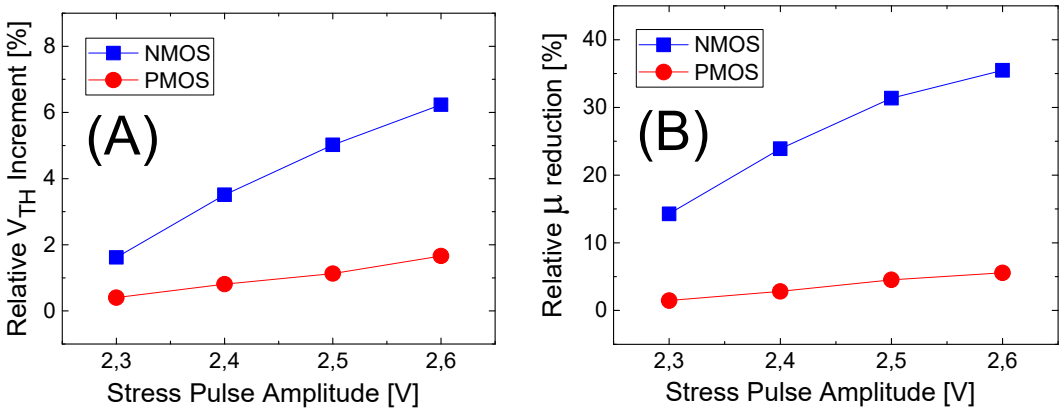

Figure 6: Relative variations of (A) V_{TH} and (B) μ of the NMOS (blue squares) and PMOS (red circles) as a function of the stress pulse amplitude, at the end of the stress.

To analyze the circuit/device degradations time dependences, since the device degradation cannot be measured during the pulsed stress, the circuit/device characteristics measured during the interrupted stress have been considered, for the case of 2.6V pulsed stress. The results are shown in Figure 7. As described elsewhere [6], larger relative degradations are observed for the NMOS (black squares) than for the PMOS (red circles), being the transistors mobility the most damaged parameter (figures 7 A and B). In addition,

the degradation of both parameters (for the two transistors) follows a power law with the stress time. Regarding the CMOS inverter, I_{DD} is largely reduced (~30% after 1 hour) while V_{INV} suffers a shift of ~5% (figures 7 D and C, respectively). At the end of the stress, the I_{DD} reduction (~30%) is very close to the μ degradation suffered by the NMOS transistor (~35%), while the V_{INV} shift (~5%) can be related to the larger V_{TH} degradation of the NMOS (~6%) compared with that of the PMOS (~1%). Note that the relative variations of the inverter performance seem to be mainly given by the NMOS degradation as observed in the results presented in figures 5 and 6.

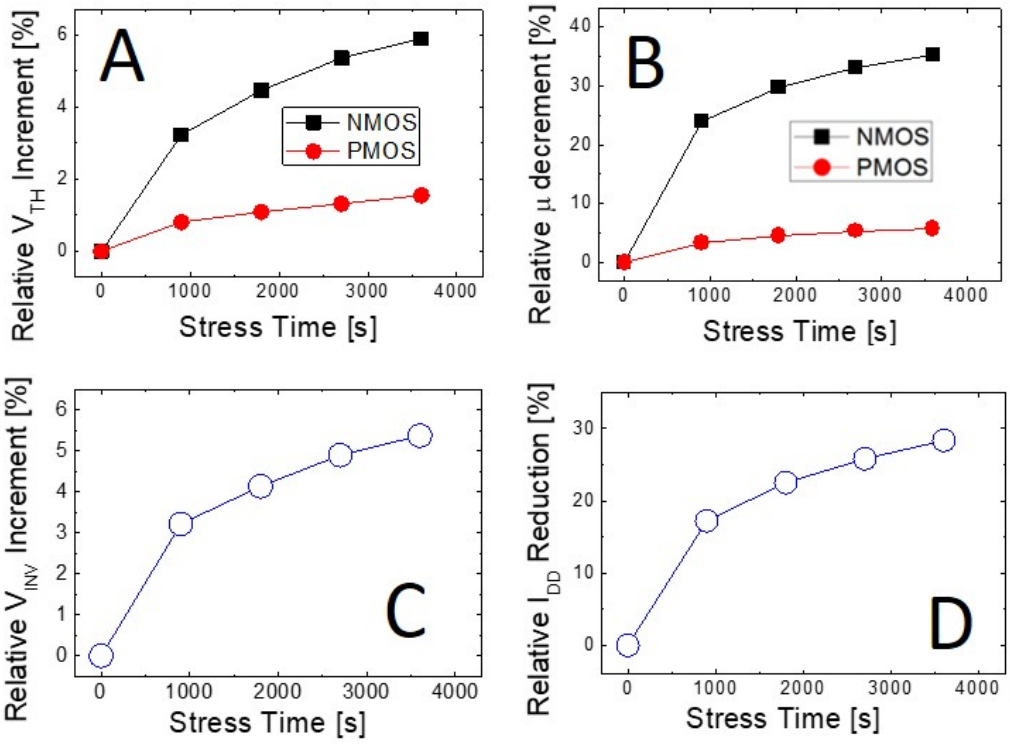

Figure 7: For the case of 2.6V pulsed stress (A) V_{TH} and (B) μ relative variations of the NMOS (black squares) and PMOS (red circles). (C) Relative shift of V_{INV} of the CMOS inverter and (D) relative reduction of I_{DD} at the inversion point.

IV. INVERSION VOLTAGE MODELLING

The V_{INV} shifts experimentally observed figures 5 and 7C have been analytically described by taking into account the device degradation (measured using the V_{TH} and μ shifts) in the equations that describe the inverter performance. A simple circuit analysis leads to equations 2 and 3, for the voltages at the device terminals at the inversion point, where V_{INV} is measured. For this point, $V_{GSN} = V_{IN} = V_{DSN} = V_{OUT} = V_{INV}$.

$$V_{DD} = |V_{DS_P}| + V_{DS_N} \rightarrow \quad |V_{DS_P}| = V_{DD} - V_{OUT}$$
$$V_{DD} = |V_{GS_P}| + V_{GS_N} \rightarrow \quad |V_{GS_P}| = V_{DD} - V_{IN} \qquad \text{(Eq. 2 and 3)}$$

Therefore, the saturation current at the inversion point for both transistors is given by equations 4 and 5:

$$I_{DD_P} = \frac{\mu_P W_P C_{OX}}{2L_P}\left(V_{INV} - V_{DD} - V_{TH_P}\right)^{\alpha}$$

$$I_{DD_N} = \frac{\mu_N W_N C_{OX}}{2L_N}\left(V_{INV} - V_{TH_N}\right)^{\alpha} \qquad \text{(Eq. 4 and 5)}$$

Where $\alpha = 2$ in these experiments.

Considering that $I_{DDN} = I_{DDP}$ and that (in the case of the samples used) device dimensions are equal, V_{INV} is described by equation 6:

$$V_{INV} = \frac{K_P^{1/\alpha}\cdot\left(V_{DD}+V_{TH_P}\right)+K_N^{1/\alpha}\cdot\left(V_{TH_N}\right)}{K_P^{1/\alpha}+K_N^{1/\alpha}} \qquad \text{(Eq. 6)}$$

Equation 6 analytically provides the inversion voltage as a function of the V_{TH} and μ of the NMOS and PMOS transistors. In this particular case, author used $\alpha = 2$ to evaluate this model.

It can be demonstrated that the experimentally observed circuit degradation can be described by equation 6, when considering the parameters of the degraded transistors. To do so, the relative variation of V_{INV} directly measured during the pulsed stress at V_{DD}=2.6V (blue line in figure 4-left) and that calculated using equation 6, using the V_{TH} and μ of the transistors measured during the stress interruption have been plotted together. First, the temporal evolution of the circuit/device degradations has been addressed, for the case of a 2.6V pulsed stress, in figure 8. As it can be seen, the equation prediction perfectly matches the measurements suggesting, that, for these pulsed tests, the temporal evolutions of the V_{INV} shifts only depend on the temporal evolutions of the shifts of V_{TH} and μ of the individual transistors.

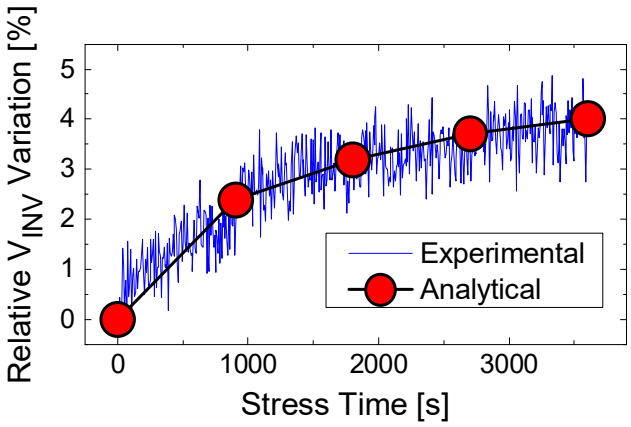

Figure 8: Relative V_{INV} variation measured during the pulsed stress with V_{DD} = 2.6V (blue) and obtained by the eq. 6 (dots), considering the V_{TH} and μ parameters of the two degraded transistors measured with the SPA.

The experimental and equation 6-predicted circuit degradations as a function of the pulse amplitude are shown in Figure 9. The relative V_{INV} variation at the end of the stress measured with 'On-the-fly' method (blue triangle), measured with the SPA (black squares), and the obtained V_{INV} variation with equation 6 (with the degraded transistor parameters obtained experimentally) are represented together. Note that, (i) there is not a remarkable difference on the results for the two measurement techniques and (ii) the analytical model matches the experimental results in the analyzed voltage range. Therefore, Figure 9 demonstrates that the inversion voltage (V_{INV}) can be measured accurately, with similar precision than that provided by the SPA, using the DSO, when a pulsed stress is applied at the input of the inverter, and predicted with the analytical model and the transistor parameters shifts.

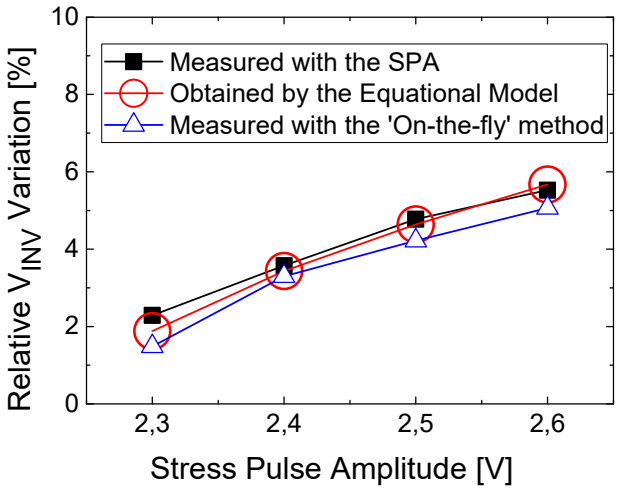

Figure 9: Relative V_{INV} variation measured with the SPA at the end of the stress (black squares) and with the 'On-the-fly' method (blue triangle) and the one obtained using the analytical equation (red circles).

V. CONCLUSIONS

An 'on-the-fly' type technique for the simultaneously monitoring of the inversion voltage shifts in CMOS inverters under pulsed stresses is proposed. 'On-the-fly' results have been validated by measuring those shifts with a semiconductor parameter analyzer at the end of the test. A power law equation that accounts simultaneously for the stress time and voltage dependences is capable to fit the experimental data. This law can be used to extrapolate the V_{INV} degradation to other operation conditions (time and voltage).

The relation between the circuit and device degradations has been analyzed in detail. Device level results show that, in this technology, the observed circuit performance shift is mostly related to the degradation suffered by the NMOS transistor when applying a pulsed stress: the V_{INV} increment is dominated by the V_{TH} degradation, while the driving current decrease is mainly related to the mobility reduction. Finally, simple circuit analysis has allowed to analytically describe the observed V_{INV} shifts, by only considering two MOSFET parameters shifts, i.e., V_{TH} and μ, of the PMOS and NMOS transistors. Although the direct measurement of transistor parameters (i.e., V_{TH} and μ) is not possible with the proposed pulsed tests, this type of technique allows the simultaneous stress and characterization of the performance degradation of an inverter, under stress conditions closer to their actual operation.

ACKNOWLEDGMENT

This work was supported by the PID2019-103869RB-C3 and TEC2016-75151-C3-R Projects, funded by the Spanish AEI and ERDF.

REFERENCES

[1] B. Kaczer, J. Franco, P. Weckx, Ph. J. Roussel, E. Bury, M. Cho, R. Degraeve, D. Linten, , H. Kukner, P. Raghavan, F. Catthoor, G. Rzepa, W. Goes, and T. Grasser, "The defect-centric perspective of device and circuit reliability — From individual defects to circuits," *45th European Solid State Device Research Conference (ESSDERC)*, pp. 218-225, Graz, Austria, 2015.

[2] M. Denais, C. Parthasarathy, G. Ribes, Y. Rey-Tauriac, N. Revil, A. Bravaix, V. Huard and F. Perrier, "On-the-fly characterization of NBTI in ultra-thin gate oxide PMOSFET's," *IEEE International Electron Device Meeting (IEDM)*, pp. 109-112, San Francisco, CA, USA,2004.

[3] H. Reisinger, U. Brunner, W. Heinrigs, W. Gustin, C. Schlunder, "A Comparison of Fast Methods for Measuring NBTI Degradation," *IEEE Transactions on Device and Materials Reliability*, pp. 531-539, 2007.

[4] A. Chenouf, B. Djezzar, A. Benabedelmoumene, H. Tahi, "Does PMOS Vth shift wholly capture the degradation of CMOS inverter circuit under DC NBTI?," *IEEE International Integrated Reliability Workshop (IIRW),* pp. 191-194, South Lake Tahoe, CA, USA, 2012.

[5] I. Messaris, S. K. Goudos, S. Nikolaidis, C: A. Dimitriadis, " A software Tool for Aging Analysis of the CMOS Inverter based on Hot Carrier Degradation modeling," 5th International Conference on Modern Circuits and Systems Technologies (MOCAST), 2016.

[6] E. Bury, et al., "Recent insights in CMOS reliability characterization by the use of degradation maps", IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), 2018.

[7] A. Chenouf, B. Djezzar, A. Benadelmoumene, and H. Tahi, "Deep investigation of NBTI Impact on CMOS Inverter Reliability" *International Conference on Microelectronics (ICM)*, 2012.

[8] A: Kerber, P. Srinivasan, S. Cimino, P. Paliwoda, S. Chandrashekhar, Z. Chbili, S. Uppal, R. Ranjan, M. I. Mahmud, D. Signh, P. P. Manik, J. Johnson, F. Guarin, T Nigam, B. Parameshwaran, " Device reliability metric for end-of-life performance optimization based on circuit level assessment," IEEE International Reliability Physics Symposium (IRPS), pp. 2D-3.1 – 2D-3.5, 2017.

[9] E. Barajas, D. Mateo, X. Aragones, A. Crespo-Yepes, J. Martin-Martinez, R. Rodriguez, and M. Nafria, "Design of a Broadband CMOS RF Power Amplifier to establish device-circuit aging correlations," *International Conference of Microelectronic Test Structures (ICMTS)*, pp. 1-3, Grenoble, France, 2017.

[10] X. Aragones, D. Mateo, E. Barajas, A. Crespo-Yepes, R. Rodriguez, J. Martin-Martinez, and M. Nafria, "Aging in CMOS RF linear power amplifiers: experimental comparison and

modeling," *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1-5, Sapporo, Japan, 2019.

[11] X. Aragonés, E. Barajas, A. Crespo-Yepes, D. Mateo, R. Rodriguez, J. Martin-Martinez, M. Nafria, "Aging in CMOS RF Linear Power Amplifiers: An Experimental Study", *IEEE Transactions on Miocrowave Theory and Techniques*, 2021.

[12] J. Maertin-Martinez, B. Kaczer, M. Toledano-Luque, R. Rodriguez, M. Nafria, X. Aymerich, and G. Groeseneken, "Probabilistic defect occupancy model for NBTI", *IEEE International Reliability Physics Symposium,* 2011.