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ABSTRACT

A low p–n built-in potential (1.75 V) makes 3C-SiC an attractive choice for medium voltage bipolar or charge balanced devices. Until recently, most 3C-SiC had been grown on Si, and power device fabrication had, therefore, been hindered by issues, such as high defect density and limited processing temperature, while devices were necessarily limited to lateral structures. In this work, we present the fabrication and characterization of a vertical PiN diode using bulk 3C-SiC material. A p-type ohmic contact was obtained on Al implanted regions with a specific contact resistance $\sim 10^{-3}\ \Omega\ \mathrm{cm}^2$. The fabricated PiN diode has a low forward voltage drop of 2.7 V at 1000 A/cm^2, and the on–off ratio at ±3 V is as high as 10^9. An ideality factor of 1.83–1.99 was achieved, and a blocking voltage of ∼110 V was observed using a single-zone junction termination design.

Wide bandgap (WBG) semiconductors are considered substrates for the next generation electronics, targeting high power and harsh environments that conventional Si devices struggle to meet. 4H-SiC is currently the most mature wide bandgap technology, available with a range of commercial unipolar diodes and transistors up to 1700 V. On the other hand, not as much work has been carried out on bipolar devices in SiC,[1,2] Ga_2O_3,[3] and diamond.[4,5] WBG bipolar power devices are far less developed compared with their unipolar counterparts, mainly due to the issues related to deep level acceptor activation, high p–n junction potentials, and low minority carrier lifetime. Due to its narrower bandgap $E_{g\_3C\text{-}SiC}$ of 2.3 eV (at 300 K),[6] 3C-SiC has a lower p–n junction built-in potential (∼1.75 V) than 4H-SiC (∼3 V). It is shown in Ref. 7 that 3C-SiC PiN diodes rated up to 4.5 kV have a forward voltage drop at 250 A/cm^2 lower than 4H-SiC. Until recently, however, the need to use 3C-SiC grown on Si substrates has made power device fabrication difficult. This is due to the high defect density within these 3C-SiC epilayers,[8,9] and also due to the need to employ lateral architectures, in order to avoid the 3C-SiC/Si heterojunction. Low voltage lateral p–n junction diodes were previously demonstrated by forming implanted regions in 3C-SiC epilayers grown on Si substrates.[10,11] Furthermore, while there were several reports achieving p-type conduction in Al doped 3C-SiC epilayers,[12–14] it remains an obstacle for implanted layers, which is often required in edge termination and Junction Barrier Schottky designs. This is mainly due to the post-implantation anneal temperature, which is limited to the 1414 °C (melting point of Si), thus not sufficient to activate the deep level Al dopants. In Ref. 15, p-type conduction was realized after Al was implanted (200 keV, $8 \times 10^{14}\ \mathrm{cm}^{-2}$, peak doping $\sim 5 \times 10^{19}\ \mathrm{cm}^{-3}$) into 3C-SiC at high temperature (850 °C) followed by a 1400 °C post-implant anneal, although the activation rate was estimated to be as low as 1%. With lower temperature Al implantation (500 °C; 180/110/60/30 keV, $11.2/7/5/2.7 \times 10^{14}\ \mathrm{cm}^{-2}$, peak doping $\sim 1 \times 10^{20}\ \mathrm{cm}^{-3}$) and anneal (1300 °C), it was shown that in Al implanted 3C-SiC layers, p-type conduction could only be achieved after a very long anneal (>317 h).[16] Studies on 3C-SiC growth methods in recent years led to a continuous reduction of defect density, and free-standing 3C-SiC wafers were demonstrated.[17–21] By removing the Si substrates (polish, etch, melt, etc.), the leftover 3C-SiC wafer not only keeps the large area

desired for lowering device costs, but also a higher processing temperature can be achieved. In addition, without the heterojunction, a vertical structure becomes possible, making the most of 3C-SiC in power device applications. In this work, by fabricating edge terminated, vertical power PiN diodes on bulk 3C-SiC wafers, both p-type conduction and high voltage (>100 V) p–n junction blocking is demonstrated.

To obtain the bulk 3C-SiC material used in this work, first, 150 μm intentionally nitrogen doped (1×10^{18} cm^{-3}) n-type 3C-SiC was grown on Si(100) substrates via Chemical Vapor Deposition (CVD). Next, the chamber temperature was increased to 1750 °C to melt and remove the Si(100) substrate. Another 10 μm thick non-intentionally doped ($\sim 2.5 \times 10^{16}$ cm^{-3}) n-type 3C-SiC epilayer was then grown on the highly doped 3C-SiC substrate. More detailed information about the bulk 3C-SiC growth can be found in Refs. 21 and 22. TEM analysis suggested that the resulting stacking fault density of these homoepitaxial grown 3C-SiC layers is below 10^3 cm^{-1},[22] which is among the lowest values obtained using various techniques, including standard Si substrate, inverted silicon pyramids substrate, and lower temperature (1400 °C) homoepitaxy growth.[18] Polishing of the as-grown 3C-SiC surface was challenging due to the stress and bowing within the wafer[23,24] and, thus, was not carried out. By performing a tapping mode AFM scan in several 10×10 μm^2 areas, rms surface roughness around 10 nm was observed.

The PiN diode fabrication began with two box-profile Al implantations, both performed at 600 °C. First a 350 nm deep, highly doped (1×10^{20} cm^{-3}) p$^+$ anode region (180/100/40 keV, $20/10/5 \times 10^{14}$ cm^{-2}) was formed. Second, a 600 nm deep, p-doped (2×10^{17} cm^{-3}) Single-Zone Junction Termination Extension (SZ-JTE) region (500/350/250/150/80 keV, $4.4/2.2/2.2/1.9/1.3 \times 10^{12}$ cm^{-2}) was formed. Post-implantation anneals were performed at 1700 °C for 2 h in Ar, with the sample surface covered by a carbon cap, which was then removed by oxidation in dry O_2 at 850 °C for 30 min. Following that, the samples went through standard RCA 1 and 2 cleaning procedures and were thermally oxidized in dry O_2 at 1300 °C to form a thin SiO_2 layer (≈75 nm), which passivates the surface dangling bonds and isolates the devices. With the top surface protected by a layer of baked photoresist, the back side SiO_2 was removed by wet etch (HF), after which, a Ti/Ni (30/100 nm) bilayer was evaporated onto the n$^+$ substrate and annealed at 1000 °C for 1 min in Ar to form the cathode.[25] Via photolithography, the surface passivation SiO_2 was selectively wet etched in diluted HF, and circular Ti/Al/Ni (30/100/50 nm) metal stacks with 40 μm diameter were then evaporated and lifted-off as the anodes.[12] To form ohmic contact, the anodes went through a rapid thermal anneal at 1100 °C for 2 min in Ar. A cross-sectional view of the final device with a circular structure is shown in Fig. 1.

Transmission Line Method (TLM) structures were fabricated in the p$^+$ implanted regions, and their room temperature I–V characteristics are shown in Fig. 2. Ohmic behavior is observed, and the lowest specific contact resistance is $\sim 9.7 \times 10^{-4}$ Ω cm^2. Not only is this among the lowest values recently reported for p-type 3C-SiC,[12,16] but also the post-implant anneal time is significantly reduced from >300 h to a more practical 2 h. However, the extracted specific contact resistance (10^{-4}–10^{-2} Ω cm^2) and sheet resistance (2500–15000 Ω/sq) values have a large distribution. This is most likely due to the rough surface previously mentioned and can be improved by optimizing the growing conditions and polishing methods.

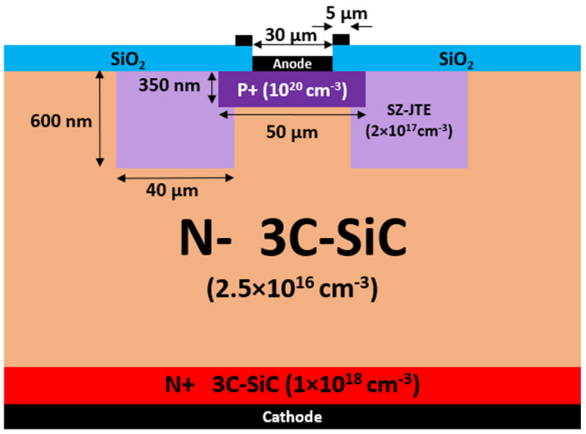

FIG. 1. Schematic cross section view of the fabricated free-standing 3C-SiC PiN diode with Single Zone Junction Termination Extensions (SZ-JTEs).

Typical room temperature forward J–V characteristics of the PiN diodes are shown in Fig. 3(a), and the built-in potential can be extracted from the intersection of forward current linear region fitting and the x-axis, which is just above 2 V, slightly higher than the theoretical value 1.75 V, but still 33% lower than the 3 V of typical 4H-SiC PiN diodes.[1,2,26] The current density goes above 1000 A/cm^2 at 2.7 V forward bias and hits the measurement compliance (5000 A/cm^2) at ~4.5 V. Device self-heating is inevitable at such a high current density. At elevated temperatures, SiC carrier lifetime was found to increase exponentially, while the carrier mobility and diffusion coefficients decrease.[27] It was shown in Ref. 28 that significant degradation occurred to 4H-SiC PiN diodes above 1700 A/cm^2, and a 9000 A/cm^2, 8-ms pulse can heat the device to 2000–2300 K. Carrier transportation in SiC in extreme conditions, such as in this work, is not yet well understood and needs further investigations. The differential specific on-resistance is estimated to be ~0.5 mΩ cm^2, and the on–off ratio at ±3 V is greater than 10^9 as shown in Fig. 3(b).

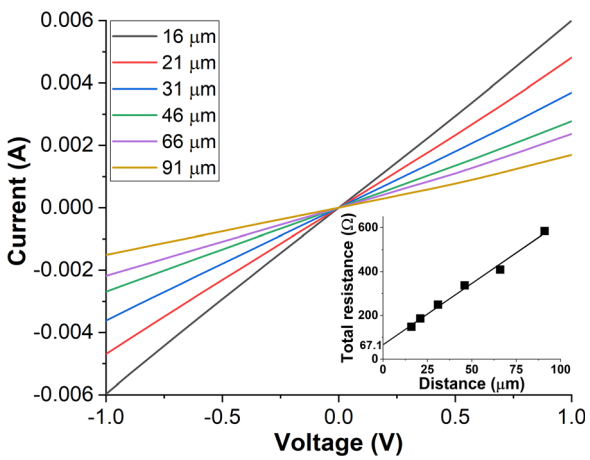

FIG. 2. Room temperature I–V characterization of the p-type ohmic contact TLM and fitting of the total resistance.

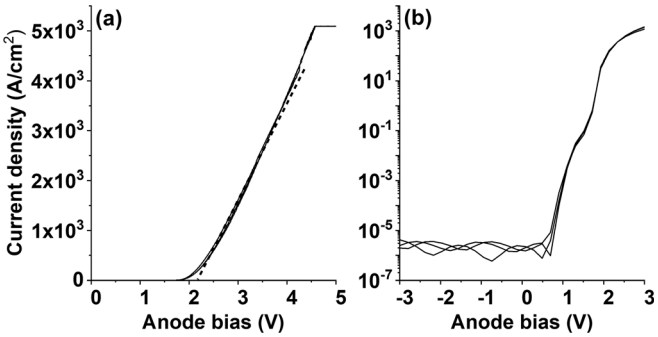

FIG. 3. Typical (a) 0–5 V forward J–V characteristics and (b) ±3 V on–off performance of PiN diodes at room temperature.

The built-in potential can be estimated from the second knee in the semi logarithmic graph [Fig. 4(a)], where the series resistance begins to dominate the forward conduction. A double-bump feature is consistently observed in the forward semi-log scale J–V curve [Fig. 4(a)]. This is usually due to an inhomogeneous interface,[29,30] which causes multiple current paths with different barrier heights, affecting the conduction mechanism. The diode ideality factor n can be extracted from the high-level injection region, and the typical values are 1.83–1.99, indicating the current transport is dominated by recombination. This latest result shows great improvements from literature, where either too large ($n > 3$[31,32]) or too small values ($n \approx 1.5$[11]) were observed. In the low-level injection region, ideality factors >2 were obtained this is most likely due to defect induced carrier recombination.[33]

At high reverse bias, the diodes suffer from a high leakage current density J_r, reaching 0.1 mA/cm^2 at −10 V as seen in Fig. 4(b). J_r does not follow a square root dependence (space-charge generation dominant) on the reverse bias. Instead, $J_r \propto V^{\alpha}$, where $\alpha \approx 6.7$ from 0 to −50 V. The fast increasing leakage is most likely due to defect assisted tunneling. It is known that stacking faults are the main cause of the high leakage in 3C-SiC devices,[34,35] and in order to achieve a low J_r of ∼0.1 mA/cm^2 at −600 V, stacking fault density needs to be kept below 700 cm^{-1}.[9] Also, the fact, J_r is above 0.1 mA/cm^2 at −10 V, means that self-heating cannot be neglected here, which can raise the leakage current level further.[36] Increasing the reverse bias further, the α value drops to ∼4.1. A maximum blocking voltage of ∼110 V was achieved [Fig. 4(b)]. Assuming a critical field for 3C-SiC of 1.4 MV/cm,[37] the theoretical 1D breakdown of the device is 210 V, occurring at a depletion region depth 3 μm from the surface. These devices, therefore, achieve ∼50% of the 1D theoretical value for this drift layer, further demonstrating the scope for improvement in the surface quality and termination.

At elevated temperatures (300–500 K), the forward current density increases, and the built-in potential decreases as shown in Fig. 5(a), which is due to the increasing number of intrinsic carriers. As can be seen from the linear plot inset [Fig. 5(a)], at relatively low current density (<60 A/cm^2), the forward J–V curves are parallel to each other, indicating a temperature independent differential resistance. Similar behavior was previously observed for 4H-SiC PiN diodes,[36] the result of compensation between an increase in carrier lifetime and a decrease in mobility and the diffusion coefficients. The low voltage (0 to −2 V) leakage current density increases significantly with increasing measurement temperature, from $\sim 1 \times 10^{-7}$ A/cm^2 at 25 °C to $\sim 1 \times 10^{-4}$ A/cm^2 at 225 °C. Despite the leakage being dominated by defect assisted tunneling, the thermally generated component, the saturation current density, J_0, can be extracted from the high-level injection region [Fig. 5(a)], and the Arrhenius plot is shown in Fig. 5(b). The activation energy for the thermally generated leakage component is estimated to be ∼0.88 eV, still lower than $E_{g\_3C\text{-}SiC}/2 \approx 1.15$ eV, in which case it is considered that carrier transportation is dominated by recombination. This is likely due to a tunneling contribution to the carrier transportation, which still cannot be neglected, even in the high-level injection (∼100 A/cm^2) regime, thus leading to a lower activation energy than expected.

A figure of merit (FoM) graph of Si, 3C-SiC, and 4H-SiC for power device applications is shown in Fig. 6 with some literature data of 3C-SiC unipolar devices.[14,38,40] due to lack of bipolar device results. As can be seen, the PiN diode fabricated in this work currently betters both the Si unipolar and super-junction limits. Also, improvement over the 3C-SiC MOSFETs and Schottky Barrier Diode can be inferred, because as the voltage rating is scaled up, the rise in on-resistance of these bipolar devices will be less than the unipolar devices. Furthermore, simple improvements can be made to these bulk 3C-SiC vertical PiN diodes to further improve this picture. Reducing the drift layer thickness to the maximum reverse depletion width (∼3 μm in this case) would have substantially lowered the on-resistance. Furthermore, lowering the drift layer doping

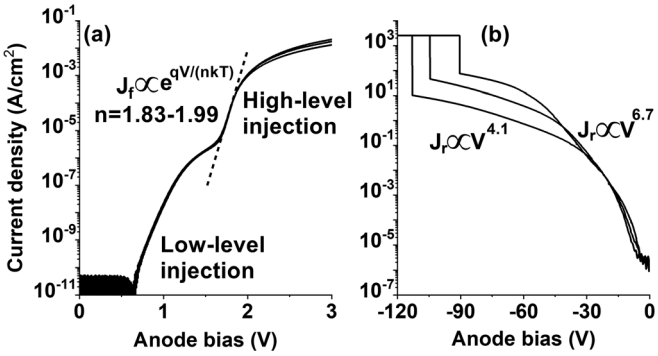

FIG. 4. Typical semi-log scale J–V characteristics of (a) forward and (b) reverse biased PiN diodes at room temperature.

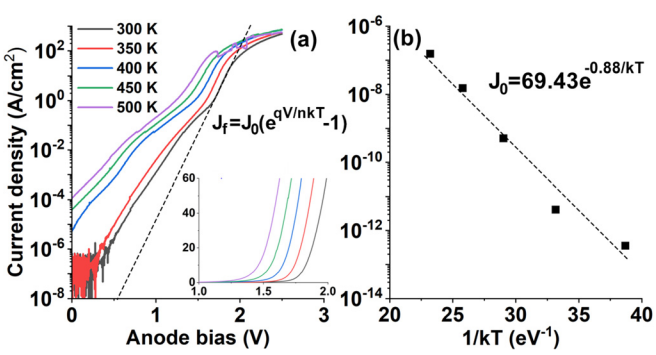

FIG. 5. PiN diode (a) log scale forward J–V characteristics at 300–500 K and (b) the saturation current density J_0 Arrhenius plot.

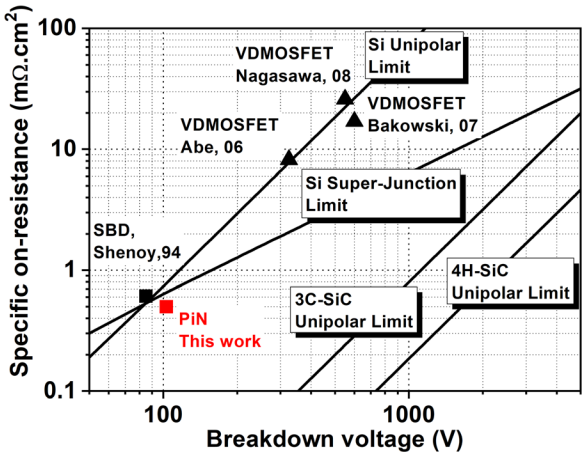

FIG. 6. Power device figure of merit graph for Si, 3C-SiC, and 4H-SiC, literature 3C-SiC devices parameters are provided.[14,37–39]

($<1 \times 10^{16}\,cm^{-3}$), smoothing the surface, and improving upon the junction termination process (use of P-Ring, or trench terminations) would all result in an increased breakdown voltage. However, there remains an evident gap between current 3C-SiC power device performance and the 3C-SiC unipolar limit, which needs will be narrowed in the near future via follow-up studies on defect density reduction and device processing.

Vertical PiN diodes have been fabricated using Al implantation into bulk 3C-SiC material. Removal of the Si substrate made possible post-implantation annealing at 1700 °C, making the development of a p-type ohmic contact more practically realizable. The diodes showed good on-state performance, with a reasonable ideality factor of 1.83–1.99. Despite a very high on–off ratio ($\sim 10^9$) at ±3 V, considerable defect assisted tunneling was observed at higher reverse bias. The thermally generated leakage component was found to be dominated by space charge generation, with an activation energy of ∼0.88 eV. Limited by the defect density and surface roughness, the maximum blocking voltage reached in this work is ∼110 V, but achieving 1000 A/cm^2 with a low forward voltage drop of 2.7 V demonstrates the potential of using 3C-SiC for PiN and Merged PiN Schottky power diodes applications.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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