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A walk on the frontier of energy electronics with power ultra-wide bandgap oxides and ultra-thin neuromorphic 2D materials

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ABSTRACT

Ultra-wide bandgap (UWBG) semiconductors and ultra-thin two-dimensional materials (2D) are at the very frontier of the electronics for energy management or *energy electronics*. A new generation of UWBG semiconductors will open new territories for higher power rated power electronics and deeper ultraviolet optoelectronics. Gallium oxide - Ga_2O_3 (4.5-4.9 eV), has recently emerged as a suitable platform for extending the limits which are set by conventional (~3 eV) WBG e.g. SiC and GaN and transparent conductive oxides (TCO) e.g. In_2O_3, ZnO, SnO_2. Besides, Ga_2O_3, the first efficient oxide semiconductor for energy electronics, is opening the door to many more semiconductor oxides (indeed, the largest family of UWBGs) to be investigated. Among these new power electronic materials, $ZnGa_2O_4$ (~5 eV) enables bipolar energy electronics, based on a spinel chemistry, for the first time. In the lower power rating end, power consumption also is also a main issue for modern computers and supercomputers. With the predicted end of the Moore's law, the memory wall and the heat wall, new electronics materials and new computing paradigms are required to balance the big data (information) and energy requirements, just as the human brain does. Atomically thin 2D-materials, and the rich associated material systems (e.g. graphene (metal), MoS_2 (semiconductor) and *h*-BN (insulator)), have also attracted a lot of attention recently for *beyond-silicon* neuromorphic computing with record ultra-low power consumption. Thus, energy nanoelectronics based on UWBG and 2D materials are simultaneously extending the current frontiers of electronics and addressing the issue of electricity consumption, a central theme in the actions against climate change.

Keywords: Energy electronics, ultra-wide bandgap, 2D-materials, power electronics, neuromorphic engineering, diodes, transistors, synaptors, memristors, memtransistors, neuristors, Ga_2O_3, $ZnGa_2O_4$, graphene, MoS_2, *h*-BN.

1. INTRODUCTION

Around a half of the energy of any kind of the world is electricity and this figure is expected to increase steadily in the near future [1]. The vast majority (if not all) of this electricity will flow through, at least, one power electronic device during its generation, transmission and final use. This is sometimes an overlooked critical aspect of the worldwide energy ecosystem, as power electronics makes renewable (and non-renewable) energy possible [2]. The introduction of solid-state switches and rectifiers made with other semiconductors more energy efficient than silicon will impact the overall power consumption, therefore reducing CO_2 emissions by a significant amount [3]. If, for example, the efficiency of electronic conversion can be increased by just ~2% "by replacing a single switch" (or, more accurately, the inefficient silicon embodiment), it may reduce global energy consumption by ~1%. Furthermore, devices made with a semiconductor having a bandgap larger than silicon can be made with less material and have less cooling requirements, hence saving a lot of space and weight in applications such as electrical transport. This integration obviously impacts the amount of energy required and, therefore, saves electrical power and/or fossil fuel (and associated emissions).

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Since the 1980s, there has been a lot of work towards replacing silicon-based (E-gap of 1.12 eV) power electronics devices with wide bandgap (3-3.4 eV) semiconductor (WBG) based devices (in particular, Silicon Carbide (SiC) and Gallium Nitride (GaN)) and power devices with superior specs (higher temperature of operation, higher power handling capability, etc.) are now commercially available (typically in the range of 650V-3.5kV) [4],[5] (Fig. 1). More recently, the frontier in the field is now given by ultra-wide bandgap semiconductors (UWBG), which have the promise of further upshifting the power rating and operation temperature. The same UWBG oxides also offer the potential for deeper ultraviolet optoelectronics [6]. Although another UWBG semiconductor, diamond, has been investigated over the last forty years, there has been limited progress and it is only recently been that other materials, such as Gallium Oxide (Ga_2O_3), Aluminum Nitride (AlN) or Boron Nitride (BN), have yielded device demonstrations with appropriate performances. Among these newer UWBG, Ga_2O_3 (4.5-5 eV) is receiving a lot of attention as a novel energy electronics semiconductor platform owing to its unusual material properties, large (*n* type tunable conductivity, extremely high breakdown field, unique optoelectronic properties, possibility of growing on large native substrates (more than 6-inch) and low cost [7]. Besides, representing the first viable oxide semiconductor for power electronics, Ga_2O_3 has opened the door to many more oxide compounds to be scrutinized (e.g. spinel $ZnGa_2O_4$) as they represent the largest family of ultra-wide semiconductors. We can anticipate, therefore, that a wide horizon of further discoveries is awaiting [8].

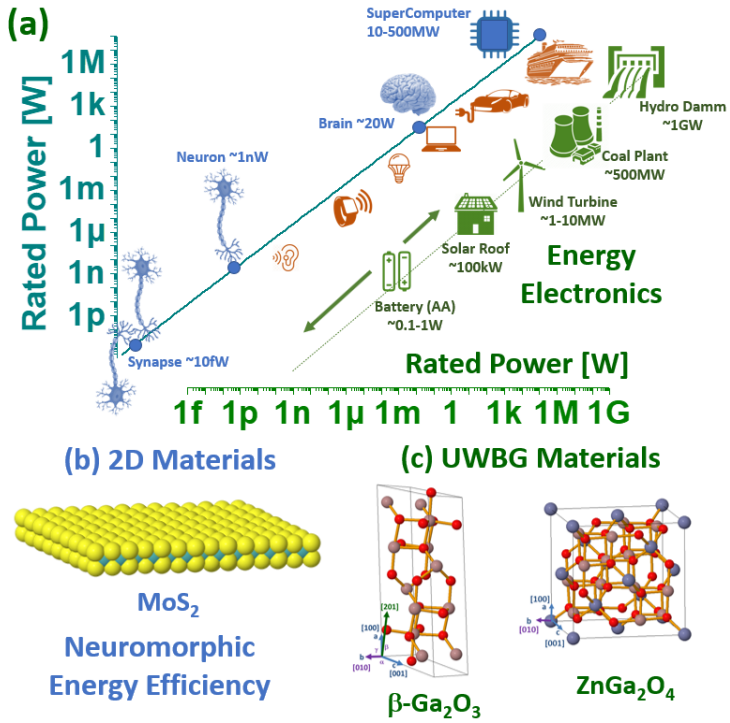

Figure 1. (a) Typical power ratings for various electronic devices and transportation systems (red) compared with the rated power of biological synapses, neurons and a human brain (20 W) along with supercomputers which (although only displaying a fraction of the human brain complexity) require some MW to function (blue). Depicted in green, the typical power delivered by some renewable and non-renewable sources. (b) *Low Power Energy Frontiers*. Neuromorphic engineering with 2D materials are predicted to provide as way to circumvent the memory wall energy consumption issues currently plaguing state-of-the-art computers. (c) *High Power Energy Frontiers*. UWBG semiconductors, and in particular, Ga_2O_3 (and related oxides, such as $ZnGa_2O_4$) are anticipated to handle power ratings way beyond those of current SiC and GaN based devices.

At the other power rating end, minute silicon, III-V and germanium based transistors (used in computer chips and memories), are reaching their limits. With the end of Moore's Law, due to the memory wall and the heat wall, new semiconductor materials and new computer paradigms are now required in order to balance our ever-growing need for data and the associated energy consumption. For example, around 18 megawatts (MW) of power is required to run the Tianhe-2 (33.9-petaflop, 3.12-million processor, 2013 world-beating Intel machine at China's National Supercomputer Center in Guangzhou), which is roughly the amount of energy required to power a small city of 15,000 inhabitants [9].

Even compared with this carbon power plant computer, for many computation tasks (e.g. image recognition), its' efficiency is dwarfed by the human brain. The most efficient and sophisticated computing machine is our brain, which is able to perform unpair achievements as simultaneous reasoning, learning, control, recognition and learning with a reduced power budget of just 20W (Fig. 1). Insights from neuroscience, thought yet mostly unexplored, attribute these impressive feats to the brain's intricate and vast inter-connectivity with a complex structural hierarchy and its time-and frequency-dependent neuronal coding [10]. The exchange of information through spikes or action potentials take place in between the basic computational units (neurons) while synapses are the interconnection memory elements that learn through these intricate codes at a minimum metabolic cost. Therefore, lower energy CMOS alternatives, that mimic biological brains neural networks (i.e., neuromorphic), are being explored based on non von-Neumann approaches [11],[12]. However, since neuromorphic CMOS chips still suffer from energy inefficient synaptic behavior, significant effort has been devoted to non-volatile memory as a foundation for neuromorphic computing: in particular, resistive random-access memory (RRAM) made primarily with WBG oxides such as TiO_x, HfO_x, TaO_x etc [13]. At the time being, most conventional memristors based on bulk materials are generally based on traditional top-down approaches and their thickness is limited to few nanometers before they become fully conducting. They also show limited tunability and control owing to the critical dependence of the device performance on the local (atomic-scale) topology of defects, filaments etc. In contrast, emerging two dimensional materials exhibit inherent control over the atomic stoichiometry and defect structure displaying unprecedented ultra-low power synaptic behaviors [14],[15].

In summary, power consumption reduction, energy efficiency and a more rational use of energy are central themes for the mitigation of the effects of global warming and thus a problem which must be addressed during the XXI century. UWBG oxide semiconductors and 2D materials are now at the very frontier of energy electronics, and a lot of cutting-edge research, challenges and opportunities are taking place. These will be succinctly overviewed in this paper.

2. UWBG ENERGY ELECTRONICS

2.1 Gallium Oxide (Ga_2O_3) and Zinc Gallate ($ZnGa_2O_4$)

Gallium oxide (Ga_2O_3) is an UWBG oxide semiconductor for which the bandgap energy lies in the range of 4.5-4.9 eV [16]. From a power devices perspective, Ga_2O_3 transistors and rectifiers have the potential to deliver excellent performances in the form of high breakdown voltage, high power and low losses because of superior material properties (e.g. high breakdown field, high electron mobility, etc.). Indeed, one major material advantage of Ga_2O_3 is its large breakdown electric field (E_{BR}), which is usually assumed to be of the order of 8 MV/cm. However, very recently it was suggested that the critical electric field of Ga_2O_3 could be as large as 13.2 MV/cm (Fig. 2(a)), if the residual donors are efficiently removed [17]. A high E_{BR} significantly increases the suitability of a semiconductor material for power devices. Baliga's figure of merit [18] for power electronics is proportional to E_{BR}^3, whilst only being linearly proportional to the bulk electron mobility (μ). This is estimated to be in the order of 300 cm^2/Vs for single crystal β-Ga_2O_3. This suggests that the on-state losses can be an order of magnitude lower than those for SiC and GaN for a given breakdown voltage. A major technological advantage of the β-Ga_2O_3 is that the single crystal structure can be synthesized via several standard melt growth methods including the Czochralski (CZ) technique [19]-[23]. *n*-type doping technology is relatively well established and straightforward in Ga_2O_3. Si and Sn atoms are known to be shallow donors with small activation energies (60-80 meV), typically yielding electron densities in an acceptable power device drift region range of 10^{15} - 10^{19} cm^{-3} [24],[25]. As in many other oxides, *p*-type doping is more challenging but there have been marked advances over the last few years [26]-[28] (Fig. 2(b)). Another highly relevant advantage of Ga_2O_3 is its' high stability in contact with the atmosphere and with many other electronic materials enabling the definition of ultra-large Schottky barriers [29], 2D conductive surfaces in a topological (ultra-wide) insulator-like fashion [30] or solar cells with giant photo-voltages [31] (Fig. 2(c),(d)). On the optoelectronics front, Ga_2O_3 (and related materials) also stand-up well; at the time being, they are the transparent conducting oxide with the largest bandgap (>5 eV). There is also the possibility of engineering this bandgap upwards, through alloying with aluminium, and thus extending the optical transparency further into the ultraviolet [27]. There are, however, still some drawbacks for the adoption of Ga_2O_3 as the wide bandgap semiconductor platform of choice including the low value of the thermal conductivity of the gallium oxide, an issue that may be addressed by thinning and/or bonding the Ga_2O_3 active layer to more efficient heat sinks [32].

Very recently, a Ga_2O_3 related oxide, the *spinel* Zinc Gallate ($ZnGa_2O_4$) (ternary alloy of Ga_2O_3 and ZnO) is also being considered as an UWBG (~5 eV) oxide semiconductor. Spinel generally refers to compounds with formulation AB_2X_4 where A^{2+} is a divalent cation such as Zn, Ni, Cu, Sn, Mg, Cr, Mn, Fe, Co or Cd, B^{3+} is a trivalent cation such as Ga, Al, In, Ti, V, Fe, Co, Ni, V, Cr or Mn, and X^{2-} is a divalent anion such as O, S or Se [33]. There are over 1,000 compounds that are known to crystalize in the spinel structure, and the sub-family of spinel oxides is a large and important class of multi-functional oxide semiconductors with many energy optoelectronics applications in areas such batteries, fuel cells, catalysis, photonics (phosphors, bio-imaging, photodetectors), spintronics (magnets, bio-magnets) or thermoelectricity [34]. A potential advantage of spinel $ZnGa_2O_4$ is its' great dopability prospects owing to the spinel's inherent diversity in cation coordination possibilities. Normal spinels have all A cations in the tetrahedral site and all B cations in the octahedral site, e.g. Zn-tetrahedral site $Zn^{2+}(T_d)$ and Ga-octahedral site $Ga^{3+}(O_h)$ so that normal $ZnGa_2O_4$ is $Zn(^{2+}[T_d])Ga_2(^{3+}[O_h])O_4(^{2-})$. The spinel's off-stoichiometry, from the ideal 1:2:4 proportions, or the creation of cation antisite defects are known routes for doping these compounds. Dominant defects in spinels are antisite donors (e.g. Zn_{Ga}) or donor-like $Ga^{3+}(O_h)$-on-T_d and antisite acceptors (e.g. Ga_{Zn}) with acceptor-like $Zn^{2+}(T_d)$-on-O_h antisite defects [35]. Some very recent work, such as those of Hrong *et al.* [36] and Galazka *et al.* [37], have evidenced the great prospects of *n*-type $ZnGa_2O_4$ as an UWBG optosemiconductor platform and new routes to bipolar devices were also opened up by *p*-type ternaries such as $ZnGa_2O_4$ [8] to mitigate the acceptor issue in binary UWBGs owing to their multiple cation coordination possibilities.

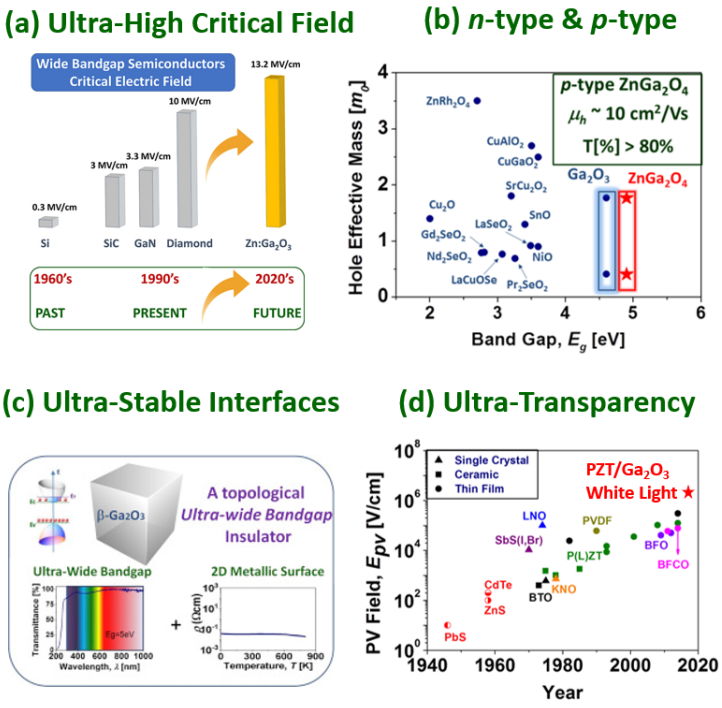

Figure 2. Ga_2O_3 and related oxides have been demonstrated to exhibit some remarkable features such as (a) ultra-high critical electric field, (b) potential bipolar operation due to its demonstrated *n*-type and *p*-type conductivity, (c) ultra-stable interfaces that may host a 2D electron gas, (d) Extended transparency into the UV-A region for transparent conducting oxide (TCO) applications (tail state density is located deeper in the ultraviolet than conventional TCOs). Panel (a) adapted with permission from Chikoidze *et al.* [17] © 2020 Elsevier Ltd. All rights reserved. Panel (b) adapted with permission from Chikoidze *et al.* [8] Copyright © 2020, American Chemical Society. Panel (c) adapted with permission from Chikoidze *et al.* [30] © 2018 Elsevier Ltd. All rights reserved. Panel (d) adapted with permission from Perez-Tomas *et al.* [218] © 2016 WILEY-VCH Verlag GmbH & Co. KGaA.

Since the seminal work of Higashiwaki *et al.* [38] demonstrating a power MESFET in a Ga_2O_3 single crystal in 2012, the power diode and transistor technology has advanced at a very fast pace [39]-[46], as highlighted in the next sections.

2.2 Gallium Oxide Power Diodes

In the past few years, impressive specs have been achieved for β-Ga_2O_3 power Schottky barrier diodes (SBDs) (Fig. 3(a)). reaching blocking voltages over 3kV [47],[48]. The general design rule for these devices is to achieve the highest breakdown voltages (V_{br}) (for a given epitaxial thickness) while keeping the (specific) on-resistance as low as possible (R_{on}) [mΩcm^2] so that the (Baliga's) high-power figure-of-merit (FOM) [usually given in GW/m^2] can be maximized ($V_{br}^2/R_{on}A$). Or in other words, a rectifying WBG device is better when thinner epitaxial WBG layers are employed so as to sustain a given blocking voltage. To this end, device terminations are very important. Field plates (FP), implanted edge termination (ET), implanted guard ring FPs, thermally oxidized termination, beveled mesas, and trench structures, have been incorporated in order to reduce the electric field crowding at the diode edges. In the literature, the usual choice for the cathode back contact is Ti/Au which is annealed at high temperature in order to achieve Ohmic behavior, while a common anode metal stack is Ni/Au, which typically delivers a Schottky barrier height of ~1eV. While delivering low contact resistance, it is worth mentioning that Au is not considered a CMOS-compatible metal. This is an issue shared with GaN-based technology [49]. Very recently, an ultra-large Schottky barrier of ~1.8 eV has been extracted for all-oxide $PdCoO_2/\beta$-Ga_2O_3 Schottky diodes [29]. The polar layered structure of $PdCoO_2$ generates electric dipoles, realizing a large Schottky barrier height of ~1.8 eV (well beyond the 0.7 eV expected from the basal Schottky-Mott relation) along with a large on/off ratio approaching 10^8, even at a high temperature of 350°C (Fig. 3(c)). As there are a number of polar oxides, this is a promising approach to increase the reverse blocking voltage of Ga_2O_3 diodes [50].

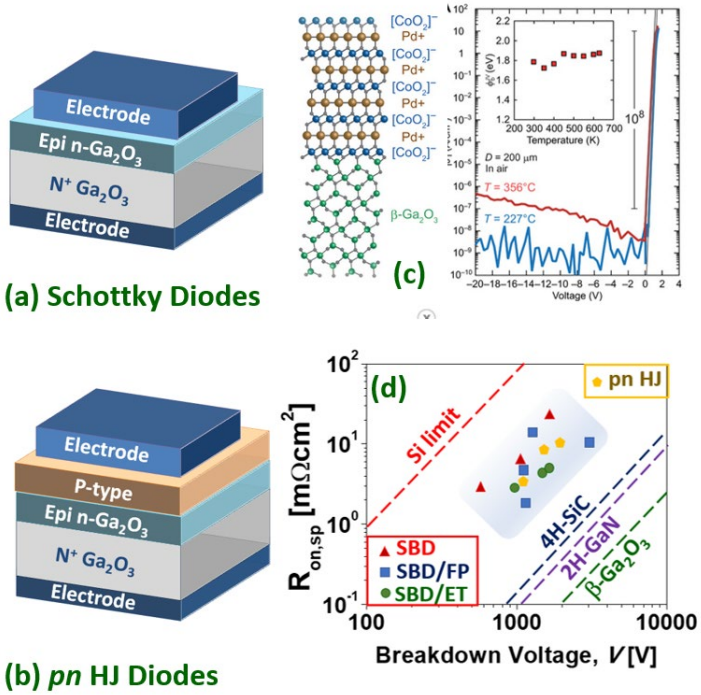

Figure 3. Schematics of (a) vertical Ga_2O_3 Schottky diodes and (b) *p-n* heterojunction diodes. (c) A $PdCoC_2/Ga_2O_3$ exhibiting the ultra-large Schottky barrier of 1.8 eV. (d) Baliga's FOM for selected Schottky and pn HJ diodes from the literature. Panel (c) adapted with permission from Harada *et al.* [29] © 2019 AAAS 4.0 (CC BY-NC).

SBD devices can be made with either a vertical architecture, using homoepitaxial Ga_2O_3 or with a lateral architecture using either homo- or heteroepitaxial (e.g. on sapphire) Ga_2O_3 . In general, the vertical structure is preferred as the device pitch is reduced and the encapsulation is simpler. Hu *et al.* [47] demonstrated a field-plated lateral β-Ga_2O_3 SBD on a sapphire substrate with a reverse blocking voltage of more than 3 kV, an R_{on} of 24.3 mΩcm^2 (anode–cathode spacing 24 μm) and a FOM > 0.37 GW/cm^2 (while a FOM of ~500 GW/cm^2 was achieved as the anode-cathode spacing (and V_{br}) was reduced). Zhou *et al.* [51] implemented a Mg implanted ET device on a vertical β-Ga_2O_3 SBD with a reverse

blocking voltage of 1.55 kV and a low specific on-resistance, of 5.1 mΩcm^2 (epi thickness 10 μm) and a FOM of 0.47 GW/cm^2. Analogously, Lin *et al.* [52] implemented a guard ring with or without a FP on vertical SBDs. The terminated devices exhibited a specific on-resistance of 4.7 mΩcm^2 and a V_{br} of 1.43 kV. Wang *et al.* [53] implemented a thermally oxidized termination on a vertical SBD with a V_{br} of 940 V, a specific on-resistance of 3.0 mΩcm^2 and a FOM of 0.295 GW/cm^2. Allen *et al.* [54] implemented a small-angle beveled field plate (SABFP), on thinned Ga_2O_3 substrates and a non-punch-through vertical SBD design rendering a V_{br} of 1100 V, a peak electric field of 3.5 MV/cm and a FOM of 0.6 GW/cm^2.

Somehow the state of the art is given by Li *et al.* [48]. They demonstrated a FP vertical Ga_2O_3 trench SBDs with a V_{br} of 2.89 kV (which is ~500 V higher than those without FPs). The trench SBDs exhibited a differential specific on-resistance of 10.5 (8.8) mΩcm^2 from DC (pulsed) measurements leading to a FOM of 0.80 (0.95) GW/cm^2. This Baliga's power FOM is approaching that for the best vertical SBD GaN devices (e.g. 1.7 GW/cm^2 [55]) but is still several times smaller than lateral AlGaN/GaN SBD (e.g. 3.6 GW/cm^2 [56]) and bipolar *p-n* vertical GaN diodes (e.g. ~4.6 GW/cm^2 [57]). Both, the 2D gas formed at the AlGaN/GaN interface and the bipolar injection are effective ways of further reducing the on-resistance in these devices while keeping the breakdown voltage high. The lack of low resistive *p*-type layer for the anode has, so far, prevented a competitive homojunction *p-n* Ga_2O_3 diode but, *p-n* heterojunction diodes have been realized by integrating *n*-type Ga_2O_3 with p-type semiconductors such as Cu_2O (1.49 kV) [58] and NiO (1.06 kV) [59], (1.86 kV) [60]; this last device yielding a Baliga's FOM of 0.33 GW/cm^2 (Fig. 3(c),(d)). Recently, extremely high-*k* dielectrics have been explored for electric field management in WBG semiconductor-based lateral and vertical device structures [31],[61]-[64]. According to the TCAD simulations of Roy *et al.* [65], a dielectric superjunction β-Ga_2O_3 SBD with practically achievable device dimensions with extremely high FOM should be possible; e.g. 20 kV can be achieved for an R_{on} of 10 mΩ-cm^2 with a dielectric constant of 300, a Ga_2O_3 width/dielectric width ratio of 0.2 and an aspect ratio (drift layer length (anode to cathode spacing) /drift layer width ratio) of 10 resulting in a PFOM of 40 GW/cm^2 (surpassing the theoretical unipolar FOM of β-Ga_2O_3 SBD by four times).

2.3 Gallium Oxide Power Transistors

A power MOSFET fabrication process generally includes a number of technological steps including gate dielectrics, surface passivation, drain/source ohmic contacts, implant doping, isolation and/or mesa etch. Due to the large bandgap of Ga_2O_3, the most suitable gate insulators are those with enough (conduction and valence) band-offsets to avoid current injection through the gate (e.g. SiO_2 and Al_2O_3; and perhaps other oxides such as Y_2O_3, MgO, Mg_2AlO_4) while balancing the dielectric constant to achieve more gate capacitance and more carriers in the conductive channel [66]. Defining a contact region by implantation, as in Si, SiC and GaN power MOSFET technologies, (typically n^+ Si-ion implantation doping for Ga_2O_3) is a usual choice [67] while other techniques have been suggested to further decrease the contact resistivity, such as the formation of surface states [68] or the adoption of a TCO as a metallic interface [69]. As in, the more mature, AlGaN/GaN HEMT technology, Ohmic contacts are typically made with a multilayer metal stack consisting of an adhesion layer (e.g Ti, Ta), an overlayer (Al), a barrier layer (e.g. Ni, Ti, Mo) and a capping of Au [70], [71]. Nevertheless, it has been argued that simpler metal structures such as Ti/Ga_2O_3 are also efficient if there is an oxygen deficient Ga_2O_3 surface [72] (a double charged oxygen vacancy is a well-known intrinsic donor in oxides [30]). Indeed, Yao *et al.* [73] suggested that the surface states appear to have a more dominant role in the transformation from a Schottky to an Ohmic interface than the choice of metal.

As with power SBDs, power MOSFETs can be defined in a vertical Ga_2O_3 homoepitaxial structure (typical of SiC power MOSFETs) and lateral structure (typical of AlGaN/GaN power HEMTs) which can be either homoepitaxial or heteroepitaxial (Fig. 4). Ga_2O_3 power MOSFETs are mostly unipolar *n*-type and operate in depletion mode (D-mode or normally-*on*) but a number of techniques have been reported to make enhancement mode (E-mode or normally-*off*) Ga_2O_3 devices. For example, Chabak *et al.* [74] reported an enhancement-mode β-Ga_2O_3 MOSFETs on a Si-doped homoepitaxial channel grown by molecular beam epitaxy using a gate recess process to partially remove the epitaxial channel under the 1-μm gated region so as to fully deplete at zero gate bias. With a breakdown voltage of 505 V (8 mm source-drain spacing), a maximum current density of 40 mA/mm and an on/off ratio of 10^9, Hu *et al.* [75] achieved (in 2018) a larger blocking voltage (1.075 kV), a larger threshold voltage (1.2-2.2 V) and a larger output current (~500 A/cm^2) in a first demonstration of vertical E-mode MOSFET with significatively larger FOM (~80 MW/cm^2). The E-mode was accomplished by doping profiling in a FinFET design (a type of 3D, non-planar transistor which has become the usual layout for the smallest CMOS 14 nm, 10 nm and 7 nm nodes). This kind of E-mode vertical power device was later optimized to sustain up to a blocking voltage of 1.6kV [76], a threshold voltage of 2.66 kV, a maximum current

density of 25.2 mWcm^2 and a record FOM of 280 MW/cm^2 [77]. Among D-mode devices, the ones reported by Lv et al. [77], [78] stand out for exhibiting a particularly large FOM. They reported (in 2019) [78] source-FP β-Ga_2O_3 MOSFETs on a Si-doped/Fe-doped semi-insulating β-Ga_2O_3 substrate exhibiting 222 mA/mm (18 mm source-drain spacing) with on-resistance of 11.7 mΩcm^2, a V_{br} of 680 V and a FOM of 50.4 MW/cm^2. Later (in 2020) [79], they adopted a T-shaped gate and source connected FP structure to increase the V_{br} up to 1.4 kV/2.9 kV (for 4.8 μm/17.8 μm source-drain spacing) and specific on-resistances of 7.08 mΩcm^2/46.2 mΩcm^2, yielding a record high FOM of 277 MW/cm^2 together with negligible gate or drain pulsed current collapse and a drain current on/off ratio of 10^9. Other lateral D-mode devices with high FOM were reported by Tetzner *et al.* [80]. By using sub-μm gate lengths (combined with gate recess) and optimization of compensation-doped high-quality crystals, implantation based inter-device isolation, and SiNx-passivation, breakdown voltages of 1.8 kV and a FOM of 155 MW/cm^2 were achieved. In 2020, Sharma *et al.* [81] reported Ga_2O_3 lateral D-mode field-plated MOSFETs exhibiting an ultra-high V_{br} of 8.03 kV (70 mm) by using polymer SU8 passivation. The current was rather low, however, due to plasma-induced damage of channel and access regions resulting in an impractical FOM of 7.73 kW/cm^2 (i.e. not above the silicon limit). As reported by Kalarickal *et al.* [64], ultra-high-*k* ferroelectric dielectrics, such as $BaTiO_3$, can, in principle, provide an efficient field management strategy by improving the uniformity of electric field profile in the gate-drain region of lateral FETs. High average breakdown fields of 1.5 MV/cm (918 V) and 4 MV/cm (201 V) were demonstrated for gate-drain spacings of 6 μm and 0.6 μm respectively in β-Ga_2O_3, at a high channel sheet charge density of 1.8×10^{13} cm^{-2}. An elevated sheet charge density together with a high breakdown field enabled a record power FOM of 376 MW/cm^2 at a gate-drain spacing of 3 μm (Fig. 4(c)). As in the case of SBDs, these performances for the Ga_2O_3 devices are already impressive and well beyond the silicon limit but still lag behind the best (much more mature) GaN devices in their respective power ratings [82],[83].

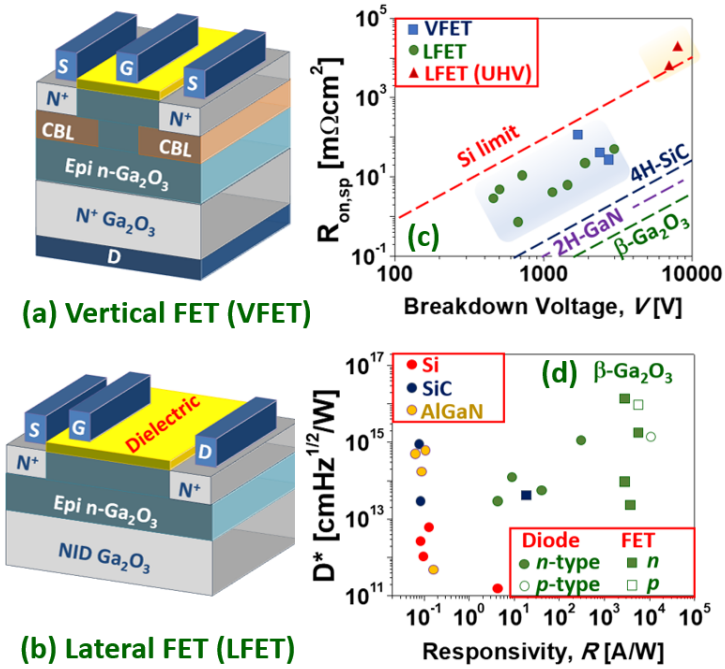

Figure 4. Schematics of (a) a vertical Ga_2O_3 power transistor (VFET) and (b) a lateral transistor (LFET). (c) Baliga's FOM for selected LFETs and VFETs from the literature. (d) Prospects of Ga_2O_3 devices as UV PDs, D* refers to specific detectivity; dots symbols referrer to diodes (either SBD or MSM) while square symbols denote transistors (data adapted from Wu *et al.* [29]).

All the above power MOSFET devices are unipolar *n*-type. These devices are sometimes referred as MISFETs so as to distinguish them from the conventional *p*-*n* junction based MOSFETs, since there are no *p*-regions in these MISFETs [76]. There are, however, several reports of *p*-type Ga_2O_3 in nominally undoped [26],[27], H-doped [84] and N-doped [28] β-Ga_2O_3. In particular, Wu *et al.* [28] proposed a growth mechanism of multistep structural phase transitions from hexagonal P63mc GaN to rhombohedral R$\underline{3}$c α-$GaN_xO_{3(1-x)/2}$ and finally to monolithic C2/m N-doped β-Ga_2O_3, which

improves the crystalline quality, facilitates acceptor doping, increases the acceptor activation efficiency, and thus enhances the *p*-type conductivity (acceptor ionization energy of 0.165 eV, Hall resistivity of 17.0 Ωcm, Hall hole mobility of 23.6 cm^2/Vs, hole concentration of 1.56×10^{16} cm^{-3}). P-type β-Ga_2O_3 films based lateral MOSFET deep-ultraviolet (DUV) PDs were fabricated with extremely high responsivity (5.1×10^3 A/W) and detectivity (1.0×10^{16} Jones) under 250 nm light illumination (40 $\mu W/cm^2$) conditions. Fig. 4(d) shows the responsivity and detectivity (D*) for state-of-the-art DUV PDs based on various WBG materials (adapted from [29]), in which it can be seen how β-Ga_2O_3 surpasses conventional Si, SiC and AlGaN based devices in terms of responsivity and detectivity.

3. 2D NEURAL AND NEUROMORPHIC ELECTRONICS

After the rediscovery, and meteoric rise, of graphene in 2004 [85], a large number of 2D materials, particularly transition metal dichalcogenides (TMDs) [86], have attracted a lot of interest. In contrast to the strong 3D ionic-covalent atomic bonding network in bulk materials (which is particularly strong in UWBG semiconductors), each layer in a 2D material is only covalently bonded in-plane with a dangling-bond-free surface, and a single layer or a few layers can be exfoliated from a bulk 2D crystal because of the weak van der Waals (vdW) force between adjacent layers. 2D materials are a diverse material system, including gapless *semimetals* (graphene), *semiconductors* (E-gap typically ranging from 1 to 2 eV) (e.g. MoS_2 E-gap 1,8 eV) and UWBG *insulators* such as hexagonal Boron Nitride (*h*-BN) [87]. The UWBG layered vdW hexagonal BN form (5.96 eV) corresponds to graphite while the cubic variety, (which has a sphalerite non 2D structure), c-BN (6.36 eV) is analogous to diamond and would be a very promising material for power electronics if it would be easier to growth [88]. TMDs are generally composed of transition metals (group IV to group VIII, e.g., Mo, W, Pt) and chalcogens (e.g., S, Se, Te), with over, approximately, 80 types experimentally developed so far. They exhibit a wide spectrum of conducting behaviors due to diverse elemental combinations, ranging from semi-metallic (e.g., $PdTe_2$, $PtTe_2$) to semiconducting (e.g., MoS_2, WSe_2) [89]. As in other semiconductor systems, such as III-Vs or perovskite oxides, new device concepts based on vdW heterostructures can be exploited through band engineering design, such as tunneling FETs [90], Gaussian transistors (GFET) [91],[92] or the Dirac-source FETs [93]. Its genuine atomically thin nature, makes 2D materials an alternative material of choice in the post-Moore era (or ultra-scaling era) when the limits established by the quantum confinement effect strongly challenges bulk channel materials for being reduced to features below ~5 nm [94].

3.1 2D Neuromorphic Computing Hardware

Seminal neuromorphic computing papers were published in the late 1980s [12] with the disruptive vision of mimicking biological neural networks, neurons and synapses with silicon transistors. These initial efforts, rapidly evolved to develop an event-driven computation based on trains of discrete voltage pulses or spikes and, later in this century, the apparition of the large-scale CMOS neuromorphic chips. The larger energy-efficiency is a salient feature of these chips and algorithm researchers are continuously engaged in enhancing the spike-driven computation learning and inference in spiking neural networks (SNNs) [10]. But this is not enough; as the requirement of larger information database management at a feasible computation and power cost is exponentially rising, it has become evident that new paradigms (architectures and/or materials) should be developed as those known as "*beyond von Neumann*" and "*beyond silicon*". In the architecture front, a promising *beyond von Neumann* approach as a way for mitigating the memory wall bottleneck, is to enable '*near-memory*' and '*in memory*' computing [95]-[97]. Near-memory computing is conceived to allow the co-location of memory and computing units in close proximity (thus reducing the associated power costs) while, in the extreme case, memory and computing will be located in the same place, as in the brain.

Regarding *beyond silicon*, non-volatile technologies [98]-[104] are usually compared to biological synapses. In fact, they exhibit two of the most important characteristics of biological synapses: synaptic efficacy and synaptic plasticity. Various works based on memristive technologies [99],[100] such as resistive random-access memory (RRAM) [101], phase-change memory (PCM) [102] and spin-transfer torque magnetic random-access memory (STT-MRAM) [103] have been explored for both matrix computations and synaptic learning based on spike-timing-dependent plasticity (STDP) rules. Initial attempts to realize neuromorphic functionality in 2D nanomaterials revealed unexpected mechanisms that subsequently spurred the development of new device concepts. For resistive switching, there are several expected advantages of 2D material neuromorphic channels over conventional materials (primarily WBG metal oxide memristors) including [14],[15],[104]:

(1) Low Energy

- *Low Energy*. The 2D materials atomic scale thickness is advantageous for faster switching, higher density, and lower energy consumption.
- *Below fJ*. Previous studies reported that the energy consumption for synaptic operation in 2D materials-based devices could be downscaled to femto Joule (fJ)-level per spike, thus being especially advantageous for neuromorphic applications [105].

(2) Layered nature

- *Enhanced Reliability*. 2D materials are expected to exhibit a more reliable operation compared with bulk metal oxides where it is difficult to control the charge carrier's pathway due to its stochastic switching nature.
- *Defect-mediated surfaces*. 2D materials exhibit defect-mediated surfaces (e.g., saturated dangling bonds at the basal plane) with minimal structural/chemical changes compared to conventional metal oxides, therefore enabling a high controllability of spatially defined conductive paths.
- *Higher linearity*. 2D materials-based synaptic devices often exhibit high linearity in the weight update that is superior to the conventional ones. This is attributed to their intrinsically anisotropic non-layered vdW structure which is unlike structurally isotropic materials.
- *Permeability*. Their planar structure with a high surface-to-volume ratio also allows for unique defect engineering schemes. Defect generation enables their application for cation-based resistive switching devices, which would otherwise be unfeasible due to their dense planar structures which are impermeable for ions/molecules [106].
- *Open Surface*. The open surfaces of 2D materials allow gate-tunability and multi-terminal synapses with heterosynaptic plasticity, providing pathways to the negative feedback loops that underlie non-Hebbian learning.
- *3D Topology.* Nanomaterials possess desirable form factors for 3D circuitry (3D integration through stacked 2D layers and vertical interconnects) with synaptic hyper-connectivity at the device level that present opportunities beyond the 3D addressable topology schemes that currently exist for two-terminal memristor crossbar arrays.

(3) Novel Aspects

- *Electrical Correlation*. The correlated processes (for example, electrical and thermal) and degrees of freedom (for example, spin and valley) in emerging nanomaterials hold promise for realizing spiking behavior that is significantly less developed than in synaptic devices.
- *Phase-Change*. Characteristic phase change behaviors in 2D materials, especially in 2D TMDs, reveals unique phase change behaviors. For example, MoS_2 transforms from the original trigonal prism (2H) into an octahedron (1T) through the intercalation of ions, resulting in a semiconducting-to-metallic transition [107],[108]. Various other methods, including charge transfer, irradiations, and stress inductions, can also induce phase change behavior in 2D TMD materials for the development of phase-change-based memristor devices [109],[110].

Already in 2017, Zhao *et al.* [105] reported sub-fJ resistive switching in an atomically thin oxidized *h*-BN layer. In 2018, Ge *et al.* [111], obtained a memristor effect in atomically-thin TMDs (MoS_2, $MoSe_2$, WS_2, WSe_2) and coined the term *atomristor*, which also presented a non-volatile resistance switching phenomenon. Owing to their mechanical resilience, 2D materials are well suited for flexible applications. Indeed, several flexible endured neuromorphic devices have already been demonstrated [112]. 2D are also promising for wearable neuromorphic technologies such as neuro-prosthetics due to their inherently thin architecture, their additional capacity for chemical sensing and their biocompatibility. These further enable neural interfaces, edge computing and afferent neurons in embodiments such as artificial skin [113]. Of these applications, one of the more advanced examples is 2D graphene neural interfaces [114].

3.2 2D Graphene Neurotechnology

Advances in brain knowledge are intimately linked with the advance of neural interfaces in terms of spatial resolution and area covered. For an increase in spatial resolution, a decrease in the area of the electrodes is required, which is

limited by the electrode impedance. Improvements in electrode coatings (mainly PEDOT, IrOx or TiN) are used to decrease the electrode size to 100 μm^2 with spatial resolution up to 30 μm [115], for which the main limiting factor to increase the recording sites is the connectivity between the transducer and the electronics which are used to digitize the signals. Monolithic solutions integrate (in a CMOS compatible process) the electrode and the electronics, thus minimizing the connection distances and preserving the signal quality [116]-[118]. Due to the lack of flexibility of silicon substrates, monolithic solutions can only be applied to intra-cortical probes with high spatial resolution (up to 20 μm and up to 1344 sites per shank). Monolithic intra-cortical solutions offer a high spatial resolution at single cortical column level. To increase the area and obtain information from different parts of the brain, Musk [119] proposed an automated robot to place up to 92 threads of 32 electrodes at different positions in the brain; all these electrodes are connected to custom ASIC that implements the digitizer.

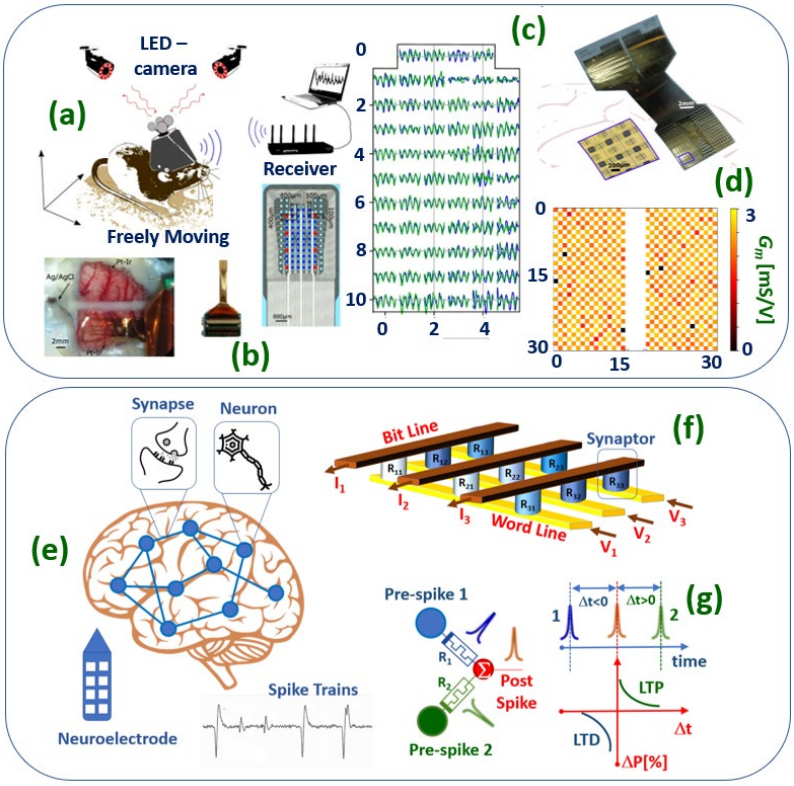

Figure 5. *Biological vs artificial spiking neural networks*. (a) An example of an in-vivo set-up for recording of biological spike trains. (b) Image of the flexible graphene neural probe made of an array of sGFETs. (c) Example of the local map of brain spikes after multiplexing. (d) A large g-SGFET arrays for epicortical recording. (e) Illustration of brain inspired spiking neural network and its' hardware implementation (f). (g) Illustration of spike timing dependent plasticity (STDP). LTP and LTD long-term potentiation and depression, ΔP[%] Synaptic weight change (plasticity change). Panel (a)-(c) adapted with permission from Garcia-Cortadella *et al.* [114] Springer Nature CC BY 4.0.

To overcome the connectivity limitations of the electrode based neural interfaces the use of onsite multiplexing strategies is required [120]. Chiang *et al.* [121] embeds silicon transistors in a flexible polyimide substrate to implement row/column addressing strategies and reduce the connectivity complexity. This strategy allows addressing of 1008 recording sites arranged in a 28x36 matrix, resulting in an impressive reduction of the connectivity complexity (34 wires to manage 1008 sites). The use of 2D graphene based solution-gated FETs (gSGFETs) as a transducer [122], will simplify the technology steps for implementing multiplexing strategies focused on the reduction of the connectivity requirements. Moreover, the use of gSGFETs has demonstrated a unique capacity to record high fidelity, infra-slow activity, providing information within the bandwidth of the electrophysiological signals. Arrays of multiplexed graphene-based active devices (FETs) in terms of number of active sites, site dimension, electronic noise, and sampling

frequency have also been evaluated. In-vivo assessment was also conducted using external switch multiplexing approaches, confirming the capacity of multiplexed graphene-based active devices for brain mapping. More recently, g-SGFETs technology has been upscaled to reach dozens and even hundreds of g-SGFET points with high yield and low noise [114] (Fig. 5(a)-(d)). The sensitivity of the devices, especially in the high frequency range (>100Hz), has been improved by protecting the graphene channel against contaminants during fabrication. This new technology also allows use of alternative passivation layers for improved long-term stability.

The computational requirements for efficient event-driven SNNs (Fig. 5(e)-(g)) set the basis for information and spike-based communication inspiring their incarnations at hardware level [123]. The sparse-event feature in particular suggest the requirement of highly interconnected memory arrays inspired by the neural networks of biological brain [124]. For example, memristor arrays are used to implement the filtering and identification of epilepsy-related neural signals, achieving a high accuracy of 93.46% and exhibiting nearly 400× improvement in the power efficiency compared to state-of-the-art CMOS systems, thus evidencing the feasibility of using memristors for high-performance neural signal analysis in next-generation brain–machine interfaces [125].

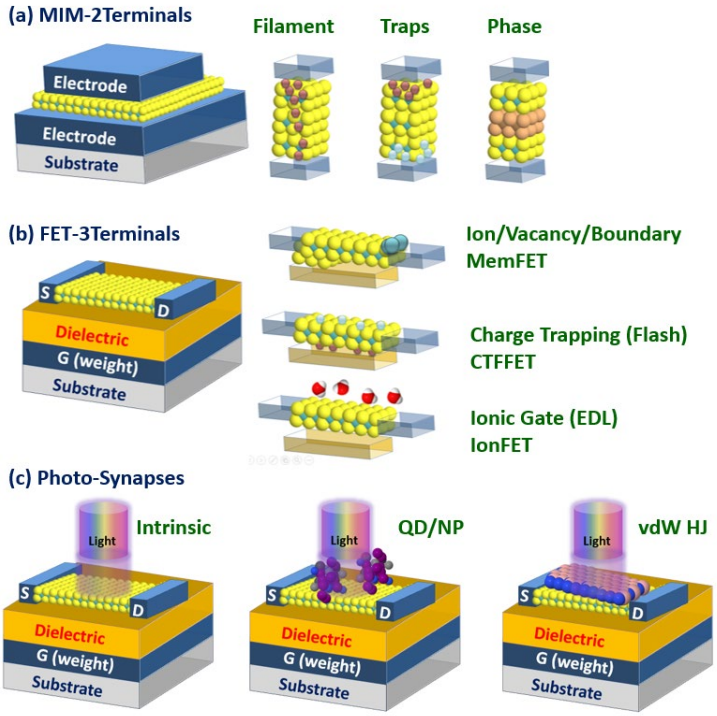

Figure 6. *2D-Synaptors*. (a) Schematic of a two-terminal MIM 2D-based memristor. (b) Schematic of a three-terminal 2D-based FET memtransistor. (c) Examples of photo-synapses.

3.3 2D Synapses (Synaptors)

Memory devices, also known as *synapses* or *synaptors*, are the core components of *beyond silicon in-memory computing* technologies. Synaptors made of 2D materials, are generally categorized as 2-terminal (*memristor*) or 3-terminal (*memtransistor*) devices. The vertical memristor consist of a metal–insulator–metal (MIM) sandwiched structure where a 2D insulator (or lightly doped semiconductor) works as the switching media (Fig. 6(a)). The memtransistor has a lateral three-terminal transistor structure (Fig. 6(b)) enabling gate tunability where grain boundary drift, ionic drift and/or trapping are the basis of the resistive switching. Specific examples of memtransistors include the charge trap flash FET (CTFFET) based on a charge tunneling mechanism and the ionic transistor which uses ionic coupling in order to realize conductance modulation (ionFET). However, it is noted that the specific charge transport mechanisms responsible for neuromorphic applications may vary depending on different intrinsic and extrinsic factors such as their constituent elements, how the devices are operated or if they are from an exfoliated flake or a CVD process. Indeed, there is an

increasing variety of phenomena described for 2D memristors and memtransistors in which traps are the usual suspects. For example, in many 2D synaptor FETs, interfacial charges at the gate oxide interfaces are believed to be responsible for starting resistive switching at small biases due to the exceptionally high surface-to-volume ratio and ultra-thinness of 2D materials [126]-[128]. In other synaptor embodiments, the interfacial charges are believed to be located at the 2D/electrode Schottky barrier due to the local redistribution of defects (e.g MoS_2 grain boundaries) [129] or electric field driven movement of the mobile OH^- ions along the vertical MoS_2 layers [130]. Defects can also be created extrinsically by using helium-ion (He^+) beam irradiation [131] or focused electron-beam irradiation [132]. As well as all of the above, the assembly of various 2D layered materials into heterostructures or the use of illumination have further diversified synaptic mechanisms [133]-[139].

A. Diode-type (2-terminal devices)

The demonstration of atomically thin (< 1 nm) vertical memristors made of a monolayer TMDs has shifted the paradigm that the leakage current across a 2D material would prevent the definition of 2D vertical synaptors [140]. In MoS_2 for example, atomistic imaging and spectroscopy reveal that metal substitution into a sulfur vacancy results in a non-volatile change in the resistance due to a single-defect memristor effect [141]. TMDs of the form MX_2 (M = Mo, W; X = S, Se) sandwiched between Au electrodes have already exhibited high switching ratios (> 10^4). Analogously, Shi *et al.* [142] demonstrated MIM memristors made by chemical vapour deposition (CVD)-grown *h*-BN[31]. As for 3D oxide memristors, the formation of filaments within 2D MIM structures has been a recurrent explanation for neuromorphic non-volatile resistive switching behavior. A type of filament formation includes the migration of ions stemming from their electrodes (also known as electrochemical switching or a conductive bridge) [143]. For example, few-layer *h*-BN two terminal synaptors contacted by electrochemically active metals (Cu or Ag) exhibited bipolar and unipolar resistive switching [144]. The filamentary ion drift local pathways can be modulated by the presence of in-plane grain boundaries [145] and/or by engineered intercalations in between each 2D layer [146]. Surprisingly, even in their embryonic stage of development, the resistive switching in 2D memristors has been observed to be more robust for certain embodiments than current oxide memristors. Wang *et al.* [147] reported few-layer MoS_2 memristors sandwiched between graphene layers operating at 340 °C while conventional metal oxide memristors only reach 200 °C. N-type donor sulfur vacancies (*on*-state) and oxygen (MoO_x) (*off*-state) exchange was evidenced by in-situ microscopy. Other non-filamentary approaches to produce resistive switching include the transformation of phases (the 3D bulk analogies are phase change memories made of chalcogenides, such as $Ge_2Sb_2Te_5$) and charge trapping/detrapping. A large number of 2D TMDs exist in various polymorphs exhibiting an electrically controllable phase change and solution-processed [148] 2H and 1T MoS_2 2D layers have already been implemented in vertical synaptors [149]. A number of authors have investigated 2D MoS_2 layers in heterostructures presenting memresistive behavior based on charge trapping/detrapping mechanisms. (see e.g. [150]-[155])

B. Transistor-type (3-terminal devices)

Although their pitch is larger and three electrodes increase the contacting complexity, one expected advantage of the three-terminal 2D memtransistor is the sneak path current mitigation within a neural network array. The sneak current is a current flowing through unselected cells that has a detrimental effect on the network accuracy of neural networks. Memtransistors could integrate the one-transistor, one-resistor architecture within a single device using a relatively simple fabrication process (Sangwan 2020). It has also been argued that three-terminal devices are required for heterosynaptic plasticity; FETs being more suitable for accommodating certain learning rules in various applications such as sound localization [156]-[159]. The gate electrode modulation of the synapse is considered as an emulation of a biological process of dendritic integration (See e.g. [160]). Several studies have investigated CVD-grown monolayer MoS_2 in lateral memtransistors [129],[145],[161]). Indeed, CVD-grown 2D materials contain lots of inherent defects, which can be cumbersome when used as a channel or gate dielectric in FETs but are useful for biomimics applications. Gate-tunable memristive switching was observed in sub-stoichiometric monolayer MoS_2 devices with individual grain boundaries in the channel [145]. However, the switching characteristics of these devices depend strongly on grain boundary topology, which may limit large-area uniformity. Thus, scalable memtransistor arrays were subsequently realized in polycrystalline MoS_2 with grain sizes that were much smaller than the channel area such that the effects of individual grain boundary geometries were averaged at the device level. The open architecture of the 2D channel further enabled multi-terminal heterosynaptic plasticity. While the initial devices possessed large operating voltages (>50 V), follow-up work reduced the operating voltage by an order of magnitude by using smaller grain sizes and ultrathin dielectrics [129].

2D materials have become a platform of choice for ionic transistors in high-performance and biological multi-function matrix computing for SNNs due to their atomic-scale layered structures and consequent special properties. Usually, 2D materials and electrolytes are used in combination in order to achieve neural synaptic electronics in SNNs [162]-[164]. Compared to the limited ion control and coupling capabilities of conventional electrolyte transistors, the surface area to volume ratio resulting from the thickness reduction of a 2D material is large, and there is a vdW gap between the layers, which is desirable for enhancing the ion gating and achieving low power consumption in a synaptic transistor. Exploiting a novel multigated architecture incorporating electrical, ionotronic and optical biased 2D memtransistors may offer charge-trapping probabilities to finely modulate the synaptic weights as well as amalgamate neuromodulation schemes for "plasticity of plasticity–metaplasticity" via dynamic control of Hebbian spike-time dependent plasticity and homeostatic regulation [165]. Since 2D nanomaterials possesses exceptionally high surface-to-volume ratios, they not only interact with oxide traps but also allow post-growth defect engineering for synaptic transistors and multi-level memory. For example, in-plane lithium-ion intercalation in few-layer WSe_2 showed reduced energy consumption (~30 fJ per event) and superior linearity and symmetry [166]. These diffusive dynamics have been generalized to other 2D nanomaterials and polymer electrolyte dielectrics [167]. Yang *et al.* [168],[169] have also illustrated the feasibility of engineering 2D materials in an ionic transistor with ultralow programming energy. Yang et al. first proposed an ionic transistor based on a 2D transition metal oxide with a precise conductance modulation over 100 states linearly and symmetrically. Benefitting from the layered structure of α-MoO_3, it facilitates the intercalation of diverse cations, enabling better tunability [168]. Similarly, controlling the ion concentration in the graphene layer or WSe_2 also realized analogue tunability (>250 non-volatile states) with a linear and symmetric conductance response. [170].

C. 2D Optoelectronic Synapses

Light stimulation is an emerging means for conductance modulation due to the excellent optical properties of 2D materials. The optoelectronic synapses can broadly be categorized as *intrinsic*, *hybrid* or *heterostructures* (HJ or vdW, if these are made of vdW materials) (Fig. 6(c)). In intrinsic 2D optical materials the photo-absorbing layer is the same as the conducting channel and the switching media. In particular, TMDs show layer-dependent optical and electrical properties. When exfoliated into monolayers, the band gaps of several TMDCs change from indirect to direct, which leads to broad applications in nanoelectronics, optoelectronics, and quantum computing. Owing to its' quantum confinement, an MoS_2 monolayer exhibits a direct bandgap of ~1.8 eV (while in the bulk form it has an indirect bangap of ~1.23 eV). Examples of intrinsic optoelectronic synapses are e.g. the demonstration of MoS_2 on SiO_2 with a *p*-type germanium substrate back-gate absorbing in the infrared by band-bending modulation [171] or few-layer MoS_2 onto Ta_2O_5-TiO_2 (charge trapping layer) absorbing in the visible [172]. Indeed, photo-synapses in a charge trap memory arrangement exhibit a large number of levels e.g. (3-bit/8-levels) [173] and a large linear dynamic range of ~4,700 (73.4 dB), low off-state current (<4 pA), and a long storage lifetime 10^4 s [174]. Analogously, Tungsten Disulfide (WS_2) exhibits an indirect optical bandgap of ~1.35 eV in its bulk form, but it broadens up to a direct optical bandgap of ~2.05 eV. Luo *et al.* [175] implemented WS_2 in optoelectronic synapses made onto ferroelectric lead zirconate titanate ($Pb(Zr,Ti)O_3$ or PZT) thus forming a 2D-ferroelectric oxide interface photo-synapse where the WS_2 channel photo-conductivity was further modulated by the switchable ferroelectric polarization of PZT. With a direct bandgap of ~1.7 eV, a monolayer of Tungsten Diselenide (WSe_2) is ideally suited to harvest light in the visible. Mennel *et al* [176] presented an artificial neural network (ANN) vision sensor based on a WSe_2 photodiode array for ultrafast recognition and encoding of pictures demonstrating that an image sensor can itself constitute an ANN that can simultaneously sense and process optical images without latency. A reconfigurable 2D semiconductor photodiode array, and the synaptic weights of the network were stored in a continuously tunable photoresponsivity matrix in order to classify and encode images that were optically projected onto the chip with a throughput of 20 million bins per second. Black phosphorous (BP) is a 2D allotrope of phosphor with a structure similar to graphite and a narrow bandgap of ~0.34 eV, which makes it suitable for harvesting in the infrared region. Ahmed *et al.* [177] oxidized few layer BP into phosphorous oxide, thus tuning the photoresponse in the synaptic devices to the UV range of 280 nm/365 nm (excitatory/inhibitory positive/negative photo-current).

Hybrid channels are used, based on incorporating nanoparticles into the 2D semiconductor channels. These nanoparticles are sensitive to a particular wavelengths of visible light and can create photo-generated carriers upon illumination. Examples of hybrid optoelectronic synapses are photo-absorbing organic-inorganic halide perovskite quantum dots QD/graphene (to operate in the visible) [178] or inorganic silicon nanocrystals Si-NC/(few layer) WSe_2 (for broadband UV-NIR photo-stimulation) [179]. The QD/graphene perovskite phototransistors exhibit a remarkable responsivity of 1.4×10^8 A/W and a specific detectivity of 4.7×10^{15} Jones at 430 nm. A light-assisted memory effect enables photonic synaptic behavior, demonstrating neuromorphic facial recognition with the assistance of machine learning. A good

example of 2D photo-synapses in a heterostructure is given for optoelectronic resistive random access memory (ORRAM) by Zhou *et al.* [180]. They reported an ORRAM synaptic device with a simple two-terminal structure of Pd/MoO_x/ITO (ITO, indium tin oxide) that exhibits ultraviolet (UV) light sensing, optically triggered non-volatile and volatile resistance switching and light-tunable synaptic behaviours. They demonstrated image sensing, image memorization and real-time preprocessing functions for image contrast enhancement which can effectively improve the image quality, and increase the processing efficiency and the accuracy of subsequent image recognition. An example of a bulk semiconductor/2D heterojunction (HJ) optical synapse is given by He *et al.* [181], reporting a CVD-grown monolayer MoS_2 as the conducting channel on *p*-Si where photo-generated electrons and holes are separated by the built-in electric field across the *n*-MoS_2/p-Si HJ. When the HJ active layers are made of 2D materials, they are commonly referred as vdW HJs, as for example *h*-BN/MoS_2 [182], graphene/MoS_2 [183] or *h*-BN/WSe_2 [184]. Compared to intrinsic 2D, the vdW heterostructure usually results in larger photo-synaptic dynamic range: Xiang *et al* [185] reported a *h*-BN/WSe_2 HJ with a high dynamic range of 10^6, 128 current states (7 bit) and a retention time of 10^4 s.

D. 2D-Synapses Spike-based Learning & Energy

Synaptic plasticity is regarded to be a central neurochemical mechanism for memory and learning. In biological brains, synaptic plasticity is modulated by varying the total number of neurotransmitters exchanged between neurons in a synaptic event and the individual neurotransmitter efficiency response. A central topic in neuromorphic engineering is, therefore, to mimic synaptic plasticity at a hardware level. In contrast to normal deep neural networks (DNN), a neuronal unit in a SNN is only active when it receives or emits spikes [10]. Different spiking neuron models with different levels of bio-fidelity have been proposed to describe the generation of spikes including the leaky integrate-and-fire (LIF), Hodgkin–Huxley (H-H), FitzHugh–Nagumo, Morris–Lecar or Hindmarsh–Rose [13]. Similarly, for synaptic plasticity, schemes such as Hebbian and non-Hebbian have been proposed. Hebbian synaptic plasticity—the modulation of synaptic weights, which translates to learning in SNNs—relies on the relative timing of pre- and post-synaptic spikes. In practice, synaptic plasticity implemented in SNNs mainly encompasses short-term synaptic plasticity (STP) and long-term synaptic plasticity (LTP). For spiking neural network applications, the spike timing and frequency encoding method requires memory devices with both *volatile* and *non-volatile* characteristics [14]. Based on neuroscience and considering the hardware energy efficiency as the most important figure of merit, unsupervised SNN training using local spike-timing-dependent plasticity (STDP)-based learning rules is the common approach.

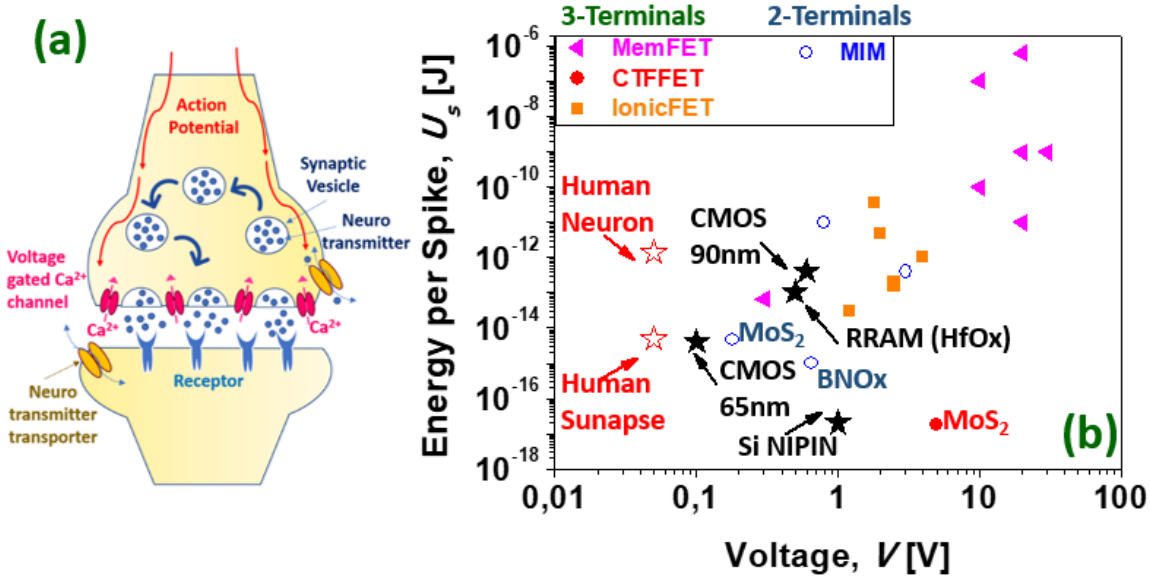

Figure 7. *2D Neuromorphic energy per spike map*. (a) Illustration of a biological synaptic event. (b) Energy per spike vs switching voltage map for 2D-based selected 2-terminal memristor and 3-terminal memtransistors devices from the literature. Black stars represent the state-of-the-art for CMOS neurons/synapses and metal-oxide RRAM memristors.

A number of vertical two-electrode neuromorphic devices have been reported to exhibit STP, LTP learning such as MIM $Ag/MoO_x/MoS_2/Ag$ (and $Ag/WOx/WS_2/Ag$) [186], graphene/2D perovskite [187] and STDP unsupervised learning (e.g. $ZnO/WS_2/Al$ [188], WS_2 [189] or in *n*- and *p*-channel MoS_2 transistors by utilizing charge trapping dynamics [190]). However, to realize practical neural networks, the 2D switching media should be defined by large-scale synthesis (e.g. CVD-growth) as in Krishnaprasad *et al.*, [183] where $Au/Ni/MoS_2$/graphene exhibited superior linearity for STP, LTP, STDP or Xu *et al.* [143], who demonstrated an ultra-low 100mV switching CVD MoS_2 synapse $Cu/MoS_2/Au$. Analogously, by exploiting the defect dynamics due to vacancies (generally chalcogenide S, Se, Te vacancies in TDMs), interfacial traps or grain boundaries, volatile and non-volatile resistive switching and synaptic plasticity have been reported in 2D memtransistors [129],[161]. Memtransistor heterosynaptic plasticity has been widely reported for 2D exfoliated flakes such as BP (BP flake FET exhibiting STDP [156]), MoS_2 (FET large hysteresis back-gated inhibitory and excitatory [126]), vdW HJs such as MoS_2/graphene (floating gate 10^5 cycles [151]) but also on CVD-grown 2D layers such as MoS_2 [129].

Since energy consumption is a major issue for big data applications, there is a strong interest in decreasing the power consumption of silicon chips. Current implementations of SNN on neuromorphic CMOS hardware [191] use only a few nJ or even pJ for transmitting a spike [192], although some setups have shown much less power consumption per spike event, for example 0.4 pJ (CMOS 90nm [193]), 4 fJ (CMOS 65nm [194]) and even as low as 20 aJ for a Si-based CMOS compatible asymmetric NIPIN diode as an LIF neuron [195]. An important figure of merit for 2D synapses is, therefore, the energy per spike where a typical low value for a RRAM oxide based memristor is 0.1 pJ [196]. As shown in Fig. 7, some reported 2D synapses have already exhibited ultra-low energy per spike (below fJ). Particularly low values were reported in work such as Zhu *et al.* [166] (for a diffusive dynamic ionic MoS_2 transistor consuming 30 fJ per spike), Zhao *et al.* [105] (in an atomically thin *h*-BN memristor (~fJ)), Feng *et al.* [197] (in an aerosol-jet-printed $Ag/MoS_2/Ag$ memristor (4.2 fJ)), and Wang *et al.* [198] (18.3 aJ for long-term potentiation on flexible MoS_2 with photoelectric dual modulation).

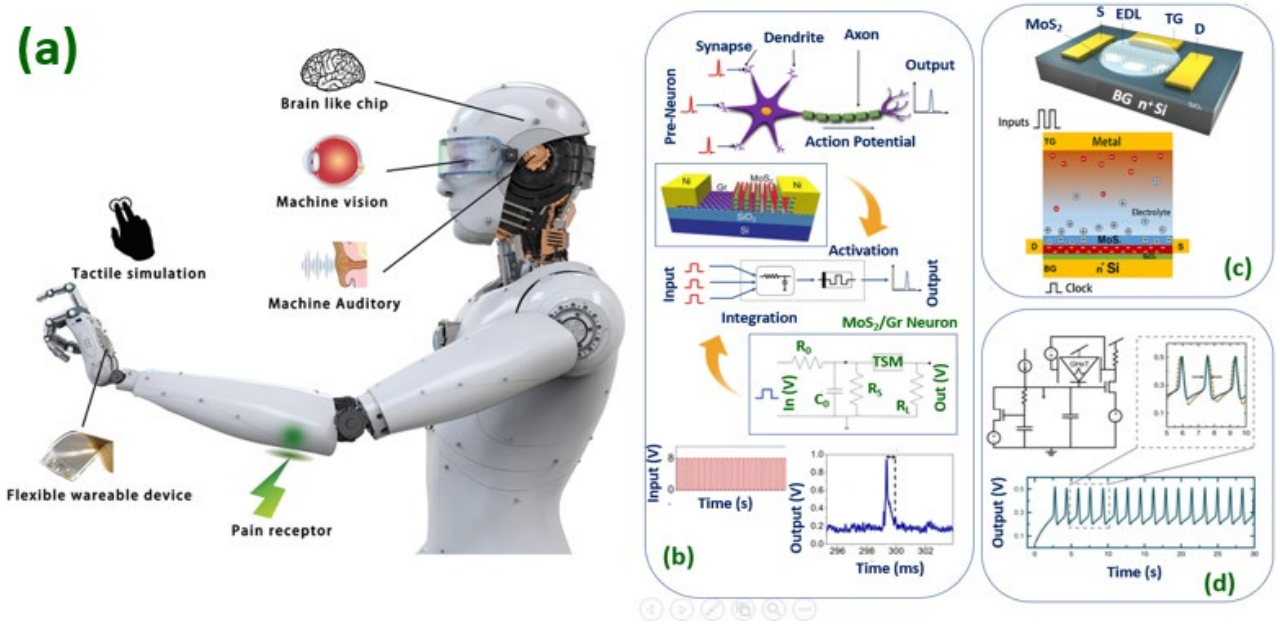

Figure 8. *Brain-machine Interface: 2D-Synaptors & 2D-Neuristors*. (a) The application prospect of synaptors in the fields of bionic intelligent products and human–computer interaction with permission from Sun *et al.* [209] ©John Wiley and Sons. (b) Neuristor made of 2D MoS_2 threshold switching memristors (TSM). (c) Neuristor operation in an ionic liquid gated 2D MoS_2 FET. (d) Neuristor circuit with a Gaussian 2D MoS2/graphene FET. Panel (b) adapted with permission from Kalita *et al.* [213] Springer Nature CC BY 4.0. Panel (c) adapted with permission from Bao *et al.* [217] Springer Nature CC BY 4.0. Panel (d) adapted with permission from Beck *et al.* [92] Springer Nature CC BY 4.0.

These ultra-low power synapses further reinforce the potential of 2D materials for the future of spiking artificial intelligence with ultra-low power matrix computation and neuromorphic massively parallel computing units. Large-area MoS_2 can also be an active channel material for developing logic-in-memory devices and circuits based on e.g. floating-gate FETs [199], highlighting the potential of atomically thin semiconductors for the development of next-generation low-power electronics. Neuromorphic computing, therefore, holds the promise of breaking the current von Neumann bottleneck for computer energy consumption by mitigating the traffic between the memory unit and the computing unit (or *memory computing)*. In the same way, *in sensor computing* [200],[201] combines sensing (e.g. visual, auditory, tactile, thermal or olfactory) with neuromorphic computing is a way to mitigate the analog-to-digital conversion energy consumption (and time latency) when sensor information is converted to a digital electronic format and passed to a computing unit for sensor information processing. In-sensor computing (by implementing an artificial neural network directly in the image sensor) has been demonstrated recently with various materials including WSe_2 [176],[202]-[204], MoS_2 [205] and BP [206]. A neural network of atomically-thin photodiodes, for which light responsivity is modified by an external voltage, may alter the connection strength (the synaptic weight) learning from their surroundings by iteration in a supervised or unsupervised fashion. During learning, an algorithm repeatedly makes predictions and strengthens or weakens each synapse in the network until it reaches an optimum setting. With the advent of deep learning for artificial intelligence, *computing-in-sensor* is becoming a necessity. As stated by Rodriges *et al.* [207], the training process of a convolutional neural network on a 4 GPU system for 1 week requires about 180 W (~32 kWh) of energy expenditure (or more) for distributed processing (N.B. the average 2018 EU household consumption is ~21 kWh per week). Thus it was projected that the power consumed by such neural networks could exceed the total power generated in the world by 2042. Mimicking neurobiological structures and functionalities of the retina provides a promising way to build a neuromorphic vision sensor with highly efficient image processing [208]. And overall, this is only one of the great prospects of memresistive devices in the fields of bionic intelligent products and human–computer interaction [209] (Fig. 7(a)).

3.4 2D Neurons (Neuristors)

At a neuromorphic hardware level, *synaptors* emulate the synaptic connection between neurons while the other basic device is a spiking neuron itself, or *neuristor*. Neuristors are the active elements of a neuromorphic circuit which mimic the essential features for action-potential (i.e. nerve impulse) computing; (i) threshold-driven spiking (all or nothing response after an electric spike), (ii) lossless spike propagation and (iii) shape and a refractory period (short memory) [13]. Neuristors circuits have approximated this spiking behavior by a series models for action potential generation such as the (H-H) and LIF. A simple device or circuit with threshold properties is generally sufficient to achieve the simplest LIF neuron model. However, neuristors with a larger degree of bio-fidelity would require more complex circuits. CMOS-based neurons are widely used for neuromorphic close-memory big brain chips [192]. For non-CMOS *beyond silicon* neuromorphic technologies, the threshold-driving spiking may be enabled by a volatile resistive switching phenomenon: the material remains insulating until a threshold field is reached, resulting in a resistance collapse. The device returns to its original insulating state when the field is removed with a characteristic relaxation time (replicating the refractive period of neurons). That required additional short memory may come from the relaxation time of some volatile resistive switching phenomena [210]. Pickett *et al.* [211] demonstrated in 2012 that the Na^+ and K^+ ion channels of the H-H model are mathematically equivalent to two volatile NbO_2 resistive switches undergoing an insulator-to-metal transition. Biological systems are, however, much more complex than simple integrate-and-fire behavior:up to twenty-three types of biological neuronal behaviors have been experimentally demonstrated. For example, Yi *et al.* [212] suggested that scalable active metal-insulator-transition VO_2 RS neurons possess all three classes of excitability (Hodgkin's classification) and most of the known biological neuronal dynamics.

Analogously, during the past few years, a number of atomically-thin neuristors have been reported based mostly on different volatile resistive switching phenomena taking place in 2D-memristors and 2D-memtransistors. 2D-Based neurons made of threshold switching memristors have been implemented on MoS_2 MIMs such as Ni/MoS_2/graphene/Ni [213], Au/MoS_2/Ag [214], and Ag/MoS_2/TiW [215]. Kalita *et al.* [213] exploited the volatile threshold behavior of a vertical-MoS_2/graphene vdW system (large area CVD-grown multilayer) to produce the integrate-and-fire response of a neuron which was connected to a resistor-capacitor (RC) circuit to demonstrate an artificial neuron (Fig. 8(b)). Upon application of input voltage pulses, the RC circuit integrated the incoming signals and built up a potential across the TSM device. Memresistive filamentary conductive bridge Ag electrodes were applied into MoS_2-based TSM devices so that a positive bias applied at the Ag electrodes caused the Ag^+ to diffuse through the MoS_2 so as to form conductive

filaments, hence making the volatile high resistance-low resistance transition [214],[215]. The Dev *et al.* [214] Au/MoS_2/Ag vertical 2D TSM exhibited a low threshold voltage of 0.35–0.4 V and a high on/off ratio of 10^6. Hao *et al.* [215] defined a 2D-memristive spiking neural network by incorporating MoS_2-based neurons and a Cu/GeTe-based synapse so as to demonstrate the computing ability (pattern classification) of the 2D-neural network. Chen *et al.* [216] made another demonstration of a LIF neuron without an external circuit using a 2D MXene (Ti_3C_2)-based TSM device.

2D MoS_2 FET-based neuristors have also been demonstrated, exploiting different conductive channel field-effect mechanisms such as in 2D dual-gate ionic, Gaussian or split-gates transistors (see e.g. [217], [92], [159]). Bao *et al.* [217] demonstrated a neuristor made of a dual-gated exfoliated PEO:$LiClO_4$ ionic MoS_2 FET (Fig. 8(c)). The top liquid gate controlled ionic migration, while the solid back gate SiO_2 modulated the FET channel population. The ionic drift of Li^+ from the top gate resulted in STP, LTP, and PPF learning. When both, top and back gates were simultaneously biased they emulated the propagation of action potential through the axon of biological neurons. The sampling clock applied at the back gate was not capable of populating the MoS_2 channel with *n*-type carriers, hence no current flowed from the drain to source. Das *et al.* [159] demonstrated a neuristor made of an exfoliated MoS_2-based multiple split-gate transistor. This split-gate neuristor turned on when a pair of split gates received the input voltage pulse simultaneously and was further implemented in an audiomorphic computing system. Beck *et al.* [92] demonstrated an H-H spiking neuron adopting a Gaussian HJ transistor (GHeT). CVD-grown monolayer MoS_2 and carbon nanotubes (CNTs) were used to form the *p*-*n* junction for a dual-gated GheT, which consumed 250 nJ per spike (Fig. 8(d)). Serial assemblies of *n*-type (MoS_2) and *p*-type (BP) 2D transistors with appropriate threshold voltages can also result in Gaussian characteristics that have been used to implement probabilistic neural networks [91]. In summary, the synaptic activity can, therefore, be effectively manipulated by tailoring the electronic or ionic gating with varied thickness and structure of the vdW material as well as the number, duration, rate, and polarity of gate stimulations, making 2D transistor-based neuristors candidates for low-power artificial neurons.

4. CONCLUSIONS

The rational use of electrical energy and information are central themes in the greatest climatic challenge of the 21st century. UWBG oxides, such as Ga_2O_3 and related materials, are promising power electronic candidates since their critical electric field is large compared to *beyond silicon* WBG (i.e., SiC and GaN), while still yielding a moderate mobility, high quality epi-layers and large bulk single crystals (more than 6-inch) using low cost and scaleable fabrication approaches. During the last nine years, the Ga_2O_3 power diode and transistor progress has been impressive, with devices now approaching the frontier of the field. The material system also opens new optoelectronics avenues (owing its' UVC spanning bandgap), and new electronics perspectives based on stabile interfaces and a natural integration with extremely high-*k* functional oxides. The advances offered by of Ga_2O_3 are also opening the door to many more UWBG oxides (the largest family of wide bandgap semiconductors) such as the spinel, $ZnGa_2O_4$, along with many more that are anticipated. While a *deterministic* ultra-high critical field is a *sine qua non* condition for managing large amounts of electric current, a *probabilistic (Bayesian)* ultra-low resistive switch is desirable for an emerging and more energy efficient neuromorphic computing paradigm based on mimicking the human brain. Ultra-thin 2D materials such as graphene, MoS_2 and *h*-BN, are ideally suited for defining *beyond silicon* ultra-low power artificial synapses and neurons in a variety of arrangements, as has been demonstrated the past few years. 2D materials have already been demonstrated their power for non-von Neumann *in-memory* and *in-sensor* computing neural networks, thus helping to make energy-efficient AI a possibility. Therefore, the ever-increasing family of UWBG oxides and atomically-thin layered materials are at the very frontier of a more efficient energy electronics which is adapted to tackle the 21st century climatic and big data objectives, although there still is a lot of room for performance improvements, technical innovation and new discoveries.

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