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Tunability Properties and Compact Modeling of HfO₂-Based Complementary Resistive Switches Using a Three-Terminal Subcircuit

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Abstract— Complementary resistive switching (CRS) arises when two bipolar-mode memristive devices are anti-serially connected, forming a single functional structure. The combined effect of both memristors leads to the appearance of high and low resistance windows in the current-voltage (*I-V*) characteristic that finds application in fields such as neuromorphic computing and logic circuits. In this work, the electric behavior of HfO₂-based CRS devices intentionally fabricated with a common central electrode is investigated both from experimental and modeling viewpoints. Experiments reveal that the maximum voltage applied to the structure allows tuning the amplitude of the resistance window following a self-balance dynamics. The origin of the abrupt (digital) and gradual (analog) transitions between the high and low resistance states is elucidated through the inclusion of the snapback and snapforward effects in the switching dynamics. The *I-V* characteristics of the CRS devices are compact modeled with two opposite-biased memdiodes and simulated in LTSpice using an equivalent three-terminal subcircuit. It is shown that the proposed model is able to reproduce with a high degree of accuracy not only the observed CRS behavior for HfO₂ but also the main features exhibited by devices with a wide variety of oxide/electrode materials.

Index Terms— complementary resistive switching, CRS, HfO₂, memristor.

I. INTRODUCTION

COMPLEMENTARY RESISTIVE SWITCHING (CRS) has been proposed as a circuitual technique able to reduce the sneakpath conduction problem in ReRAM-based crosspoint-type memory arrays used for neuromorphic computing [1]. Structurally, CRS is the result of the anti-serial combination of two electroformed Metal-Insulator-Metal (MIM) capacitors forming a single two-terminal device. The connection point between both MIM structures is generally disregarded (left floating) or just used for sensing the behavior of the individual structures. However, when different input signals are applied to the pins of the CRS device or when they are short-circuited, the central contact operates as an essential terminal of a new device. This occurs in a number of configurations aimed at performing

logic operations such as the IMPLY [2],[3], MAGIC [4], and MIN-MAX gates [5]. In addition, there is another type of CRS device which does not have a central metallic electrode but whose conducting behavior is the consequence of the dissimilar electrical properties exhibited by the electrode-oxide interfaces of a single MIM structure [6],[7]. In this case, the device can block or allow the flow of electrons depending on the voltage drop at each interface giving rise to a pseudo-CRS behavior [8].

TABLE I
CRS MODELS BENCHMARK

Features	This work	QMM [15]	[10]	[11]	[12]	[13]	[14]
Snapback and snapforward	✓	✓	✗	✗	✓	✗	✓
Triggered set transition	✓	✓	✗	✗	✗	✗	✗
Gradual reset option	✓	✓	✗	✗	✓	✗	✗
Full-time dependence	✓	✗	✓	✓	✓	✓	✓
Tested for a variety of materials	✓	✓	✗	✗	✗	✗	✗
Implemented for circuit simulators	✓	✓	✓	✓	✗	✓	✗
Code available (Copy&Paste)	✓	✓	✗	✓	✗	✗	✗
Three-terminal compact model	✓	✗	✗	✗	✗	✗	✗

Comparative table for a number of CRS models found in the literature. The features reported in this table are discussed along the text. QMM refers to the quasi-static memdiode model [15]. Triggered set transition means a hard threshold for the potential drop across the device. The gradual reset option means VCM or ECM-type transition. Full-time dependence means set and reset processes driven by a first-order time differential equation.

In most of the cases, a CRS device is fabricated using two bipolar resistive switching (RS) structures or memristors which

alternately switch to generate a conducting window between two threshold voltages. The kind of RS mechanism we are discussing here is a nonvolatile effect, *i.e.* the resistance of the whole structure remains unaltered when the input signal is unable to induce a change of state. Since each RS structure is characterized by its own high (HRS) and low (LRS) resistance states and set (V_S) and reset (V_R) voltages, the combination of devices does not necessarily yield a symmetric output curve. Moreover, asymmetries can also arise from a number of issues such as variability associated with the fabrication process, the electroforming step, or the RS physical mechanism itself. These are the reasons why a flexible and compact model for the simulation of CRS devices is strongly required. Several CRS models can be found in the literature, such as a physics-based nonlinear memristive model for two anti-serially connected ECM cells [9],[10], a Verilog A-based CRS model [11], a model that reproduces the abrupt set and gradual reset transitions [12], a model for extended HP-memristor [13] and a physics-based model to describe RS and CRS [14]. Table I describes some features of each model found in the literature along with our previous quasi-static model [15]. Many of the points referred to in Table I will be discussed along the text. One central feature of the model reported here is that it allows simulating the abrupt or gradual current transitions thanks to the inclusion or exclusion of the so-called snapback and snapforward effects [16] in combination with a trigger condition. This leads to a wide variety of behaviors in the current-voltage (I - V) characteristic that many of the aforementioned models are not able to cope with. In addition, our model script is written in LTSpice code so that it can be straightforwardly used for simulating complex circuits without focusing the attention on numerical and time discretization issues. It is also worth pointing out that the experimental data reported in this work were obtained from HfO_2 -based CRS devices with an accessible central terminal. The devices were deliberately fabricated this way and they are not the result of the external connection of two isolated structures [17]. The availability of a third input/output terminal opens the door to new applications not considered until this moment. To put a simple example, among these applications could be the external control of the set and reset voltages of the structures.

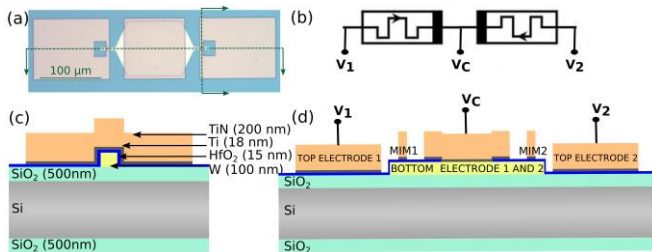


Fig. 1: (a) Optical image of the fabricated anti-serially connected TiN/Ti/HfO₂/W memristors with a common central electrode. (b) Electrical scheme. (c) Vertical and (d) horizontal schematic cross-sections (indicated by the dotted green arrows in (a)).

This paper is organized as follows: in Section II, the CRS device fabrication procedure is reported. The electrical

characterization and tuning capability of the fabricated devices are discussed in Section III. In Section IV, the Dynamic Memdiode Model (DMM) is briefly introduced. In Section V, experimental and simulated curves using LTSpice, obtained with different electrical stress conditions and various electrode/oxide material combinations are reported. In section VI, the use of the proposed three-terminal subcircuit compact model to perform in logic circuits is shown. Finally, conclusions are presented in Section VII.

II. DEVICE FABRICATION AND MEASUREMENTS

Anti-serially connected TiN/Ti/HfO₂/W MIM devices with a common bottom electrode were fabricated on Si wafers [18]. The fabrication process started with the thermal oxidation of the Si substrate, leading to a 500 nm-thick SiO₂ isolating layer. A 100 nm-thick W bottom electrode was deposited by magnetron sputtering and patterned by photolithography and wet etching. After that, a 15 nm-thick HfO₂ insulating film was grown by Atomic Layer Deposition (ALD) at 225 °C using TDMAH and H₂O as precursors, and N₂ as carrier and purge gas. Subsequently, the HfO₂ film was opened at the contact areas of the bottom electrode by photolithography and dry etching. Finally, the top electrode composed of 200 nm TiN and 18 nm Ti was deposited by magnetron sputtering and defined by a lift-off process. The area of each structure is 5×5 μm². Figures 1 (a)-(d) show a top view optical microscope image, the electrical scheme, and the vertical and horizontal schematic cross-sections of the fabricated device structures, respectively. The electrical characterization of the devices was carried out using a Keysight B1500 semiconductor parameter analyzer. Voltage ramps were programmed with a sweep rate of ~ 0.2 Vs⁻¹. In order to control the instrumentation and to perform successive and automatic measurements, a software tool was developed in MATLAB.

III. ELECTRICAL CHARACTERIZATION AND TUNABILITY PROPERTIES OF THE FABRICATED DEVICES

In this Section, the CRS behavior exhibited by our devices is presented and discussed. The fabricated TiN/Ti/HfO₂/W devices are RS structures based on the filamentary-type valence change mechanism (VCM) [19]-[21]. The Ti capping layer acts as an oxygen scavenger that favors the formation and partial destruction of an oxygen deficient filamentary path [22],[23]. Figure 2 shows typical I - V loops obtained from single RS devices and from the complementary structure. The electrical characterization started with the electroforming process of the individual devices (not shown here) that led to the formation of an oxygen deficient conductive filament (CF) connecting the top and bottom electrodes and driving the device into LRS. This process was carried out by applying a positive voltage ramp with current compliance (I_{CC}) of 10 mA to prevent irreversible dielectric breakdown. In both devices, the voltage was applied to the TiN/Ti top electrode with the W bottom electrode grounded (see the insets in Figs. 2 (a) and (b)). The forming voltage of the individual TiN/Ti/HfO₂/W MIM devices was ~4.5V, while the current of pristine devices was below the current resolution (1pA) of the semiconductor parameter

analyzer. Subsequently, a reset process was induced by applying a negative voltage ramp to the top electrode, which resulted in a partially broken CF leading the device to HRS. Next, we tested the RS behavior in both devices separately. To this purpose, departing from HRS, a double voltage ramp from 0 V to 1.1 V was applied to the top electrode with $I_{CC}=10$ mA. It can be seen that the current abruptly increases at V_S , leading the device again to LRS. Physically, this process corresponds to oxygen anion migration from the dielectric layer to the Ti scavenging layer, whereby the oxygen deficient CF is rebuilt again. The reset process is then performed by applying a double voltage ramp from 0 V to -1.4 V. Notice that the device continues in LRS until the applied voltage reaches V_R , where the current abruptly decreases, bringing the device back to HRS. During reset, the migration of oxygen anions from the Ti layer to the dielectric layer and oxygen vacancy recombination processes take place, resulting again in the CF rupture and generating a gap or barrier along the filament pathway. It can be observed in Figs. 2 (a) and (b) that the RS behavior is similar in both devices but not identical. In addition, it is shown that the cycle-to-cycle variability is larger in HRS than in LRS. This fact can be explained by the cyclical variations of the barrier gap formed between the conductive filament and the electrode when the reset process is activated.

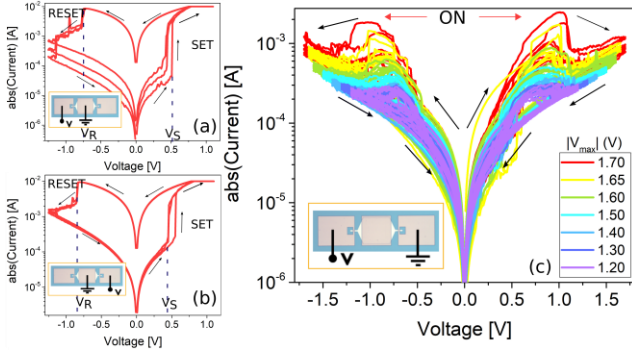


Fig. 2: (a)-(b) RS behavior of the individual devices for $V_{max} = [-1.4, 1.1]$ V and $I_{CC} = 10^{-2}$ A during the SET process. (c) Experimental CRS behavior of anti-serially connected devices for several $|V_{max}|$ values. Every 10 cycles $|V_{max}|$ is decreased from $V_{max} = [-1.7, 1.7]$ V to $V_{max} = [-1.2, 1.2]$ V. The inset in each figure shows a top view optical microscope image of the structure, where the biased and grounded terminals are indicated. Arrows indicate the voltage sweep directions for the RS and CRS phenomena.

For the CRS measurements (see Fig. 2 (c)), the voltage was applied to the top electrode of one of the devices, with the top electrode of the second device grounded. After initializing the devices individually as mentioned above and departing from one device in HRS and the other in LRS, some cycles were performed first in order to stabilize the switching behavior. After that, CRS was measured by applying a double voltage ramp from 0 V to $+|V_{max}|$, and then from 0 V to $-|V_{max}|$. During these processes, at a given voltage polarity, one device undergoes a set event, while the other undergoes a reset event at a higher voltage. Remarkably, CRS measurements were performed without I_{CC} since the current in one device limits the conduction in the other device acting as load resistance [19]. After several identical sweeps, a self-balance is reached and the I - V curve evolves towards a stable symmetrical state. As illustrated in Fig. 2 (c), two low-resistance regions (ON regions)

are generated at both sides of the curve characterized by a minimum resistance R_{ON} at the corresponding voltage value V_{ON} . In these regions, both devices are in LRS, while in the other regions of the cycle, the devices are either in opposite states or both in HRS.

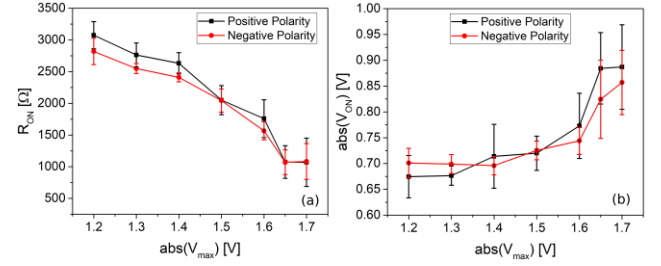


Fig. 3: (a) Average values for R_{ON} versus $|V_{max}|$, and (b) $|V_{ON}|$ versus $|V_{max}|$, for positive (black squares) and negative (red dots) voltage polarities. The error bars indicate the standard deviation.

The CRS behavior for $|V_{max}|$ values ranging from 1.7 V to 1.2 V can be seen in Fig. 2 (c). 10 cycles for each studied voltage were performed to evaluate the cycle-to-cycle variability. This variability is intrinsic to the RS mechanism, an issue out of the scope of this work. Notice that the maximum applied voltage is reduced during the experiment, which indicates that the induced changes are reversible. Obtained results reveal a remarkable dependence of the CRS window (R_{ON}) on the maximum voltage applied to the structure. Furthermore, for the highest V_{max} values, the transitions between states become more abrupt due to the occurrence of the snapback and snapforward effects that take place in the set and reset processes during the CF growth and dissolution, respectively. As it will be shown in the next Section, these effects are related to the series resistance effect [24],[25]. The series resistance limits the current during the set process and acts as a voltage divider during the reset [26]. Understanding this kind of analog to digital transition and *vice versa* is a key feature for properly modeling the shape of the I - V curve. In order to get further insight into how the operating conditions affect the CRS behavior and to quantitatively assess the symmetry of the I - V curves, a systematic analysis of R_{ON} and V_{ON} was carried out for both voltage polarities and different V_{max} values. Figure 3 reports the average and standard deviation values for R_{ON} and $|V_{ON}|$ as a function of $|V_{max}|$. It is observed that R_{ON} decreases as $|V_{max}|$ increases, while $|V_{ON}|$ increases with $|V_{max}|$. Notice that the experimental trends are quite similar regardless of the voltage polarity. This is the result of the self-balance mechanism mentioned above. Moreover, to assess whether the CRS behavior is symmetric or not, the relationship between R_{ON} and V_{ON} was investigated for both polarities (see Fig. 4). The obtained results indicate that these parameters are statistically correlated and strongly linked to V_{max} (see Fig. 3). The correlation between R_{ON} and V_{ON} for both polarities is described by the Pearson coefficient (ρ), giving values of 0.96 and 0.82, respectively. These values point out the almost symmetric behavior of the CRS curves (see Fig. 2 (c)). Random variations can be attributed again to the inherent cycle-to-cycle variability of the CF microstructure after each set and reset transition [27]. Notice that lower ρ values were experimentally

obtained for the V_{ON} plot compared to the R_{ON} plot, indicating that the effects of variability have a larger impact on the V_{ON} parameter. The corresponding Pearson correlation coefficients with their lineal fits are shown in Fig. 4.

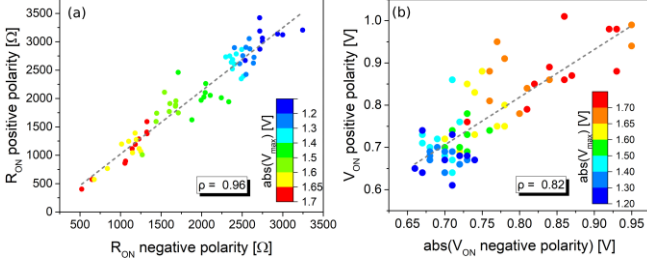


Fig. 4: (a) R_{ON} at positive voltage polarity as a function of R_{ON} at negative polarity, and (b) $|V_{ON}|$ at positive voltage polarity as a function of $|V_{ON}|$ at negative polarity for several $|V_{max}|$ values.

IV. DYNAMIC MEMDIODE MODEL FOR CRS

In this Section, the DMM compact model for CRS devices is described. This is different from the previously published quasi-static model (QMM), which is based on a time-independent hysteresis operator [28],[15]. The model considers two RS structures anti-serially connected forming a single three-terminal subcircuit. The third terminal is the central connection point. By assuming a three-terminal subcircuit, redundant components can be eliminated and the final LTSpice script simplified (see Appendix I). If the RS structures are identical, the model script can be further reduced. The conceptual approach followed for modeling the structure is that proposed by Prof. Chua for memristive devices, namely two coupled equations: one for the electron transport flowing through a filamentary-type conducting structure and a second equation representing the reversible movement of vacancies/ions within the dielectric layer caused by the application of the external electrical stimulus. The model corresponding to each RS structure is succinctly reviewed first and then the combined action discussed. A complete reference guide to the DMM model for an isolated device can be found elsewhere [29].

According to the DMM, the I - V characteristic of a RS structure is given by the transcendental equation:

$$I(V) = I_0(\lambda) \sinh\{\alpha(\lambda)[V - (R_C(\lambda) + R_{SB})I(V)]\} \quad (1)$$

where V is the voltage drop across its terminals, I_0 is the current amplitude factor, α the slope factor, and R_C is the constriction resistance (variable part of the resistance). The three λ -dependent parameters included in (1) change linearly from a minimum to a maximum according to the value of λ . For instance, $I_0(\lambda) = I_{min} + \lambda(I_{max} - I_{min})$, where I_{min} and I_{max} are model calibration parameters. $0 \leq \lambda \leq 1$ is the so-called memory state variable and it is used to control the transitions $HRS \leftrightarrow LRS$. R_{SB} is a fixed-resistance and is referred to as the snapback resistance. Its main purpose is to model the load line of the device and can be external, internal, or both. While I_0 fundamentally affects the magnitude of the current, the role of R_C in combination with R_{SB} in (1) is to linearize the exponential I - V curve (HRS) when the current reaches a high value (LRS). Since the DMM is a behavioral model, the $\sinh$ dependence in

(1) can represent different electron transport mechanisms, such as diode-like, tunneling, quantum point-contact conduction, as well as any other mechanism described by an exponential law. The memory state of the device, λ , is described by the balance-type differential equation:

$$\frac{d\lambda}{dt} = \frac{1 - \lambda}{\tau_S(\lambda, V_{CT})} - \frac{\lambda}{\tau_R(\lambda, V_{CT})} \quad (2)$$

where τ_S and τ_R are the characteristic set and reset times, respectively. According to the DMM model, these times are expressed as:

$$\tau_S(\lambda, V_{CT}) = \exp[-\eta_S(V_{CT} - V_S(\lambda))] \quad (3)$$

$$\tau_R(\lambda, V_{CT}) = \exp[-\eta_R \lambda^\gamma (V_{CT} - V_R)] \quad (4)$$

where $V_{CT} = V - I R_{SB}$ is the constriction voltage, $\eta_S > 0$ and $\eta_R > 0$ the transition rates, and $V_S > 0$ and $V_R < 0$ the set and reset voltages, respectively. Notice that both τ_S and τ_R depend on λ . In (3), λ generates a sudden collapse of τ_S by reducing V_S when the current reaches a given threshold value I_{SB} indicating the completion of the filamentary path and the triggering of the snapback process. This is followed by the local accumulation of defects which occurs at a fixed constriction voltage $V_{CT} = V_T$ called the transition voltage [16]. On the contrary, in (4), λ generates a relaxation of τ_R as the memory state drops so that a reduction of the current is achieved indicating the end of the snapforward process and the beginning of the progressive dissolution of the remainder filamentary path. The rate at which this dissolution process occurs is governed by the parameter γ . The snapback effect, as well as the vertical current increase associated with the progressive accumulation of defects occurring at positive biases, are illustrated in Figs. 5 (a) and (b). For negative biases, Fig. 5 illustrates the snapforward effect (abrupt current drop) and the progressive dissolution of the filament (current tail occurring at the highest biases).

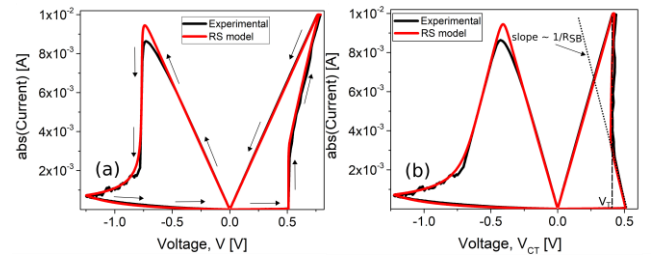


Fig. 5: Experimental and simulation results for a single TiN/Ti/HfO₂/W memristor exhibiting snapback and snapforward effects. (a) I - V curve as measured, (b) current vs the constriction voltage (V - IR) for the same memristor. R_{SB} is the snapback resistance and V_T is the transition voltage. Arrows in (a) indicate the voltage sweep direction for the RS phenomenon.

Remarkably, as illustrated in Fig. 6(a), (2) can be represented by a two-mesh equivalent circuit with behavioral current sources and a single capacitor. Since both RS devices are anti-serially connected to form the CRS, there is only one branch for the I - V curve and two independent instances of the memory circuit with complementary initial conditions $\lambda(t=0)=0$ (HRS)

and $\lambda(t=0)=1$ (LRS). These initial states correspond to the initial voltages across the capacitors in Fig. 6(a). Notice how the central contact is externally accessible (V_c) creating the three-terminal subcircuit depicted in Fig. 6(b). The name memdiode comes from the particular interpretation of (1) as two back-to-back connected diodes (see Fig. 6 (a)).

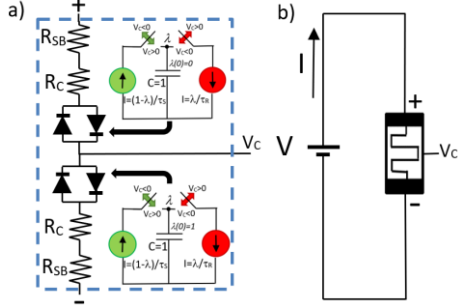


Fig. 6: (a) Schematics for the internal implementation of the CRS device. The green and red arrows indicate the set and reset process, respectively. $\lambda(t=0)$ is the initial memory state. (b) Three-terminal equivalent circuit model.

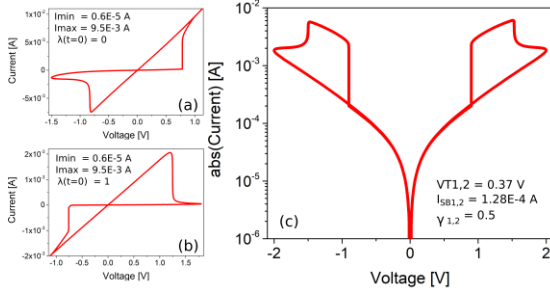


Fig. 7: (a), (b) Simulation results for two RS devices with digital set (abrupt) and digital/analog (abrupt/progressive) reset transitions. (c) Simulation result for the CRS devices corresponding to curves (a) and (b). Notice the abrupt OFF→ON transitions. The inset indicates the model parameter values.

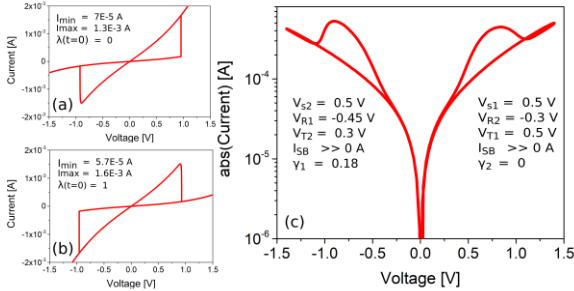


Fig. 8: (a), (b) Simulation results for two RS devices with no snapback effect (no reduction of the device voltage drop). (c) Simulation result for the CRS devices corresponding to curves (a) and (b). Notice the progressive OFF→ON transitions. The inset indicates the model parameter values.

One central feature of our proposal is the possibility of simulating digital (abrupt) or analog (progressive) OFF↔ON transitions in the CRS curve as experimentally observed. The difference between the two cases is a consequence of the kind of transition considered for the individual RS devices. If the snapback process is relevant, *i.e.* if the completion of the filament leads to a noticeable reduction of V_{CT} along the load

line as illustrated in Fig. 5 (b), the CRS OFF→ON transition is digital (see Fig. 7), otherwise the transition is analog (see Fig. 8). In this case, no reduction of V_{CT} is detected. This behavior is controlled by the threshold current value I_{SB} . Similarly, if the snapforward process is completely abrupt, the ON→OFF transition is digital (see Fig. 8), otherwise if it exhibits a deviation at the highest bias, the transition is a combination of digital and analog (see Fig. 7). This behavior is controlled by the reset parameter γ . In summary, our three-terminal subcircuit compact model can deal with any possible situation.

V. EXPERIMENTAL AND SIMULATION RESULTS

In this Section, we present experimental and simulation results obtained from our own structures as well as from a variety of devices reported in the literature. The original references are indicated in each figure's caption. This study is aimed at emphasizing the flexibility and accuracy of the three-terminal subcircuit approach described in Section IV. To begin with, Fig. 9 illustrates experimental and simulation results for our TiN/Ti/HfO₂/W-based CRS devices with different $|V_{max}|$ values. The curves illustrate mainly analog transitions. For the complete picture see Fig. 2 (c). In addition, Figs. 10(a) and (b) show how the model is able to capture digital and analog switchings of considerable complexity. The curves correspond to unstable loops obtained before reaching the stationary cycles (self-balance dynamics regime) shown in Fig. 2(c).

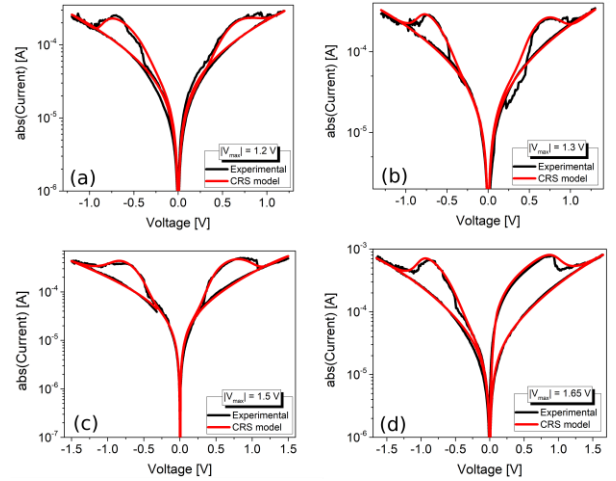


Fig. 9: Experimental and simulation results for our TiN/Ti/HfO₂/W-based CRS devices. V_{max} is the maximum voltage applied to the structure.

As aforementioned, the model was also tested for a wide variety of CRS structures reported in the literature. The results are shown in Figs. 11 and 12. For the sake of clarity, model parameters are reported in Appendix II. Figure 11 shows experimental and model results for HfO₂-based CRS devices similar to ours [16]. In this case, digital transitions are observed both for set and reset. Notice that the individual RS devices have dissimilar I - V curves. This additional information, which is not always available, is of utmost importance for obtaining the best fitting results.

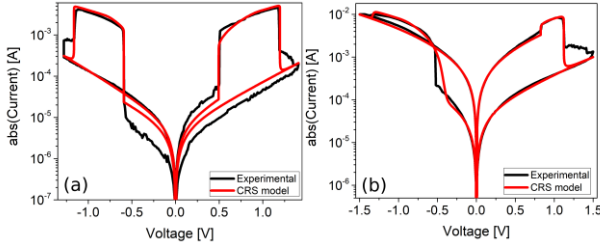


Fig. 10: Examples of experimental and simulated unstable cycles of our TiN/Ti/HfO₂/W-based CRS devices showing the capability of the proposed model to deal with such situations.

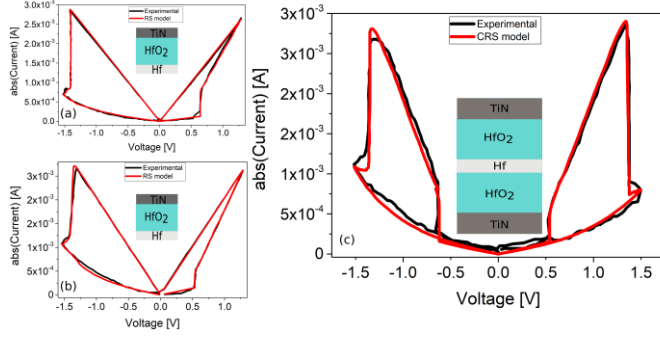


Fig. 11: Experimental and simulation results for HfO₂-based CRS devices. Data are extracted from [16].

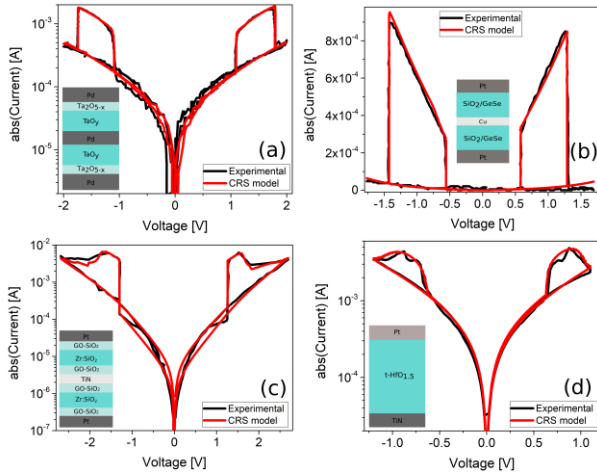


Fig. 12: Experimental results and simulations for different CRS devices. Data are extracted from the corresponding papers. (a) Tantalum oxide-based antiserially connected devices [30]; (b) GeSe-based devices [1]; (c) CRS with a two-sided graphene and Zr-SiO₂-based CRS structure[31]; (d) CRS for t-HfO_{1.5} device[32].

In other cases, such as the ones shown in Fig. 12, data are only available for the CRS I - V curve. Figure 13(a) illustrates abrupt and nearly symmetric CRS transitions for a combination of two bilayer Pd/Ta₂O_{5-x}/TaO_y/Pd structures [30]. Figure 12(b) shows abrupt CRS transitions obtained for two serially connected Pt/SiO₂/GeSe/Cu devices [1]. The I - V curve in Fig. 12(c) exhibits a combination of digital set and analog reset transitions obtained for a graphene/Zr:SiO₂-based CRS structure [31]. Figure 12(d) corresponds to a highly oxygen deficient tetragonal HfO_{1.5}-based CRS device. In this case, the I - V characteristic exhibits a pseudo-CRS behavior. Notice the absence of the central electrode [32].

VI. THREE-TERMINAL SUBCIRCUIT APPLICATION

In order to demonstrate the ability of the proposed three-terminal subcircuit compact model to perform in logic circuits, we present the simulation of the simplest material implication (IMPLY) logic gate [33]. As indicated in Fig. 13(a), four input combinations need to be considered. To perform this logic operation, a single CRS device connected as shown in Fig. 13 (b) is required. The IMPLY is performed under the following conditions: (i) $V_p < V_s$; (ii) $V_q > V_s$; (iii) $R_{OFF} > R > R_{ON}$. In our case, $R_{ON} = 385 \Omega$ and $R_{OFF} = 135 \text{ K}\Omega$. The resistor connected to the third terminal is $R = 10^3 \Omega$. In this logic (if p then q), the currents flowing through the CRS lateral terminals indicate the device logic state. Two different voltage pulses are applied to the terminals to induce a change of state. The states of P and Q are represented by the p and q logic variables. The '1' logic state corresponds to LRS and '0' to HRS. Figure 13 (c) shows the voltage pulses (read, write, read) and the current that flows through each terminal before and after the IMPLY operation. The red and blue curves correspond to the voltages and currents in the Q and P terminals, respectively. The time scale used in Fig. 13 (c) is only for illustrative purposes.

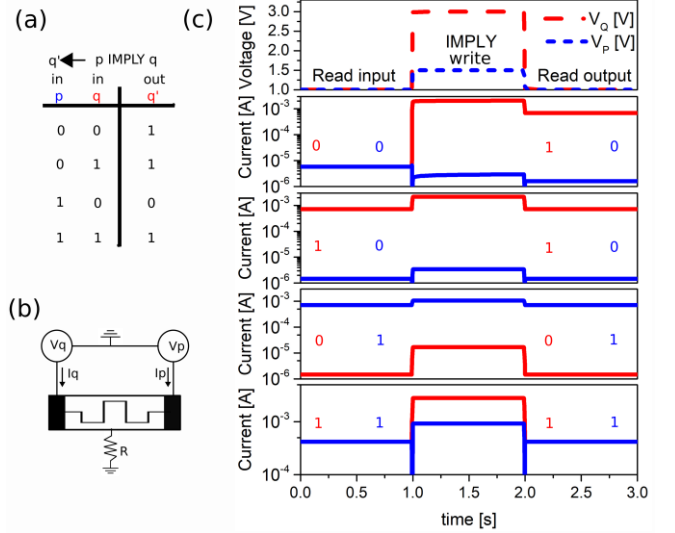


Fig. 13: Simulation of the IMPLY logic gate. (a) The truth table for the IMPLY operation (if p then q); (b) Connections of the CRS device; (c) The red and blue curves show the voltage and current values at the terminals Q and P, respectively. The absolute value of the current is plotted. The model parameters are H01,H02=0 or 1 depending on the truth table, $rsb1,2=300\Omega$, $etas1,2=20\text{V}^{-1}$, $vs1,2=3\text{V}$, $etar1,2=20\text{V}^{-1}$, $vr1,2=-0.5\text{V}$, $imax1,2=1\text{E}-2\text{A}$, $amax1,2=amin1,2=1\text{V}^{-1}$, $rcmax1,2=rcmin1,2=0.5\Omega$, $imin1,2=0.5\text{E}-5\text{A}$, $vt1,2=0.4\text{V}$, $isb1=isb2=0.2\text{E}-4\text{A}$, $gam1=gam2=0.3$, $RPP=1\text{E}10\Omega$. The subindexes 1 and 2 refer to each RS device in the CRS structure.

VII. CONCLUSIONS

In this work, HfO₂-based CRS devices intentionally fabricated with an accessible central terminal have been studied and modeled taking into account the presence of snapback and snapforward effects during the set and reset transitions. The experimental results reveal that the maximum voltage applied to the structures allows modulating the shape and width of the resistive windows following a self-balance approach. Moreover, the symmetric behavior of the CRS state transitions and the inherent cycle-to-cycle variability present in CRS

devices have been discussed. A three-terminal compact subcircuit model developed in LTSpice has been proposed to simulate the CRS behavior with abrupt or gradual current transitions thanks to the inclusion or exclusion of the snapback and snapforward effects. The model has been validated by comparing simulations with experimental measurements obtained from our devices and from a wide variety of devices with different oxide/electrode material combinations extracted from the literature, demonstrating its versatility, robustness, and accuracy. Finally, the ability of our model to perform logic circuits has been demonstrated by a successful simulation of the operation of the IMPLY logic gate.

APPENDIX I

Figure 14 shows the LTSpice script used for all the CRS simulations reported in this work. The parameters are: H0 is the initial memory state (0 for HRS, 1 for LRS); etas, vs, etar, and vr control the set and reset transitions. The characteristic parameters used to describe the LRS and HRS I - V curves are imax, amax, rcmax, and imin, amin, and rcmin. To describe the snapback and snapforward effects, the parameters vt, isb, and gam are used. Figure 15 illustrates: (a) the central potential and (b) the I - V curve corresponding to the script shown in Figure 14.

```
.subckt CRS + c -
X1 + c MEM H0=0 rsb=300 etas=20 etar=20 vs=3 vr=-0.5 imax=1e-2 imin=0.5E-5
+ amax=1.0 amin=1.0 rcmax=5 rcmin=5 vt=0.4 isb=0.2e-4 gam=0.3 rpp=1E10
X2 - c MEM H0=1 rsb=300 etas=20 etar=20 vs=3 vr=-0.5 imax=1e-2 imin=0.5E-5
+ amax=1.0 amin=1.0 rcmax=5 rcmin=5 vt=0.4 isb=0.2e-4 gam=0.3 rpp=1E10
.subckt MEM + -
BH 0 H I=if(V(+,-)>0,(1-V(H))/TS(V(A,-)), -V(H)/TR(V(A,-))) Rpar={rpp}
CH H 0 1 ic={H0}
RE + A {rsb}
RS A B R=K({rcmin},{rcmax})
BD B - I=K({imin},{imax})*sinh(K({amin},{amax})*V(B,-)) Rpar={rpp}
.func K(min,max)=min+(max-min)*limit(0,1,V(H))
.func TS(x)=exp(-(etas)*(x-if(I(BD)>{isb},{vt},{vs})))
.func TR(x)= exp({etar}*pow(limit(0,1,V(H)),{gam})*(x-{vr}))
.ends
.ends
```

Fig. 14: The LTSpice script described above corresponds to the three-terminal CRS subcircuit model proposed in this work. “+” and “-” are the extreme terminals while “c” is the central contact of the device.

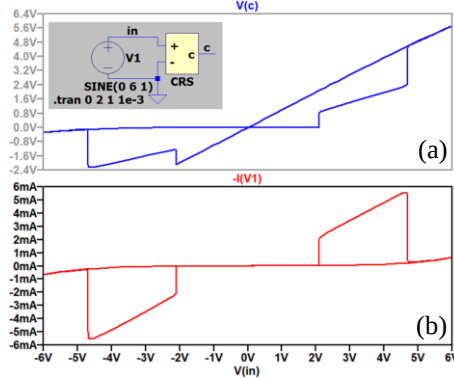


Fig. 15: (a) Typical simulation scheme and voltage at the central terminal (V_c) of the device. (b) Current-Voltage characteristic.

APPENDIX II

TABLE II
CRS MODEL PARAMETER VALUES

Fig	rsb (Ω)	etas (V^{-1})	etar (V^{-1})	vs (V)	vr (V)	imax (A)	imin (A)	amax (V^{-1})	amin (V^{-1})	rc (Ω)	vt (V)	isb (A)	gam
9 (a)	50	17	7	0.44	-0.44	4.50E-4	5.50E-5	2.4	2.4	5	0.44	-	0
	50	17	3.1	0.38	-0.35	1.00E-3	6.50E-5	2.6	2.7	4	0.35	-	0
9 (b)	50	20	11	0.4	-0.48	1.30E-4	7.00E-5	2.15	2.15	5	0.48	-	0.5
	50	20	3.1	0.5	-0.45	1.50E-3	5.70E-5	2.6	2.6	4	0.45	-	0
9 (c)	50	19	11	0.5	-0.45	1.30E-3	7.00E-5	2.34	2.34	5	0.5	-	0.18
	50	20	3.1	0.5	-0.3	1.60E-3	5.70E-5	2.85	2.85	4	0.3	-	0
9 (d)	50	15	11	0.01	-0.4	1.00E-3	5.00E-5	2.4	2.8	5	0.4	1.00E-4	0.6
	50	10	10	0.6	-0.6	1.00E-3	5.70E-5	2.6	2.68	4	0.45	-	0.7
10 (a)	0.1	100	100	1	-0.53	2.50E-3	1.20E-5	2.9	3.2	5	0.4	2.70E-5	0.5
	0.1	100	100	1	-0.65	2.50E-3	1.00E-5	2.4	2.7	5	0.4	2.35E-5	0.45
10 (b)	0.1	50	50	1	-0.6	6.00E-3	8.00E-4	2.4	3.7	5	0.4	3.30E-3	0.3
	0.1	50	50	0.4	-0.54	6.00E-3	1.00E-4	2.4	2.1	5	0.5	-	0.4
11 (c)	85	100	28	1	-0.37	3.90E-3	8.00E-5	1.8	1.8	5	0.35	1.58E-4	0.9
	85	100	45	1	-0.4	3.90E-3	8.00E-5	1.8	1.8	5	0.38	1.62E-4	0.9
12 (a)	50	100	100	2	-0.8	1.00E-3	9.00E-5	1.5	1.5	10	0.44	1.75E-5	0
	50	100	100	2	-0.8	1.00E-3	9.00E-5	1.5	1.5	10	0.44	1.75E-5	0
12 (b)	58	60	40	0.75	-0.6	6.60E-4	6.00E-6	1.8	1.8	3.5	0.24	7.35E-6	0
	68	70	80	0.6	-0.58	6.90E-4	4.80E-6	1.8	1.8	2.7	0.28	5.80E-6	0
12 (c)	1	50	35	2	-0.8	8.00E-4	5.70E-8	3.3	3.2	10	0.1	2.70E-4	0.8
	1	50	50	5	-0.8	8.00E-4	5.00E-8	3.3	3.3	10	0.1	2.50E-4	0.8
12 (d)	10	10	6	1	-0.4	8.00E-3	6.60E-4	2.1	2.5	1	0.35	1.20E-3	0.22
	8	8	10	1	-0.44	8.70E-3	6.00E-4	2.1	2.5	1	0.5	1.25E-3	0.15

CRS model parameters for the indicated figures. The parameter r_c corresponds to $rcmax = rcmin$ in the LTSpice script. Grey rows correspond to a single device with an initial memory state, $H_0 = 0$, and white rows correspond to $H_0 = 1$. When the parameter isb is activated, V_s does not play role in the simulation and must be chosen high enough.

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