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Exploiting the KPFM capabilities to analyze at the nanoscale the impact of electrical stresses on OTFTs properties

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Abstract— Two different Kelvin Probe Force Microscopy (KPFM) measurement configurations have been combined to evaluate at the nanoscale the effects of an electrical stress on Organic Thin Film Transistors (OTFTs) properties. As an example, Channel Hot Carrier (CHC) degradation has been induced to provoke some damage in the studied devices. The results show that the use of the two KPFM configurations, together with their nanoscale resolution, provides additional information about the damage in the different regions/materials of the devices, allowing to correlate device level characteristics with the nanoscale material properties.

I. INTRODUCTION

OTFTs are an interesting and promising alternative to Si-based technologies [1] in different applications such as wearable electronics, flexible devices and circuits or low-cost sensors. This diversity of applications is possible thanks to the good features they present, such as low fabrication complexity, mechanical flexibility, low-cost and/or higher compatibility with a wide range of substrates. Due to these good characteristics, many studies in the literature are focused on the analysis of the materials properties [2 - 4] or device performance [5] and have proposed electrical models for describing their behavior [6], where the electrical properties of the organic material play a very important role. In spite of that, relatively few studies have been performed on the reliability of OTFTs [2], which is one of the key points in order to make this technology viable for the market. The electrical properties of the commonly used organic polymers are very sensitive to the environment conditions (temperature and humidity), what clearly affects the reliability of these devices. Moreover, the usual large operating conditions of the OTFTs can be also critical, due to the high voltages required (in the 10-30V range). In this sense, the effect of the electrical stresses on the organic polymer and the device performance must be analyzed in detail. Moreover, the aging mechanisms activated in the OTFTs during the stresses should be studied and compared with those in conventional CMOS technologies to understand the role of the organic polymer in the device reliability. This task could be further complicated because of the large number of semiconductor polymers available in the market, so different strategies are necessary to assess the origin of the possible reliability issues.

In this regard, measurement techniques with nanoscale resolution, as Conductive Atomic Force Microscope (CAFM) and Kelvin Probe Force Microscope (KPFM) have been shown to be very powerful to get topographical and electrical information at the nanoscale of materials and devices. They can provide additional information about the causes of their degradation, beyond the electrical I-V curves obtained at device level. When the AFM tip is in contact with a given material, it plays the role of the top electrode, with a contact area that corresponds to the contact region between the tip and the sample. Since this area can be very small (~100 nm², on dielectrics [7]), the technique allows the nanoscale electrical characterization with a resolution of ~10 nm. CAFM and KPFM have been thoroughly used for the nanoscale electrical characterization of different materials, as graphene [8 - 10], gate dielectrics [11 - 17] or organic materials [18]. For example, in [19], KPFM has been used to study the effect of a Bias Temperature Instabilities (BTI) stress on OTFTs, obtaining information about the charge density at the polymer/dielectric interface after the electrical stress. In this work, we extend the use of this technique to preliminary analyze the impact of an electrical stress (in our case, a Channel Hot Carrier stress applied at device level) in both, the polymer layer (channel) and the gate stack of the OTFT (polymer and dielectric), at the nanoscale. With this purpose, two different KPFM measurement configurations have been used to obtain complementary information, which would allow to correlate device level and nanoscale characteristics.

II. EXPERIMENTAL DETAILS

The OTFTs were fabricated on a heavily doped silicon wafer (which plays the role of the gate electrode) with a 300 nm-thick thermally grown SiO_2 dielectric layer on top (Fig. 1a). The substrate was cleaned sequentially with acetone, isopropyl alcohol and deionized water in an ultrasonic bath, followed by blowing dry with nitrogen gas. On top of the gate dielectric, Au source-drain electrodes (thickness of 30 nm, Fig. 1a and 1b) were defined by photolithography to get a channel length (L) of 20 μ m and channel width (W) of 15 mm. The organic channel was obtained by means a procedure based on solution processed organic semiconductors. A semiconductor solution of DPP-DTT in 1,2-dichlorobenzene (10 mg mL-1) was then spin coated and annealed at 80 °C for 10 min under nitrogen environment, resulting in an 80 nm thick P-type organic semiconductor. A cross-section of the resulting device can be seen in Figure 1a. It is worth noting that the surface of the device is totally covered by the DPP-DTT polymer, but the height profile mirrors the profile of the defined Au electrodes that are buried under the polymer layer. Fig 1c correspond to a topographical image and profile along the line of an OTF channel between two Au electrodes.

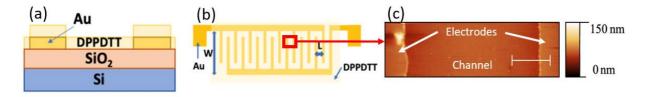


Fig. 1. (a) Cross-section and (b) top view of the OTFT under study. (c) shows the topographical image of the resulting DDP-DTT layer on two Au electrodes in the area inside the red box of (b). The scale bar is $5\mu m$.

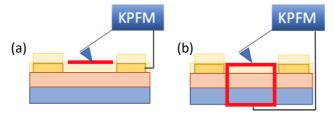


Fig. 2. KPFM configurations corresponding to the (a) lateral KPFM (L-KPFM) and (b) vertical KPFM (V-KPFM). The red lines indicate the area (for L-KPFM) or volume (for V-KPFM) analyzed.

Before and after the electrical stress, I-V curves at device level (i.e. I_G-V_G and, I_D-V_G) and the nanoscale properties of the channel and gate stack were measured with a Semiconductor Parameter Analyzer (SPA) and with a KPFM, respectively. The I-V curves were measured with the Keithley 4200 SPA, which was also used to apply the electrical stress. The stress was a -30V constant voltage applied at the Gate and Drain Terminals during 6000s. The nanoscale properties of the OTFT were investigated with a Nano-Observer KPFM from Concept Scientific Instruments, with which it is possible to measure, simultaneously to the topography, the Contact Potential Difference (CPD) between the tip and the sample. In our case, KPFM images have been obtained in air, using Si tips from AppNano. Since the CPD data correspond to the difference between the Work Functions (WF) of the tip and the sample, assuming a constant value of the tip WF during the experiment, the measured CPD variations are related to the WF fluctuations of the sample. Therefore, the CPD image provides information on the local value of the WF of the structure under analysis. However, since the tip WF is not known and absolute values of WF are also very sensitive to ambient conditions and can change between different measurements, only WF relative variations in a given image will be considered. The setup allows bimodal single pass Amplitude Modulation KPFM (AM-KPFM) measurements [20]. Fig. 2a and b show the two KPFM measurement configurations used in this work. In the first one (Fig. 2a), the KPFM measurements are performed between the Organic channel and the electrodes (called from now on Lateral KPFM configuration, L-KPFM), as the ground of the microscope is connected to one of the metal electrodes. In the second one (Fig. 2b), ground is connected to the gate electrode so, the measurements are performed between the organic channel and the substrate (called from now on Vertical KPFM, V-KPFM). Therefore, each configuration will provide details of the properties of different layers/stacks of the device.

III. RESULTS

First, we have investigated the electrical properties of the OTFTs before the application of the electrical stress. A pristine OTFT, which will be considered as reference, has been analyzed at device level and at the nanoscale with the L-KPFM and V-KPFM configurations. Fig. 3 shows, for the L-KPFM configuration, the topography (a) and CPD (b) images of a region overlapping the channel and one of the electrodes, and Fig. 3c profiles along the lines drawn in the images. Fig. 3d-f correspond to the topography and CPD maps and the corresponding profiles (Fig. 3f), for the V-KPFM case.

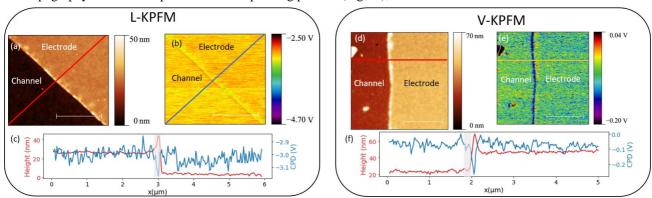


Figure 3. (a and d) Topographical and (b and e) corresponding KPFM images of a region that overlaps the channel and electrode areas, for the L-KPFM (a and b) and V-KPFM (d and e) configuration. A profile along the lines on the images in the topography/CPD maps is shown in (c) and (f). The CPD is approx. constant over the two regions except at the step between the channel and electrode (grey area in the profiles), related to measurement artifacts. The scale bar is 2 um.

In both cases, in the topography image (and its corresponding profile), a step is detected between the electrode (highest region) and channel (lowest region). This step is detected in the V-KPFM image as an artifact due to the crosstalk effect, in which a sudden change in the topography may induce an instantaneous change in the CPD [21]. This phenomenon can be seen at the center of the V-KPFM image (Fig. 3.f). However, leaving aside this artifact, the images and the profiles indicate no relevant differences between the CPDs of both regions (channel and electrode), as expected, since the tip is always contacting the asdeposited organic material and the devices have not been subjected to any electrical stress. The device electrical characteristics measured with the SPA is shown in Fig. 4b. There, the black curve corresponds to the I_D - V_G curve measured before the stress, which will be the reference to which the curves measured after the stress (red dots) will be compared.

After the pre-stress characterization, a CHC stress has been applied to the OTFT with the SPA. Fig. 4a shows a schematic of the device biasing. While the source was grounded, a voltage of -30V was applied to the Drain and Back Gate of the device. Note that, with this configuration, positive carriers flow from Source to Drain, getting the maximum energy near the Drain and, therefore, damaging that region. On the other hand, since $V_D=V_G$ at the Drain area, vertical electric fields are negligible near the Drain and, therefore, NBTI damage (if any), should appear near the Source region only.

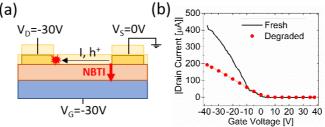


Fig. 4. (a) Scheme of the connections and biasing for the CHC stress (VD=-30V, VG=-30V and VS=0V for 6000s). (b) I-V curves of the OTFT before (black) and after (red) the CHC stress.

After the stress, the I_D - V_G characteristics has been measured (red curve in Fig. 4b). A large current reduction in the I_D - V_G characteristics is observed after the CHC stress, caused by a strong mobility reduction with negligible threshold voltage (V_{TH}) variation. Since BTI degradation is mostly related to V_{TH} variations and CHC degradation to mobility reductions, these results suggest that CHC degradation drives the device degradation while BTI seems to be negligible [22].

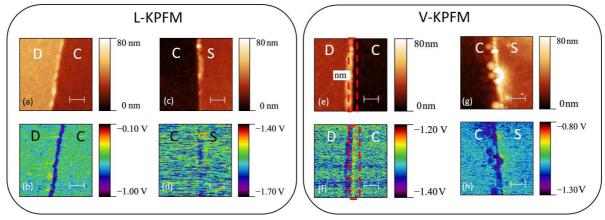


Fig. 5. L-KPFM (a/b/c/d) and V-KPFM (e/f/g/h) images of the channel/drain (C/D) and channel/source (C/S) overlapping regions. The scale bar is 0.5 μm. In general, the changes in CPD values match the changes in topography, except in the drain region when measured using the V-KPFM configuration (e/f). In this case, an additional CPD signal appears along the drain electrode, that is enclosed by the red box.

To investigate the effects of the stress on the properties of the different regions/materials of the device, L-KPFM and V-KPFM measurements were performed along the channel (close to Source and Drain electrodes). Fig. 5 shows L-KPFM (a-d) and V-KPFM (e-h) images of the channel/drain (C/D) and channel/source (C/S) overlapping regions. The top/down images correspond to topography/CPD maps. In the Source/Channel region (Fig. 5c/d/g/h), negligible differences are observed in the CPD image between the electrode and channel region, independently of the measurement mode, as was also observed in the fresh device (Fig. 3). Only some observable differences in the CPD values are measured in Fig. 5h, which can be related to measurement artifacts associated to the topographical changes observed in Fig. 5g. Although they could be related to some kind of contamination of the sample, their origin is not clear and further studies are required to investigate their origin. In any case, the results suggest that the stress has not induced visible NBTI changes neither in the channel nor in the gate stack close to the Source. Since NBTI effects (see Fig. 4a) (if any) in this CHC stress are expected to be located at that region, extending into the channel region, the results suggest that NBTI has little impact in this kind of devices, as also pointed out by the device level characterization (Fig. 4). In the Drain/Channel region, the CPD L-KPFM image (Fig. 5d) did not show remarkable changes in the CPD between the drain electrode and channel regions, being similar to that measured in pristine OTFTs (Fig 3b). This suggests that there is a negligible damage on the surface of the OTFTs channel. However, the V-KPFM images (Fig. 5e/f) suggest the presence of an additional difference in the KPFM signal, not previously observed, close to the step. This difference, which is the main modification of the CPD observed, can be seen as a line that follows the Drain/Channel interface (enclosed in a red box in Fig. 5f), ~90 nm wide into the channel region and with an increase of the CPD of ~60mV. This CPD signal is not related to any topographical feature near the step between the Drain/Channel interface. As it is observed in the channel region and with L-KPFM no damage is observed at the surface, this could be indicative of local damage at the dielectric and/or at the gate oxide/channel interface. These results, though preliminary, are compatible with the CHC degradation observed at device level (Fig. 4b), whose damage is expected to be concentrated close to the Drain.

IV. CONCLUSIONS

In this work, two KPFM measurement configurations have been combined with device level tests to evaluate the impact of an electrical stress (in this case, a CHC stress) on OTFTs electrical properties. The results show that the use of the L-KPFM and V-KPFM configuration can provide complementary information to device level tests on the nanoscale damage of the different materials/regions of the device. Because of the particular structure of these devices, destructive sample preparation is not required, so that measurement-stress-measurement sequences can alternate device level and nanoscale tests, allowing a time-dependent analysis of the device properties at both scales.

V. ACKNOWLEDGEMENT

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REFERENCES

- C. Reese, M. Roberts, M. Ling, Z. Bao, "Organic thin film transistors", Materials Today, vol. 7, p. 20-27 (2004). DOI: 10.1016/S1369-7021(04)00398-0
 S. H. Ko, H. Pan, C. P. Grigoropoulos, C. K. Luscombe, J. M. J. Fréchet, and D. Poulikakos, "All-inkjet-printed flexible electronics fabrication on a polymer substrate by low-temperature high-resolution selective laser sintering of metal nanoparticles," Nanotechnology, vol. 18, no. 34, p. 345202, (2007). DOI: 10.1088/0957-4484/18/34/345202.
- [3] H. Jeong, S. Baek, S. Han, H. Jang, S. H. Kim, and H. S. Lee, "Novel Eco-Friendly Starch Paper for Use in Flexible, Transparent, and Disposable Organic Electronics," Adv. Funct. Mater., vol. 28, no. 3, p. 1704433, (2018). DOI: 10.1002/adfm.201704433.
- [4] N. A. Azarova, J. W. Owen, C. A. McLellan, M. A. Grimminger, E. K. Chapman, J. E. Anthony and O. D. Jurchescu, "Fabrication of organic thin-film transistors by spray-deposition for low-cost, large-area electronics," Org. Electron. physics, Mater. Appl., vol. 11, no. 12, pp. 1960–1965, (2010). DOI: 10.1016/j.orgel.2010.09.008.
- [5] A. Arnal, A. Crespo-Yepes, E. Ramon, Ll. Terés, R. Rodríguez and M. Nafría, "DC characterization and fast small-signal parameter extraction of organic thin film transistors with different geometries," IEEE Electron Device Letters, vol. 41, no. 10, pp. 1512-1515, (2020). DOI: 10.1109/LED.2020.3021236.
- [6] J. S. Chang, A. F. Facchetti, R. Reuss, S. Member, A. F. Facchetti, and R. Reuss, "A Circuits and Systems Perspective of Organic/Printed Electronics: Review, Challenges, and Contemporary and Emerging Design Approaches," IEEE J. Emerg. Sel. Top. Circuits Syst., vol. 7, no. 1, pp. 7–26, (2017). DOI: 10.1109/JETCAS.2017.2673863.
- [7] M. Porti, M. Nafría, X. Aymerich, A. Olbrich and B. Ebersberger, "Electrical characterization of stressed and broken down SiO2 films at a nanometer scale using a conductive atomic force microscope", J. Appl. Phys., vol. 91, no. 4, pp. 2071-2079, (2002). DOI: https://doi.org/10.1063/1.1430542.
- [8] F. Giannazzo, I. Deretzis, A. La Magna, F. Roccaforte and R. Yakimova, "Electronic transport at monolayer-bilayer junctions in epitaxial graphene on SiC", Phys. Rev. B, vol. 86, art. 235422, (2012). DOI: 10.1103/PhysRevB.86.235422.
- [9] R. Kumar, D. Varandani, and B. R. Mehta, "Nanoscale interface formation and charge transfer in graphene/silicon Schottky junctions; KPFM and CAFM studies," Carbon, vol. 98, pp. 41–49, (2016). DOI: https://doi.org/10.1016/j.carbon.2015.10.075.
- [10] D.-H. Park, Y. J. Cho, J.-H. Lee, I. Choi, S.H. Jhang and H.-J. Chung, "The evolution of surface cleanness and electronic properties of graphene field-effect transistors during mechanical cleaning with atomic force microscopy", Nanotechnology, vol. 30, Art. No. 394003, (2019). DOI: https://doi.org/10.1088/1361-6528/ab2cf6.
- [11] M. Porti, M. Nafría, M. C. Blum, X. Aymerich and S. Sadewasser, "Atomic force microscope topographical artifacts after the dielectric breakdown of ultrathin SiO2 films," Surface Sci., vol. 532–535, pp. 727–731, (2003). DOI: 10.1016/S0039-6028(03)00150-X
- [12] M. Lanza, M. Porti, M. Nafria, X. Aymerich, G. Benstetter, E. Lodermeier, H. Ranzinger, G. Jaschke, S. Teichert, L. Wilde, P. Michalowski, "Crystallization and silicon diffusion nanoscale effects on the electrical properties of Al2O3 based devices", Microelectronic Engineering, vol. 86, pp. 1921-1924, (2009). DOI: 10.1016/j.mee.2009.03.020
- [13] V. Yanev, M. Rommel, M. Lemberger, S. Petersen, B. Amon, T. Erlbacher, A.J. Bauer, H. Ryssel, A. Paskaleva, W. Weinreich, C. Fachmann, J. Heitmann and U. Schroeder, "Tunneling atomic-force microscopy as a highly sensitive mapping tool for the characterization of film morphology in thin high-k dielectrics," Appl. Phys. Lett., vol. 92, Art. No. 252910, (2008). DOI: https://doi.org/10.1063/1.2953068
- [14] Y. L. Wu, J. J. Lin, B. T. Chen, C. Y. Huang, "Position-dependent nanoscale breakdown characteristics of thin silicon dioxide film subjected to mechanical strain," IEEE Trans. Device Mater. Rel., vol. 12, no. 1, pp. 158–165, (2012). DOI: 10.1109/TDMR.2011.2179804
- [15] K. Shubhakar, K.L. Pey, N. Raghaban, S.S. Kushvaha, M. Bosman, Z. Wang and S.J. O'Shea, "Study of preferential localized degradation and breakdown of HfO2 /SiOx dielectric stacks at grain boundary sites of polycrystalline HfO2 dielectrics," Microelectron. Eng., vol. 109, pp. 364–369, (2013). DOI: https://doi.org/10.1016/j.mee.2013.03.021
- [16] K. Murakami, M. Rommel, B. Hudec, A. Rosová, K. Hušeková, E. Dobročka, R. Rammula, A. Kasikov, J.H. Han, W. Lee, S.J. Song, A. Paskaleva, A.J. Bauer, L. Frey, K. Fröhlich, J. Aarik and C.S. Hwang, "Nanoscale characterization of TiO2 films grown by atomic layer deposition on RuO2 electrodes", ACS Appl.Mater. Interfaces, vol. 6, no. 4, pp. 2486–2492, (2014). DOI: 10.1021/am4049139
- [17] S. Claramunt, Q. Wu, M. Maestro, M. Porti, M.B. Gonzalez, J. Martín-Martinez, F. Campabadal, M. Nafria, "Non-homogeneous conduction of conductive filaments in Ni/Hf02/Si resistive switching structures observed with CAFM", Microelectron. Eng., vol. 147, pp. 335-338, (2015). DOI: https://doi.org/10.1016/j.mee.2015.04.112
- [18] T. Cramer, L. Travaglini, S. Lai, L. Patruno, S. de Miranda, A. Bonfiglio, P. Cosseddu and B. Fraboni, "Direct imaging of defect formation in strained organic flexible electronics by Scanning Kelvin Probe Microscopy", Sci. Rep., vol. 6, Art. No. 38203, (2016). DOI: https://doi.org/10.1038/srep38203
- [19] L. Bürgi, T. Richards, M. Chiesa, R. H. Friend and H. Sirringhaus., "A microscopic view of charge transport in polymer transistors", Synthetic Metals, vol. 146, issue 3, p. 297-309, (2004). DOI: https://doi.org/10.1016/j.synthmet.2004.08.009
- [20] A. Ruiz, N. Seoane, S. Claramunt, A. Garcia-Loureiro, M. Porti, C. Couso, J. Martin-Martinez and M. Nafria, "Workfunction fluctuations in polycrystalline TiN observed with KPFM and their impact on MOSFETs variability," Appl. Phys. Lett. 114, 093502, (2019). DOI: https://doi.org/10.1063/1.5090855.
- [21] S. Barbet, M. Popoff, H. Diesinger, D. Deresmes, D. Théron, and T. Mélin, "Cross-talk artefacts in Kelvin probe force microscopy imaging: A comprehensive study," J. Appl. Phys. 115(14), 144313, (2014). DOI: https://doi.org/10.1063/1.4870710
- [22] C-L. Fan, T-H. Yang, C-Y. Chiang, "Performance Degradation of Pentacene-Based Organic Thin-Film Transistors Under Positive Drain Bias Stress in the Atmosphere," IEEE Electron Device Letters, vol. 31, No. 8, p. 887-889, (2010). DOI: 10.1109/LED.2010.2051212