A 1024-Channel 10-bit 36-μW/ch CMOS ROIC for Multiplexed GFET-Only Sensor Arrays in Brain Mapping

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***Abstract*—This paper presents a 1024-channel neural read-out integrated circuit (ROIC) for solution-gated GFET sensing probes in massive μECoG brain mapping. The proposed time-domain multiplexing of GFET-only arrays enables low-cost and scalable hybrid headstages. Low-power CMOS circuits are presented for the GFET analog frontend, including a CDS mechanism to improve preamplifier noise figures and 10-bit 10-kS/s A/D conversion. The 1024-channel ROIC has been fabricated in a standard 1.8-V 0.18-μm CMOS technology with 0.012 mm^2 and 36 μW per channel. An automated methodology for the in-situ calibration of each GFET sensor is also proposed. Experimental ROIC tests are reported using a custom FPGA-based μECoG headstage with 16×32 and 32×32 GFET probes in saline solution and agar substrate. Compared to state-of-art neural ROICs, this work achieves the largest scalability in hybrid platforms and it allows the recording of infra-slow neural signals.**

***Index Terms*—Integrated circuits, ROIC, neural recording, μECoG, GFET, CMOS, TDM, CDS, ADC, headstage**

I. Introduction

NEUROSCIENTISTS are demanding large-scale recording systems for deciphering the fundamental mechanisms and processes that take place in human brain and whose knowledge is critical to develop more effective therapies for neurological injuries [1], treatment-resistant disorders [2] and neurodegenerative diseases [3]. One of the key enabling technologies that can improve the spatiotemporal resolution of these brain interfaces are the CMOS read-out integrated circuits (ROICs) specifically conceived for neural mapping. Their research interest is evident given the number of neural ROICs published in literature during the last fifteen years [4]–[78].

In general, the morphology of neural ROICs can be classified according to the three major applications illustrated in Fig. 1(a): high-density arrays for cell culture [4]–[19], penetrating shanks for intracortical recording [20]–[45] and conformal probes for micro-electrocorticography (μECoG) [46]–[78]. Electrophysiological signals to be read out in each recording site may contain low-frequency (i.e. 1 Hz to 1 kHz) local field potentials (LFPs) as well as high-frequency (i.e. 1 kHz to 10 kHz) single-unit active potential spikes, depending on the particular array density, with practical dynamic range values around 10 bit and full-scale amplitudes in the mV-range [79]. In most cases, recording sites are built from passive microelectrode arrays (MEAs) for either cell culture [6], intracortical recording [27] or μECoG [80]. However, active sensors based on solution-gated graphene field-effect transistors (GFETs) are opening new possibilities, like early amplification and multiplexing at array level [81], improved electrochemical stability in chronic implants with very low-rate drifts [82], low-impedance sensor-to-circuit interconnectivity that tends to mitigate signal loss, and DC coupling that can unlock the infra-slow (i.e. below 0.1 Hz) neural signals [83]. All these advantages are at the cost of extra power consumption in the sensing array and a challenging sensor downscaling.

The required connectivity from the recording sites of the sensing array to the analog frontend (AFE) circuits of the ROIC can follow

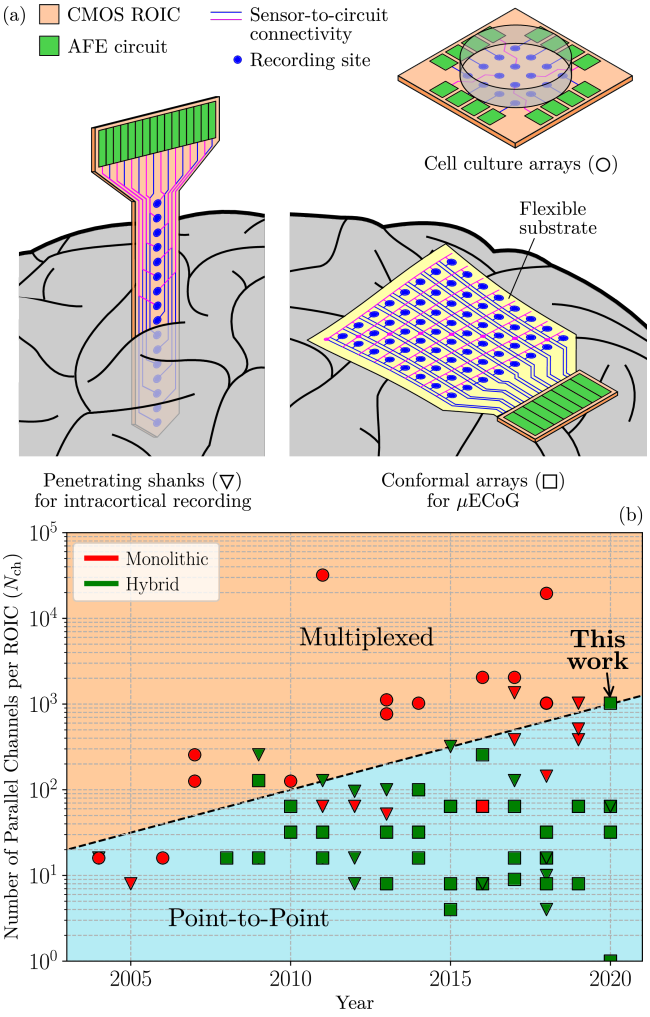

Figure 1. Neural ROIC device types (a) and state-of-art survey [4]–[78] according to ROIC application, sensor-to-circuit architecture (point-to-point vs. multiplexed) and CMOS integration (monolithic vs. hybrid) (b). Dashed line shows overall trend on scalability of single-ROIC channel count.

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dedicated point-to-point [19], [32]–[45], [49]–[78] or time-domain multiplexing [4]–[18], [20]–[31], [46]–[48] schemes. In terms of integration, monolithic solutions [4]–[18], [24]–[31], [44], [45], [48] build the sensing array in the same chip substrate as the read-out circuits, typically by CMOS post-processing techniques, while hybrid devices [19]–[23], [32]–[43], [46], [47], [49]–[78] combine separated technologies for each part through advanced packaging.

Scalability of such brain mapping systems is driven by two main vectors: large array sensing area and high spatial density of recording sites. From the ROIC viewpoint, both vectors tend to converge into the same figure of merit that is the total number of parallel read-out channels per chip (N_{ch}). In this sense, the state-of-art survey of Fig. 1(b) returns a sustained trending of two-fold increase in N_{ch} every three years. Classically, monolithic CMOS solutions have been employed to approach scalability, as it can be noticed by the red markers dominating the upper bounds of Fig. 1(b). Indeed, if the sensing array is integrated in the ROIC itself, then the number of one-to-one connections between each recording site and the corresponding AFE circuit can be easily scaled up while preserving analog signal integrity. Furthermore, this integration scheme allows to shift channel multiplexing higher in the circuit hierarchy (e.g. dedicated AFEs sharing a common A/D data converter). Unfortunately, monolithic solutions usually involve expensive CMOS post-processing steps, like ROIC micromechanization in penetrating shanks, and they are definitely not suitable for those brain mapping applications requiring either large sensing areas or conformable flexible arrays, as in μECoG. Hybrid devices can mix optimum technologies for the sensing array and ROIC parts, but they still have to face the packaging limitations in case of non-multiplexed sensor-to-circuit connectivity.

This work presents a large-scale neural ROIC architecture for solution-gated GFET sensing arrays in massive μECoG brain mapping. The proposed array multiplexing enables low-cost scalable hybrid integration and its CMOS circuit design compensates the effects of array scaling on noise performance while maintaining low-power operation. Following this architecture, 1024 simultaneous channels are fit in a single chip to achieve the largest scalability in hybrid neural ROICs, as highlighted in Fig. 1(b). Furthermore, the resulting system is also capable of recording infra-slow neural signals. The rest of the paper is organized as follows: Section II presents the solution-gated GFET arrays for brain mapping, while their time-domain multiplexing is proposed in Section III; the modular 1024-channel ROIC architecture is introduced in Section IV; the low-power CMOS row circuits for noise cancellation and A/D conversion are presented in Sections V and VI, respectively; the 1024-channel ROIC fabricated in 1.8-V 0.18-μm CMOS technology is described in Section VII; Section VIII explains the automated system calibration methodology with experimental examples, while Section IX compiles the electrical characterization results; finally, conclusions are summarized in Section X. Pre-Silicon design information of this ROIC has been presented by these authors in [84].

II. Neural Sensing with Solution-Gated GFET Arrays

Solution-gated GFETs as shown in Fig. 2(a) are effective transducers of neural signals [85] and a promising building block for large-scale neural probes due to their sensitivity [82], [86], stability in aqueous environments [82] and performance in multiplexed operation [81], [87]. The good sensitivity of solution-gated GFETs stems from the high electrical mobility of charge carriers in graphene and the high capacitance at the graphene-electrolyte interface [88]. These two factors lead to a remarkable transconductance (G_{m}), which is reflected in the transfer characteristics of Fig. 2(b), and therefore to a strong modulation of the graphene conductance by electrical potentials in the brain. In order to polarize the solution-gated GFETs

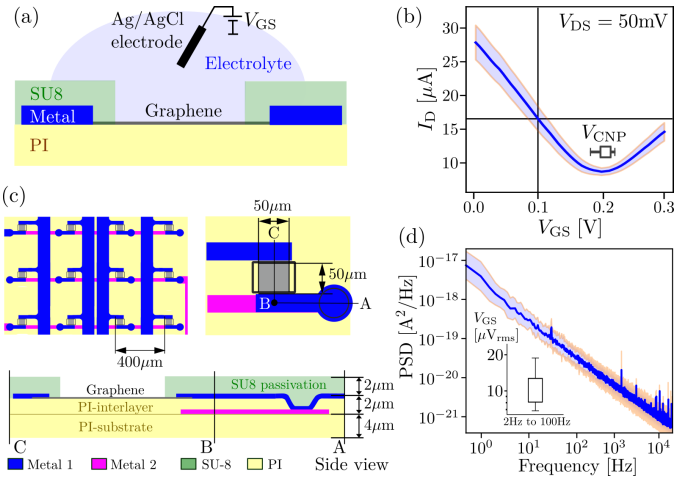

Figure 2. Solution-gated GFET sensor cross section (a), device electrical transfer curve (b), array layout (c) and noise spectral profile (d). Statistical data obtained from 20 samples.

in a regime of maximal sensitivity, a controlled overpotential can be applied between the graphene sensors and a stable reference electrodes in the aqueous environment, such as Ag/AgCl in Fig. 2(a), to shift the Fermi level in the graphene channel. The potential at which the Fermi energy is closest, on average, to the Dirac point of graphene is referred to as the charge neutrality point (CNP) of Fig. 2(b).

Graphene active sensors are three terminal devices and as such can be arranged in a column/row addressable array following Fig. 2(c). Selective biasing of the column interconnections can be used to multiplex the GFET signals detected at the rows. Recent works have demonstrated the good sensitivity and promising scalability of GFET neural probes multiplexed in the time-domain [81] as well as in the frequency-domain [46], [87]. The ROIC presented in this work allows to upscale the solution-gated GFET arrays multiplexed in the time-domain to 1024 channels while providing a compact headstage for in-vivo electrophysiological recordings. Another important aspect of solution-gated GFETs is their sensitivity in a wide frequency band. The electrical noise in these devices is dominated by their flicker noise, originating in trapping-detrapping events [89] up to very high frequencies beyond the bandwidth of neural activity, as shown in Fig. 2(d). While the absolute noise is above the levels of micro-electrode technologies, solution-gated GFETs still show a high sensitivity compared to alternative multiplexed active sensors. The state-of-the-art multiplexed μECoG arrays is currently defined by [90], in which the active sensors present a root mean square (RMS) noise of 58 μV in the 2Hz–100Hz band for 195×270 μm^2 devices. As shown in Fig. 2(d), the median RMS noise in our case is lower for the same frequency band and for a smaller area of 50×50 μm^2.

In addition to these noise characteristics, solution-gated GFETs present a constant frequency response for clean graphene-electrolyte interfaces [83], [91]. In contrast to microelectrodes, traditionally used in electrophysiology, graphene active sensors are fully DC coupled devices. The transfer characteristics of these sensors represent their stationary response, and therefore any change in the DC potential at the gate is ideally transduced into a DC current shift, which is reflected into a theoretically flat frequency response down to arbitrarily low frequencies [83], [91]. In the application of graphene active sensors in-vivo, the overpotential between graphene and the reference electrode may fluctuate due to electrochemical changes in the reference electrode or the graphene channel. However, due to

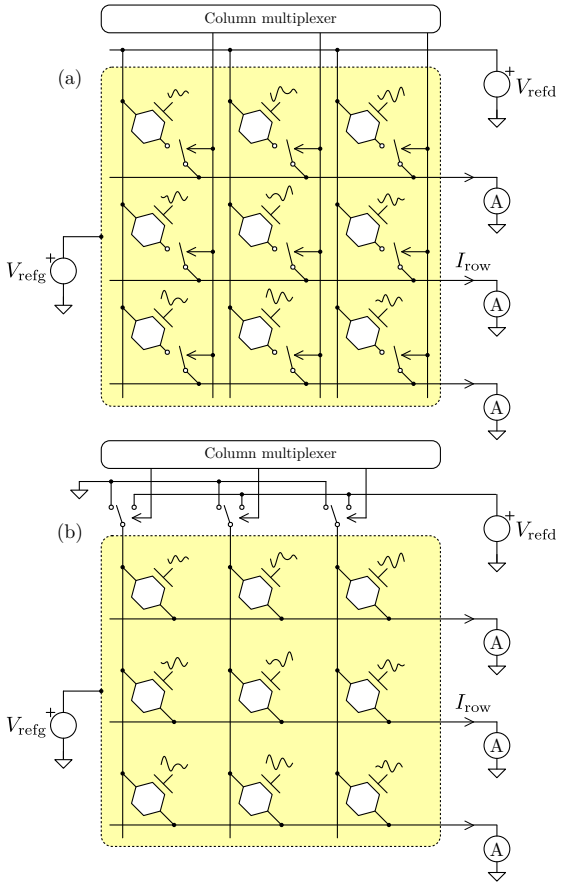

Figure 3. Classic (a) and proposed (b) time-domain multiplexing schemes for solution-gated GFET sensing arrays.

the chemical inertness of graphene, drifts occur only at very low rates, typically 50 mV/day when stabilized, allowing V_{GS} retuning on a daily basis and also the detection of brain signals in the infra-slow frequency regime [82], [83], [92], [93]. Furthermore, the high homogeneity in the CNP of solution-gated GFETs allows to polarize all the sensors close to the optimal bias simultaneously as seen in Fig. 2(b). In order to determine the optimal gate bias for the operation and to periodically correct for slow drifts between the reference electrode and the graphene potentials, the recording system must provide the capabilities to acquire the transfer curves of the transistors online.

III. Time-Domain Multiplexing of Solution-Gated GFET Sensing Arrays

Classic time-domain multiplexing (TDM) in current-mode sensing arrays usually employs a selection switch per pixel following Fig. 3(a), where V_{refg} and V_{refd} stand here for the GFET equivalent V_{GS} and V_{DS} biasing, respectively. Thanks to the column-wise scanning of these series switches, only one GFET sensor is connected to each row at any time and its source terminal is automatically biased to ground by the corresponding row amperometric circuit in order to read out the output current I_{row} in parallel for all rows.

The circuit alternative shown in Fig. 3(b) is proposed for the TDM of GFET sensors instead, where all devices are permanently connected to their shared columns and rows of the array. In other words, no individual series switch is required anymore for each μECoG recording site. Indeed, channel multiplexing is controlled from the ROIC by changing the effective V_{DS} biasing of each GFET

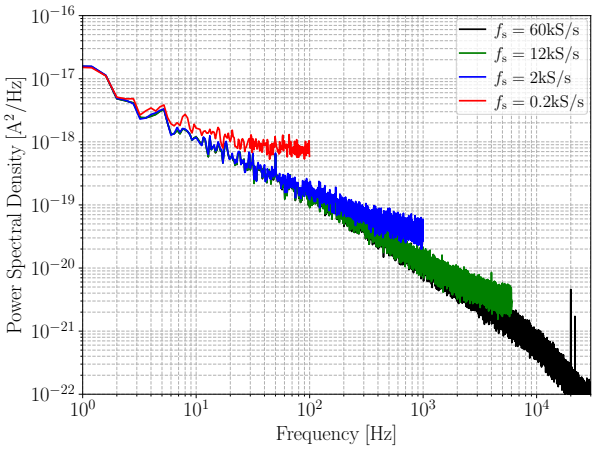

Figure 4. Experimental example of GFET noise folding effects in the proposed TDM scheme for different channel sampling rates.

column wise. While all row lines are biased to ground by their respective amperometric read-out circuits, the selection of a particular sensor of each row involves changing its column voltage from ground (i.e. $V_{DS} \equiv 0$) to the activation level (i.e. $V_{DS} \equiv V_{refd}$), with typical values of $V_{refd} < 100$mV. As a result, only the GFET sensor biased to $V_{DS} \neq 0$ can effectively contribute to I_{row}, so the wanted TDM functionality is achieved. However, it is key to control the biasing voltage of all array columns even when their active sensors are not selected, since leaving them in high impedance would cause crosstalk currents flowing between rows.

The proposed μECoG channel multiplexing method presents two main advantages. First, in the classic arrangement of Fig. 3(a), the ambivalent conduction nature of the GFET active sensor means in practice that another transistor technology needs to provide the switching devices embedded in the array. On the contrary, all switches of Fig. 3(b) are outside the flexible probe and located inside the CMOS ROIC, with the corresponding reduction in both technology complexity and integration costs of the GFET-only sensing array. Second, the proposed TDM scheme avoids digital control signals crossing the array and it allows smooth voltage transitions at the selected GFET, since its current is not turned off by interposing a high-impedance series switch, like in the classic scheme of Fig. 3(a), but by decreasing its V_{DS} biasing using low-impedance voltage sources instead. In consequence, artifacts and spurious signals due to charge injection and clock feedthrough can be attenuated. However, the multiplexing approach of Fig. 3(b) introduces a couple of circuit design challenges as well. Technology mismatching between GFETs of the same row requires a programmable offset cancellation mechanism to subtract from I_{row} the individual DC current level of each channel. Also, the parallel connection of several GFET devices reduces the row impedance seen by the ROIC, which causes a degradation of the corresponding input preamplifier noise figure. Indeed, both design challenges are fully addressed by the chip architecture of Section IV.

Nevertheless, two non-ideal effects can limit in practice the scalability of the GFET TDM solution proposed in Fig. 3(b). On the one hand, there is the intrinsic noise folding associated with the sampling process of the discrete-time multiplexing. Since no previous anti-aliasing filter can be performed at each recording site, noise folding becomes unavoidable, but it can certainly be mitigated by the use of oversampling. In this sense, Fig. 4 shows the benefits of this technique applied at the sensing array level. A safe margin of $f_s \geq 10$kS/s is chosen here to preserve the GFET noise levels at the frequencies of

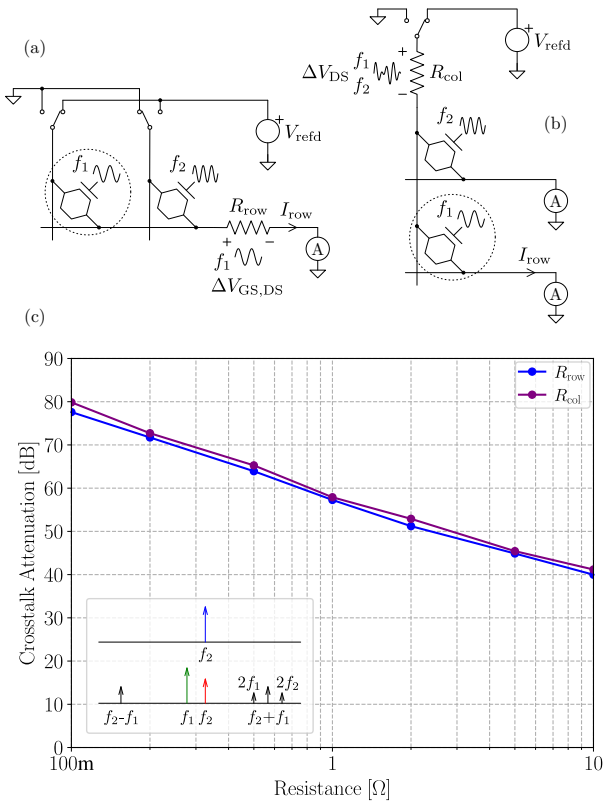

Figure 5. Main crosstalk mechanisms at row (a) and column (b) levels of the proposed TDM scheme, and simulated crosstalk attenuation (b) at 1-mV$_p$ inputs with $f_1 = 2.4$kHz, $f_2 = 2.6$kHz and the GFET bias point of Fig. 2(b).

interest in μECoG applications. As the number of columns scales up, the required scanning rate at the column multiplexer of Fig. 3(b) can become unfeasible to maintain the channel oversampling ratio.

On the other hand, crosstalk issues may arise in large sensing probes due to technology parasitics. Unlike in MEAs, the low-impedance nature of all the array rows and columns in the proposed TDM scheme means that the effects of parasitic coupling capacitances can usually be neglected here in favour of the contributions from the series resistances. This general concept is illustrated in Fig. 5(a) and (b), where R_{row} and R_{col} stand for the parasitic resistances at row and column levels, respectively. For simplicity, these lumped elements include the contributions from both the individual GFET drain/source contacts and the long routing of the array tracks. When $R_{row} \neq 0$, all the unselected GFET elements of the given row do not remain biased at $V_{DS} \equiv 0$ anymore and they contribute to the effective I_{row} readout with a low current for every column. Furthermore, each of these crosstalk currents is being modulated by the large signal of the active sensor through the GFET V_{GS} and V_{DS} ripple. In the case of R_{col}, crosstalk occurs between all the sensors selected at the same time through a V_{DS}-only mixing mechanism, so each I_{row} will contain signal components from every row. For illustrative purposes, Fig. 5(c) reports the simulation results obtained from the crosstalk analysis. Here, the GFET MIT model [94] has been employed after fitting the typical DC characteristics of Fig. 2(b). The obtained crosstalk figures point towards an upper bound of parasitic resistance around 1 Ω to preserve the 10-bit channel dynamic range. As the size of the μECoG probe scales up, the parasitic resistance of the flexible thin film technology can become dominant.

IV. 1024-Channel ROIC Architecture

The architecture of the 1024-channel ROIC and its attachment to a 32×32 GFET probe for μECoG are both shown in Fig. 6. Thanks to the use of TDM at array level, only 64 pads are needed to implement all the sensor-to-circuit connections, which means a 16-fold reduction in the wiring requirements of the hybrid packaging respect to the point-to-point solutions referred in Section I.

The ROIC internal structure follows a highly modular approach to ease its scalability in which most part of the circuitry is devoted to the row read-out signal processing. The first stage of the row AFE consists on an offset current subtractor circuit, explained later on, and the current-to-voltage preamplifier with a fixed transresistance gain $R_{gain} = 25$kΩ. The resulting voltage waveform is further processed by the buffer stage, whose purpose is double: to implement the single-ended to fully-differential signaling conversion at V_{amp} and to provide kickback isolation between the posterior discrete-time blocks and the continuous-time input preamplifier. The next stage of the row module is a switched-capacitor (SC) programmable-gain amplifier (PGA) with fixed feedback capacitor $C_f = 1$pF and configurable sampling capacitor C_s to program gain factors C_s/C_f equal to ×2, ×4, ×8 or ×16. This stage is in charge of adapting the envelope of V_{pga} to fit the data converter full scale, and it also implements the low-frequency noise cancellation mechanism described in Section V. Data conversion is executed in parallel for each row through the successive approximation register (SAR) ADC detailed in Section VI. This ADC provides a theoretical 13-bit dynamic range per TDM sample at 422 kS/s, which is equivalent to 13.2 kS/s per channel. In this sense, a 3-bit safe guard is chosen to compensate for possible losses due to extra circuit noise and distortion in order to ensure 10 bit per channel. Finally, row digital outputs are collected and packed in groups of 4 rows resulting in a total of 8 output serial lines at 27 Mbps. The modular ROIC architecture of Fig. 6 allows the definition of regions of interest (ROIs) in the GFET array for the purpose of lowering circuit power consumption. In this sense, all the ROIC internal configuration, like the individual offset current cancellation per GFET or the PGA gain factor per row, is digitally programmed through a custom serial peripherial interface (SPI).

The channel multiplexing mechanism of Section III, with activation levels $V_{refd} \sim 100$mV together with GFET on-resistance values $R_{gfet} \sim 2$kΩ, returns a typical static current of 50 μA for each selected channel. Since the read-out system is DC coupled, this component needs to be subtracted from I_{row} to prevent signal saturation at the output of the preamplifier. Due to GFET technology mismatching, such a current cancellation can not be performed through a constant sink, so the digitally controlled offset subtraction mechanism of Fig. 7 is proposed for this purpose. The row current-mode D/A converter (I-DAC) generates the offset level I_{off} for each individual column according to the global reference V_{refo} and a digitally programmable thermometric resistor network. A resistor-based implementation of I-DAC has been chosen instead of a programmable MOS current mirror in favour of lower flicker noise contributions at the input of the row preamplifer, but at the cost of introducing absolute resistance calibration, as described in Section VIII. The 8 combinations of the parallel resistor network of Fig. 7 return the following equivalent resistance configurations:

$$R_{off}[n] = \frac{7}{7+n} R_u \quad \text{for} \quad n = 0 \ldots 7, \tag{1}$$

which correspond to $\left\{1, \frac{7}{8}, \frac{7}{9}, \frac{7}{10}, \frac{7}{11}, \frac{7}{12}, \frac{7}{13}, \frac{1}{2}\right\} R_u$. Hence, the resulting I-DAC offset current shows a linear behaviour respect to its digital control according to:

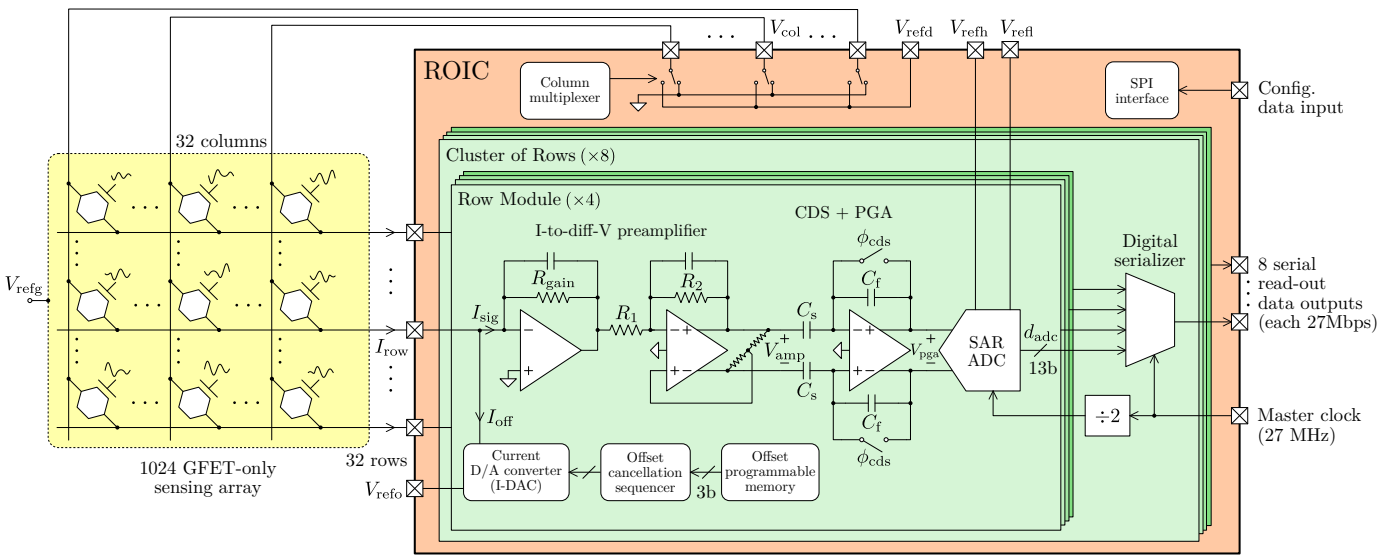

Figure 6. 1024-channel ROIC architecture proposal for the time-domain multiplexing of GFET-only sensor arrays in brain mapping.

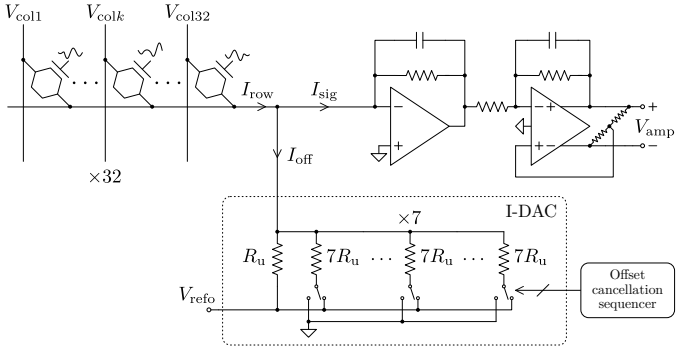

Figure 7. Row 8-level current D/A converter (I-DAC) for the individual subtraction of each GFET current offset.

$$I_{\mathrm{off}}[n] = -\frac{V_{\mathrm{refo}}}{R_{\mathrm{u}}}\left(1+\frac{n}{7}\right) \quad \text{for} \quad n = 0\ldots 7, \tag{2}$$

with an equivalent least significant bit (LSB) equal to $V_{\mathrm{refo}}/7R_{\mathrm{off}}$. For the nominal values $R_{\mathrm{u}} = 14.3\mathrm{k}\Omega$ and $V_{\mathrm{refo}} = -0.5\mathrm{V}$, the offset cancellation range is $-15\,\mu$A to $+20\,\mu$A around the typical GFET DC bias of $50\,\mu$A and its residue at I_{sig} is limited to $\pm 5\,\%$, which is low enough to not saturate the AFE chain. In practice, the thermometric code is generated from a 3-bit natural-binary signature stored in the ROIC for each of the 1024 GFETs of the sensing array. The resulting 3-kbit calibration map of the array probe is uploaded into the ROIC through its digital SPI interface and, if necessary, it can be updated at any time between recordings.

Concerning the OpAmps needed in Fig. 6 for the continuous-time section of each row AFE, they must deal with resistive loads and low-amplitude signals with high-speed transitions due to the switched nature of the TDM waveforms I_{row} coming from the GFET array. Taking into account the above requirements, the CMOS circuit topology of Fig. 8 is proposed for their implementation. The presented solution is based on a Class-AB variable-mirror amplifier (VMA) from these authors [95] but modified here to incorporate a floating push-pull output stage and a continuous-time common-mode feedback (CMFB) control. As it can be noticed, the OpAmp circuit is composed of two parallel and complementary paths for the control of the push-pull section. The core of the OpAmp topology is the

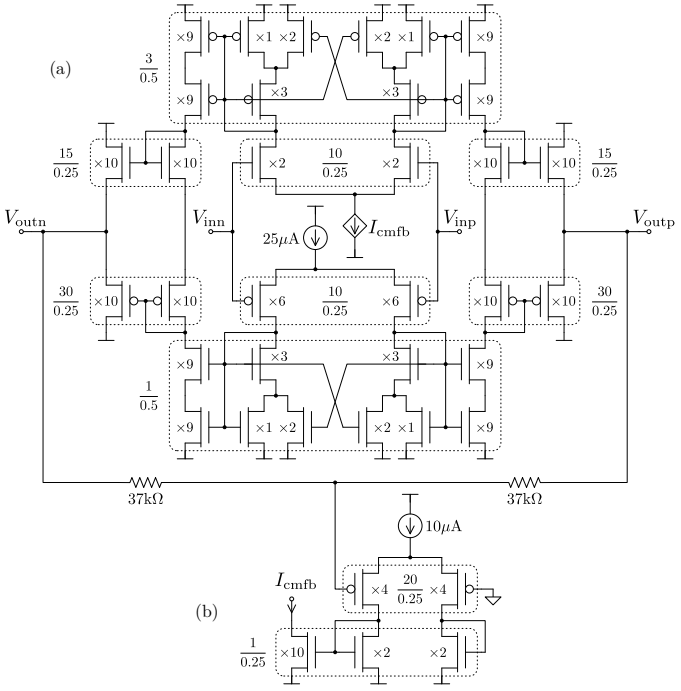

Figure 8. Fully-differential push-pull Class-AB VMA (a) and CMFB (b) CMOS circuits proposed for the second section of the row preamplifer. All transistor dimensions in μm and technology matching groups in dashed boxes.

variable-geometry current mirror attached to each input differential pair, which introduces partial positive feedback through the use of cross-coupled transistors in order to generate Class-AB peak currents that exceed the bias levels of the tail sources. Apart from this low-power capability, two other main advantages of the VMA are exploited here. Firstly, since the amplifier open-loop gain is located in a single stage, the close-loop frequency compensation can tolerate a wide range of output loading conditions without stability issues. This robustness is of special interest due to the changes in the row impedance when the GFET sensing array is scaled up (e.g. 4×4, 8×8 up to 32×32), as illustrated in Section V. Secondly, the Class-AB operation of the variable mirror relies on

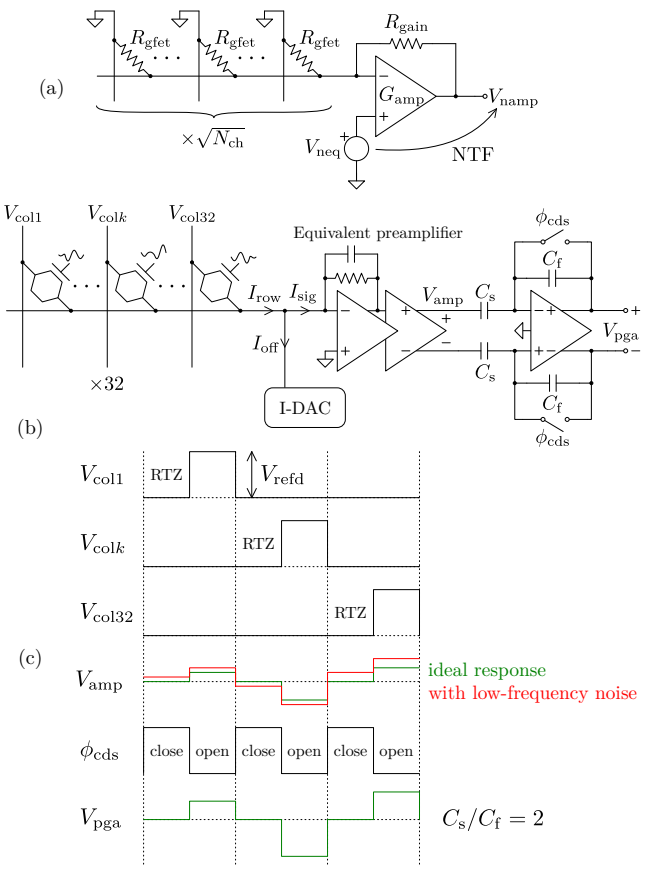

Figure 9. Row preamplifier low-frequency noise model (a), cancellation scheme (b) and CDS operation at the PGA stage (c). Waveforms not to scale.

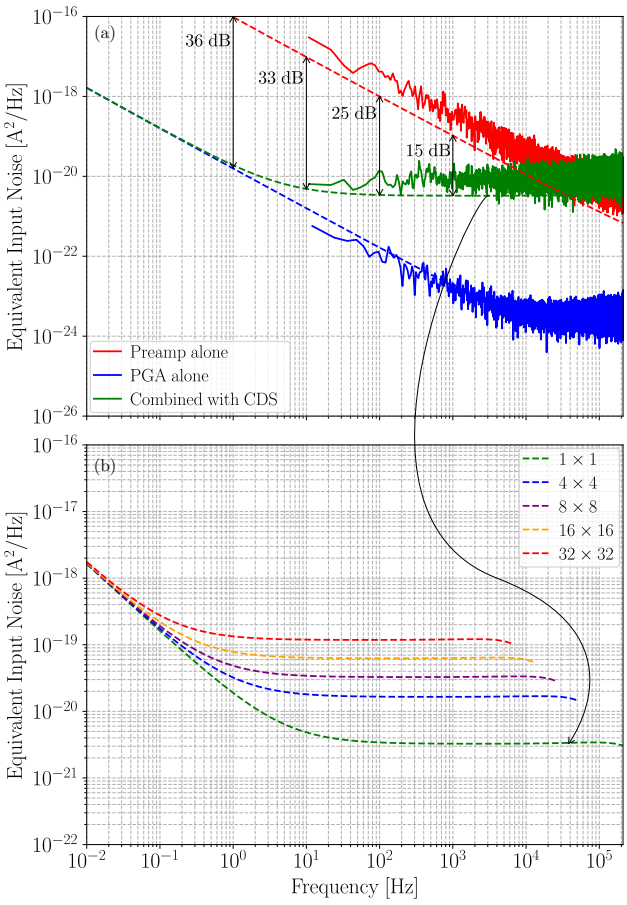

Figure 10. Post-layout simulation of the CDS noise cancellation mechanism for $C_s/C_f = 2$ (a) and noise profile per channel after time-domain demultiplexing for different GFET probe array sizing (b). Solid and dashed lines from transient noise and periodic noise results, respectively.

transistor matching only [95], so OpAmp speed performance shows low sensitivity to process, supply voltage and temperature.

V. CMOS Flicker Noise Cancellation

Due to the permanent and parallel connection of all GFET devices to the corresponding rows of the sensing array in the proposed TDM scheme of Fig. 3(b), the equivalent resistance of each row scales $\propto 1/\sqrt{N_{ch}}$, and it may be as low as $R_{gfet}/32 \sim 60\,\Omega$. While this is advantageous against capacitive coupling between routing lines, it imposes severe noise restrictions for each row preamplifier of the ROIC. Such an unwanted effect can be explained using the AFE equivalent noise model of Fig. 9(a). The associated noise transfer function at low frequency is found to be:

$$\mathrm{NTF} \doteq \frac{V_{namp}}{V_{neq}} = \frac{G_{amp}}{1+G_{amp}H} \sim \frac{1}{H}, \tag{3}$$

where G_{amp} stands for the DC open-loop gain of the preamplifier OpAmp and H is the voltage feedback factor defined by the row impedance:

$$H = \frac{R_{gfet}/32}{R_{gfet}/32 + R_{gain}} \simeq \frac{1}{32}\frac{R_{gfet}}{R_{gain}} \sim \frac{1}{400}. \tag{4}$$

Hence, although the VMA OpAmps like Fig. 8 can exhibit G_{amp} values exceeding 80 dB, their NTFs will always suffer from the high feedback attenuation imposed by the upscaling of the GFET array. In order to minimize its impact, the preamplifier noise cancellation mechanism of Fig. 9(b) is proposed. Basically, this scheme reuses the discrete-time SC PGA stage already present in Fig. 6 to implement a correlated double sampling (CDS) of the preamplifier noise for the purpose of promoting the cancellation of its low-frequency components, like MOSFET flicker noise contributions.

The principle of operation of this cancellation circuit is illustrated in the chronogram of Fig. 9(c). As it can be noticed, each time slot dedicated to the multiplexing of one GFET column has been divided in two periods, a return-to-zero (RTZ) phase (ϕ_{cds} high), when none of the column GFETs is selected, and the regular channel amplification phase (ϕ_{cds} low). During the RTZ phase, V_{amp} only holds the preamplifier noise, which is sampled in C_s. Once in the second phase, this noise sample value is subtracted from the channel signal before the actual amplification provided by the capacitive ratio C_s/C_f of the PGA circuit. As a result, the low-frequency noise components and offsets introduced by the preamplifier are cancelled in V_{pga} prior to the data conversion of each TDM sample.

Fig. 10(a) shows the AFE spectral profiles returned from the noise simulation of the ROIC connected to the 32×32 GFET sensing array with the typical MOSFET flicker noise roll-off of -10 dB/dec. As expected, the unfavourable NTF of the preamplifier would cause this stage to dominate the overall noise figure when compared to the PGA contribution. Thanks to the embedded CDS mechanism running at 422 kHz, a first-order noise shaping is applied to the preamplifier profile. Some excess of noise is cumulated at high frequency due to uncorrelation and also from folding not cancelled by the limited anti-aliasing filtering provided by the preamp stages of Fig. 6. Anyway, the

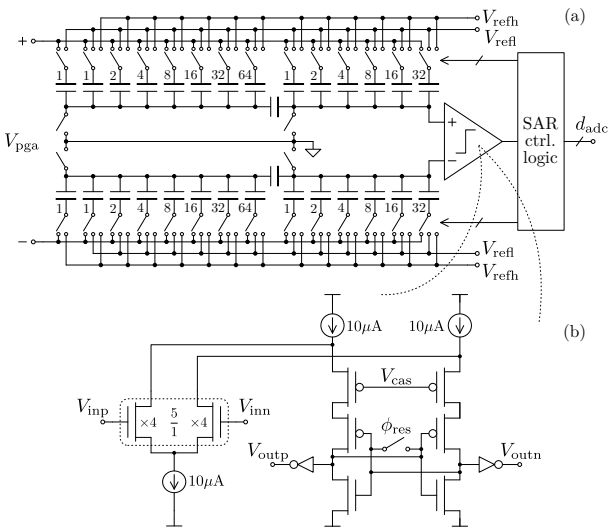

Figure 11. Segmented SC SAR ADC (a) as row data converter of Fig. 6 and proposed low-kickback comparator (b). All transistor dimensions in μm.

signal-to-noise ratio at the μECoG frequencies of interest drastically improves and even the noise floor of the PGA can be reached in the infra-slow spectrum band. The resulting noise profile per individual recording channel is shown in Fig. 10(b), where the noise folding contributions generated by the time-domain demultiplexing process can be clearly noticed.

Finally, it is important to clarify that, despite the operation of the auto-zeroing CDS mechanism described above, the complete signal processing chain of each row in Fig. 6 remains fully DC coupled to the GFET sensors. Therefore, the ROIC architecture is still capable of recording infra-slow signals.

VI. Row SAR A/D Converter

The SAR ADC architecture of Fig. 11(a) is chosen for the data conversion at row level of Fig. 6. This topology includes a SC network of 60-fF unitary capacitors segmented in two banks for the purpose of compacting the area of the feedback DAC. With an equivalent single-ended total sampling capacitor of 3.84 pF, these banks of 6-bit and 7-bit binary-weighted capacitance elements are responsible for the most significant bit (MSB) and LSB parts of the digital conversion, respectively. The row ADC features 2-$V_{\rm pp}$ differential input full scale around the common mode level of 0.9 V for $V_{\rm refl} = 0.4$V and $V_{\rm refh} = 1.4$V. The ADC circuit has been designed for a theoretical 13-bit dynamic range in terms of signal-to-quantization-noise ratio (SQNR) and kT/C noise floor. However, a conservative 3-bit safe margin was left for non-ideal circuit effects such as technological mismatching of the bridge capacitor between the MSB and LSB banks of the SC feedback DAC or noise coupling through the supply rails of the full chip. The data converter runs at an internal clock frequency of 13.5 MHz to provide a 422-kS/s conversion speed, which is equivalent to an effective Nyquist sampling rate of 13.2 kS/s per channel, so it covers the 10-kS/s oversampling specification per recording site for a 32×32 GFET probe array.

One of the typical bottlenecks of low-power SAR ADCs is the logic kickback from the comparator output reaching the high-impedance nodes of the SC network of the feedback DAC. In order to mitigate such an effect that tends to generate distortion, the CMOS comparator of Fig. 11(b) is proposed. This topology is intentionally split in two stages for better kickback isolation. Indeed, the circuit combines a continuous-time folded-cascode input stage together with a discrete-time latched output stage preset in metastability to limit the voltage swing observed by the input differential pair at every quantization phase.

Table I
Example of ROIC calibration results for four rows.

	$R_{\rm gain}$ [Ω]	$V_{\rm off1}$ [mV]	$\frac{R_2}{R_1}$	$\frac{C_{\rm s}}{C_{\rm f}}[0]$	$\frac{C_{\rm s}}{C_{\rm f}}[1]$	$\frac{C_{\rm s}}{C_{\rm f}}[2]$	$\frac{C_{\rm s}}{C_{\rm f}}[3]$	$V_{\rm off2}$ [mV]
Nominal	25324	0.00	1.000	2.000	4.000	8.000	16.00	0.00
Row 0	23142	-1.05	0.981	2.009	3.994	7.872	15.82	-39.3
Row 1	23614	-0.68	0.986	2.027	4.060	7.895	15.82	-18.0
Row 2	23878	-0.79	0.989	1.996	3.967	7.874	15.92	-30.5
Row 3	24142	-1.00	0.992	1.994	3.981	7.923	15.85	-35.4

	$R_{\rm off}[0]$ [Ω]	$R_{\rm off}[1]$ [Ω]	$R_{\rm off}[2]$ [Ω]	$R_{\rm off}[3]$ [Ω]	$R_{\rm off}[4]$ [Ω]	$R_{\rm off}[5]$ [Ω]	$R_{\rm off}[6]$ [Ω]	$R_{\rm off}[7]$ [Ω]
Nominal	14286	12500	11111	10000	9091	8333	7692	7143
Row 0	14051	13240	10823	9664	9437	8093	7826	6948
Row 1	14362	13141	11048	9891	9422	8242	7805	7124
Row 2	14411	13008	11127	10059	9307	8375	7840	7178
Row 3	14306	12800	11042	9932	9205	8246	7759	7065

VII. 1024-Channel ROIC in 0.18-µm CMOS technology

The 1024-channel ROIC has been fabricated in a 1.8-V 0.18-μm 6-metal MiM-capacitor CMOS technology, as shown in Fig. 12(a). The complete chip occupies an overall area of 18.7 mm^2, which is equivalent to 0.018 mm^2 per acquisition channel. As it can be noticed, most of the chip area is dedicated to the array of row modules. The ROIC total pad count is 120, but only 64 of them are used for the TDM of the 32×32 GFET sensing array, while the rest of pads are devoted to the high-speed serial read-out lines, the SPI-like interface for configuration, analog references and redundant supply pads.

Fig. 12(b) details the layout of the row module, which includes all the circuits explained in Sections IV to VI. The floorplan exhibits a mirroring symmetry respect to the x-axis in order to improve matching between the positive and negative paths of the fully-differential circuits. The total power consumption per row is 1.15 mW from the 1.8-V supply, which is equivalent to 36 μW per acquisition channel. From the breakdown analysis of Fig. 12(c), it is clear that most of the power consumption is due to the preamplifier, while the largest part of the row area is occupied by the SAR ADC.

VIII. System Calibration Methodology

Due to the high modularity of the ROIC architecture proposed in Fig. 6, some calibration procedure is needed to account for channel-to-channel mismatching caused by technological deviations between GFET sensors of the array and also between CMOS row modules. This section presents an automated methodology focused on individual channel gain equalization and also on dynamic range optimization. For illustrative purposes, experimental results from a tiny 4×4 GFET array and the corresponding ROIC rows are presented. The same automated procedure is applied later in Section IX for the case of 1024 channels with 32×32 GFET probes. The sequential steps of this system calibration methodology are as follows:

1) At ROIC row level, the low-power CMOS circuits presented in Sections IV to VI rely on a total of 16 parameters dependent on either absolute values or matching ratios: I-DAC offset configuration $R_{\rm off}[0\ldots7] = \left\{1, \frac{7}{8}, \frac{7}{9}, \frac{7}{10}, \frac{7}{11}, \frac{7}{12}, \frac{7}{13}, \frac{1}{2}\right\} R_{\rm u}$, preamplifier transimpedance gain $R_{\rm gain}$, preamplifier offset $V_{\rm off1}$, single-to-differential buffer matching R_2/R_1, PGA gain configuration $C_{\rm s}/C_{\rm f}[0\ldots3] = \{2, 4, 8, 16\}$ and combined PGA-ADC offset $V_{\rm off2}$. In order to calibrate them per row, $V_{\rm refo}$ can be exploited as an external test input in Fig. 6. Without

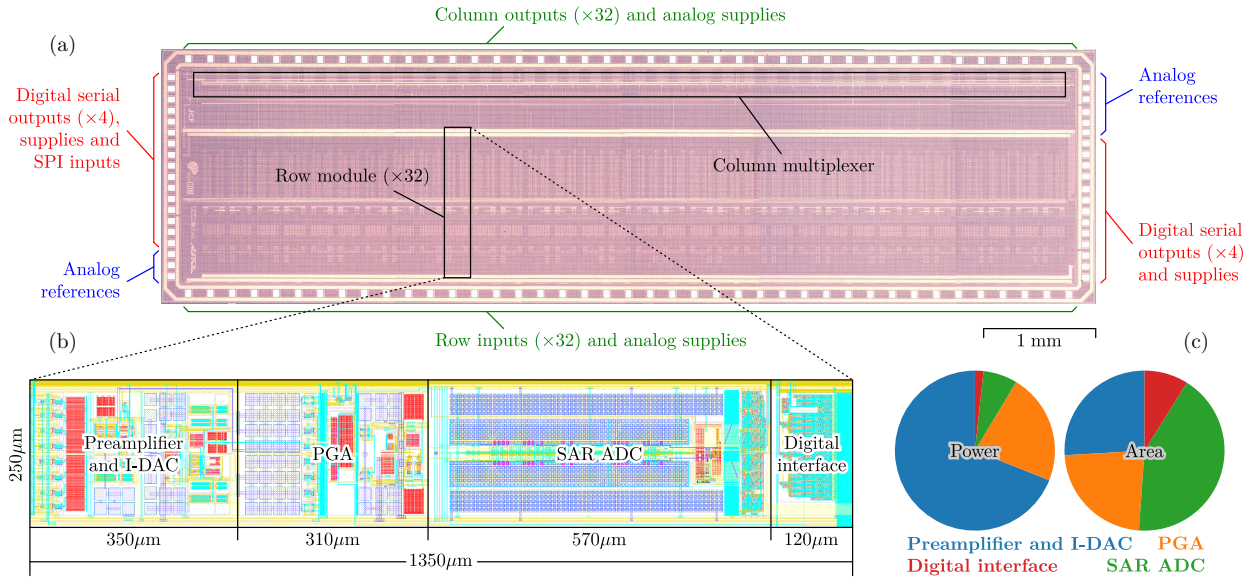

Figure 12. Chip photo (a), row layout (b) and breakdown (c) of the 1024-channel ROIC in 1.8-V 0.18-μm CMOS technology. Chip size is 2.2mm×8.5mm.

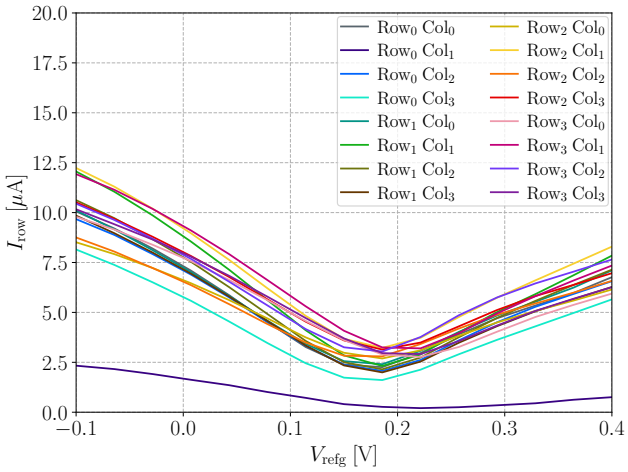

Figure 13. DC transfer curve for each GFET sensor of the array measured by the ROIC at $V_{\mathrm{refd}} = 16\mathrm{mV}$, $V_{\mathrm{refo}} = -100\mathrm{mV}$, $R_{\mathrm{off}}[3]$ and $C_{\mathrm{s}}/C_{\mathrm{f}} = 2$.

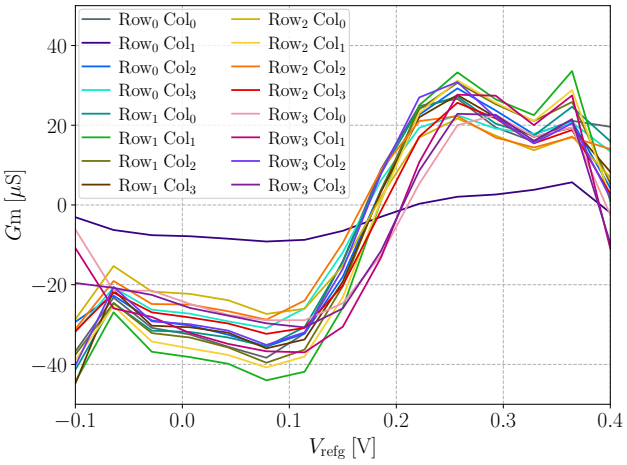

Figure 14. Transconductance curve for each GFET sensor of the array obtained from the experimental results of Fig. 13.

connecting any GFET probe to the ROIC, this input allows the following controllability of the equivalent analog read out at the ADC:

$$V_{\mathrm{adc}} = 2\frac{C_{\mathrm{s}}}{C_{\mathrm{f}}}\frac{R_2}{R_1}\left[\frac{R_{\mathrm{gain}}}{R_{\mathrm{off}}}V_{\mathrm{refo}} - \left(1+\frac{R_{\mathrm{gain}}}{R_{\mathrm{off}}}\right)V_{\mathrm{off1}}\right] + V_{\mathrm{off2}}. \tag{5}$$

By taking 16 measurements per row with different configurations, (5) becomes a 16-variable system of linear equations from which to extract the individual parameter values. The test pattern chosen for this purpose is: $R_{\mathrm{off}}[3]$, $C_{\mathrm{s}}/C_{\mathrm{f}}[0]$ and $V_{\mathrm{refo}} = \{-15, -25, -35, -45, -65, -75\}$ mV; $R_{\mathrm{off}}[0, 2, 5, 7]$, $C_{\mathrm{s}}/C_{\mathrm{f}}[0]$ and $V_{\mathrm{refo}} = -50\mathrm{mV}$; $R_{\mathrm{off}}[1, 4, 6]$, $C_{\mathrm{s}}/C_{\mathrm{f}}[0]$ and $V_{\mathrm{refo}} = 50\mathrm{mV}$; $R_{\mathrm{off}}[0]$, $C_{\mathrm{s}}/C_{\mathrm{f}}[1, 2, 3]$ and $V_{\mathrm{refo}} = \{-50, -25, -15\}$ mV. The resulting V_{adc} values are read out through the corresponding SAR ADC in parallel for all the 32 rows of the ROIC unit. An example of experimental extraction results for 4 rows is listed in Table I. In general, this first calibration step can be understood as a CMOS fabrication signature of each row circuit and therefore it may only need to be measured once during the lifetime of the ROIC device.

2) The next step is to choose the global V_{GS} (i.e. V_{refg}) and V_{DS} (i.e. V_{refd}) biasing levels of the GFET array in Fig. 6 that optimize overall sensitivity. This selection requires the measurement of the DC I-V transfer curve of every graphene transistor of the array. Given the $\pm$10-μA AFE input full scale for the minimum PGA gain configuration, I-DAC is programmed at $R_{\mathrm{off}}[3]$ and $V_{\mathrm{refo}} = -100\mathrm{mV}$, so each row module can handle $I_{\mathrm{row}} \in [0, 20\mu\mathrm{A}]$. With a preliminary low-value V_{refd} to avoid saturation, V_{refg} sweeping is concurrently executed for all GFET devices. Fig. 13 shows an example of the GFET curves measured through the ROIC. The derived G_{m} plots of Fig. 14 should allow the proper selection of the common bias point (e.g. $V_{\mathrm{refg}} = 100\mathrm{mV}$ and $V_{\mathrm{refd}} = 50\mathrm{mV}$).
3) Based on the measured curves, the equivalent G_{m} map of the array is recomputed for the new global $V_{\mathrm{refg,d}}$ bias point using GFET electrical models [94], like in Fig. 15(a). Together with

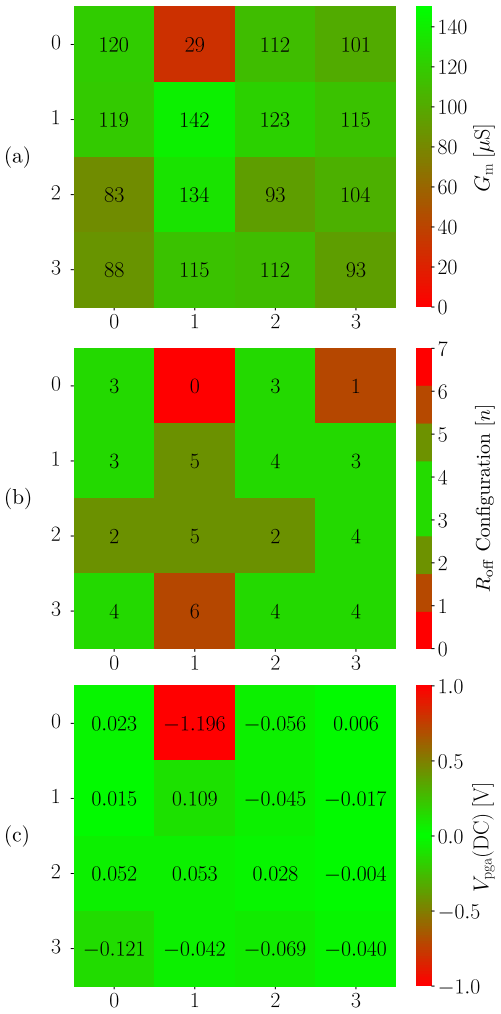

Figure 15. Experimental calibration map examples: (a) GFET transconductance for $V_{\mathrm{refg}} = 100\mathrm{mV}$ and $V_{\mathrm{refd}} = 50\mathrm{mV}$, (b) 3-bit I-DAC $R_{\mathrm{off}}[n]$ selection and (c) differential DC residue referred to the ADC input full scale.

Table I, this map is fundamental for the later individual channel gain equalization, and its simple inspection already allows the screening of the sensor array to locate non-working or poor-sensitivity recording sites (e.g. Row_0 and Col_1).

4) The last step involves the selection of the global V_{refo} level and the individual 3-bit I-DAC codes in Fig. 6 to minimize I_{sig} offsets caused by GFET mismatching, which prevent reaching the maximum full-scale occupancy (so dynamic range) at the ADC stage. According to the GFET array screening, the overall average DC current level $\bar{I}_{\mathrm{gfet}}$ of all working sites is computed together with the average $\bar{R}_{\mathrm{off}}[3]$ of all the 32 row I-DAC modules, so the global offset reference level is set to $V_{\mathrm{refo}} \doteq -\bar{I}_{\mathrm{gfet}}\bar{R}_{\mathrm{off}}[3]$. Finally, each individual GFET I-DAC code can be found to minimize the DC residue at V_{pga} taking into account Table I. Experimental examples of the resulting $R_{\mathrm{off}}[n]$ configuration and DC residue maps are shown in Fig. 15(a) and (b), respectively.

The effectiveness of the above system calibration methodology can be noticed in the measurement example of Fig. 16, when a global harmonic waveform is applied to the reference electrode V_{refg} of the GFET array of Fig. 6.

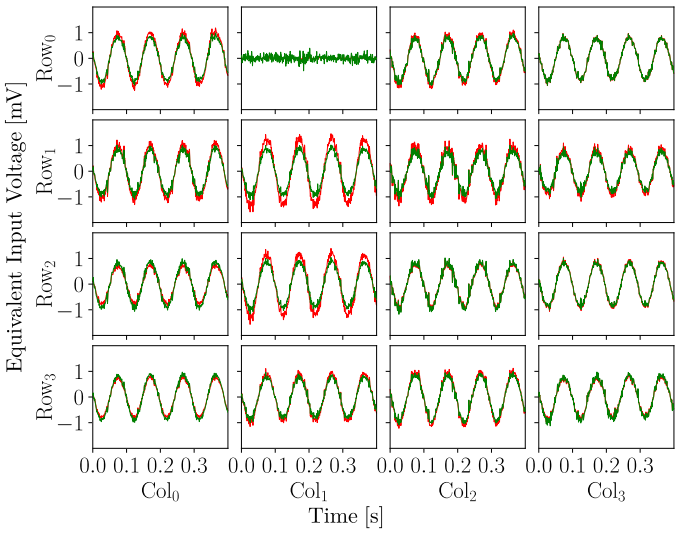

Figure 16. Demultiplexed transient waveforms measured by the ROIC at $V_{\mathrm{refg}} = 100\mathrm{mV}$ and $V_{\mathrm{refd}} = 50\mathrm{mV}$ when 1-$\mathrm{mV_p}$ 10-Hz harmonic stimulus is added to V_{refg}. Raw ADC data (red) and equalized readings from calibration (green) after applying 100-Hz digital low-pass filtering.

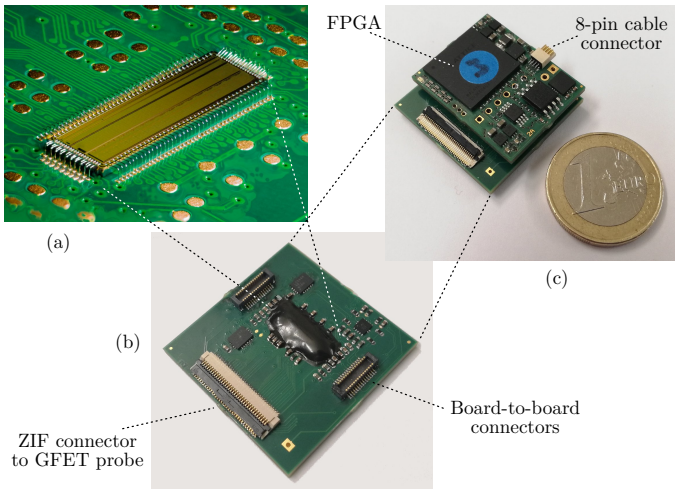

Figure 17. ROIC direct wire-bonding (a) to chip carrier (b) and stacked FPGA PCB for 1024-channel tethered headstages (c). Overall size is 28mm×28mm.

IX. Experimental Results

The custom ROIC headstage of Fig. 17 has been developed for μECoG recording in small-size animals like rodents. As it can be noticed, the printed circuit board (PCB) design is oriented towards a compact-size lightweight device with high modularity, so its scalability can be extended by combining multiple ROICs. The headstage is composed of two hardware modules, the chip carrier and the field-programmable gate array (FPGA) board, which is capable of managing several ROIC modules.

Due to the 3:1 aspect ratio of the die of Fig. 12, direct wire bonding has been chosen to attach the 120-pad ROIC to its chip carrier, as shown in Fig. 17(a), combined with glob-top passivation. Apart from carrying the ROIC die itself, the PCB module of Fig. 17(b) also holds the decoupling capacitors, analog buffers for references and 3-state logic buffers, packed here in 74244 chips, for the serial outputs running at 27 Mbps, so several 1024-channel ROIC modules can be stacked to share the same bus for connecting to a single FPGA module. Indeed, two 30-pin board-to-board connectors from Molex LCC, IL, provide all the connectivity between ROIC and FPGA

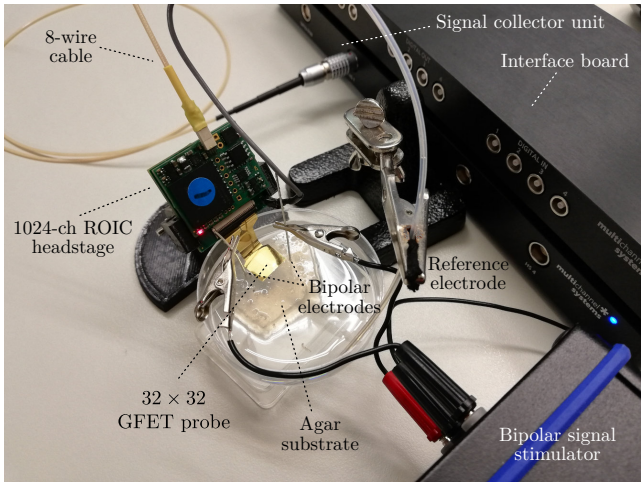

Figure 18. Laboratory setup for the test of the 1024-channel ROIC μECoG headstage with 32×32 solution-gated GFET probes.

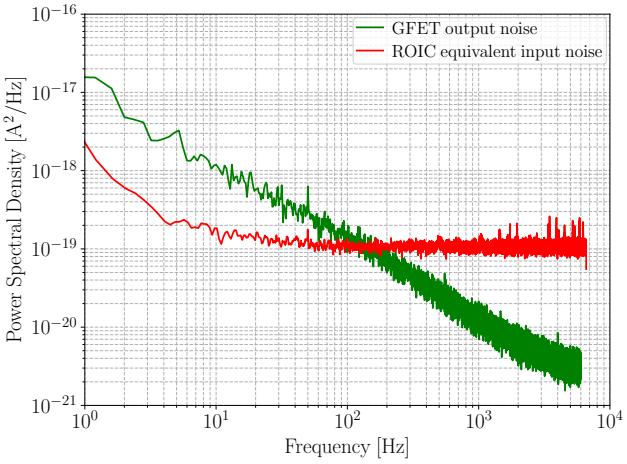

Figure 19. Measured equivalent input noise of the ROIC channel for $C_s/C_f = 2$ compared to the experimental output noise of the GFET sensor sampled at 12 kS/s, like in Fig. 4.

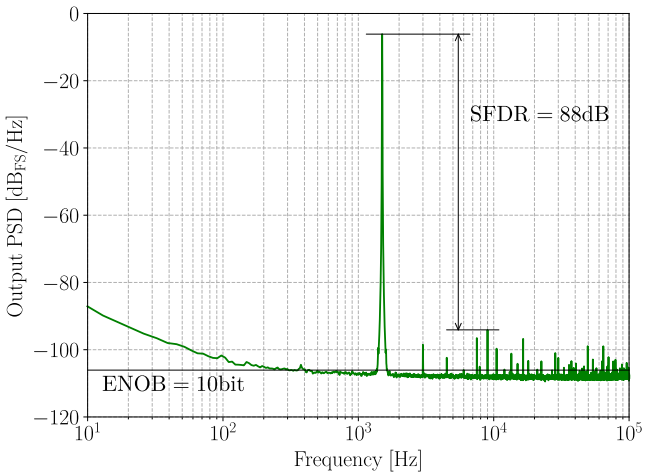

Figure 20. Measured output of the row SAR ADC for an harmonic input signal at -6 dB$_{FS}$ and 1.5 kHz.

PCBs. On the other hand, the compact 70-pin zero-insertion-force (ZIF) connector FH29B-70S from Hirose Electric Co. Ltd., Japan, is employed for the direct attachment of each 32×32 GFET probe to its corresponding ROIC module.

The FPGA board stacked on top of Fig. 17(c) is built around the LFE5U-45F device from Lattice Semiconductor Corp., OR, packed here in ceramic 256-pin ball-grid array. This FPGA already contains several necessary blocks for the ROIC application, such as the 54-MHz phase-locked loop (PLL), the 378-MHz serializer/deserializer (SerDes) and the low-voltage differential signalling (LVDS) drivers for the system cable, which is operated at double data rate (DDR). The custom parts synthesized inside this FPGA are the read-out data packetizer and the SPI master for the selection/configuration of each ROIC. The FPGA board also hosts the power management unit and the 10-bit octal DAC 108S085 from Texas Instruments Inc., TX, for the programmability of ROIC analog references V_{refg}, V_{refd}, V_{refo}, V_{refh} and V_{refl} of Fig. 6. Finally, the 8-pin polarized connector PZN-08-AA from Omnetics Connector Corp., MN, is used to plug the system cable carrying the 4 differential wire pairs for master-slave input and output, clock and supply.

The size and weight figures of the resulting 1024-channel μECoG headstage are $28 \times 28 \times 7\,\mathrm{mm}^3$ and 6.7 g, respectively. Also, the average current consumption is around 150 mA from the 4.5-V external supply, being only 20 mA drained by the ROIC. Concerning the acquisition system, this headstage is combined with the signal collector unit MCS-SCU and the interface board MCS-IFB both from Multi Channel Systems GmbH, Germany, for the connection to a PC through USB 3.0 interface. The complete laboratory setup with instrumentation for in-vitro measurements is shown in Fig. 18.

The first electrical tests have been carried out without attaching any GFET sensing array and they have been focused on the characterization of the row CMOS circuits of the ROIC. In this sense, Fig. 19 returns the equivalent input noise spectral density of the ROIC channel when compared to the typical flicker profiles experimentally obtained from solution-gated GFET sensors. The measured results are consistent with the simulation profiles of Fig. 10(b) and they show that ROIC noise contributions do not constrain GFET sensitivity below 100 Hz. In terms of large-signal linearity, the half full-scale harmonic response measured at the row SAR ADC in Fig. 20 does not exhibit relevant harmonics with spurious-free dynamic range (SFDR) values around 90 dB, while the practical ENOB figure is 10-bit due to the transfer curve dead zones caused by non-exact bridge capacitors.

The second ROIC tests incorporate a 16×32 array of solution-gated GFET sensors in saline solution for the validation of the calibration methodology proposed in Section VIII. For this purpose, the battery-operated generator g.SIGgen from g.tec medical engineering GmbH, Austria, has been employed to apply an harmonic signal of 1 mV$_p$ and 10 Hz at the reference electrode, so all recording sites of the GFET probe are stimulated simultaneously and homogeneously. Although this GFET array is half the scale of a 1024-channel probe, it already uses the full 32 rows of the ROIC. The measured results before and after applying the automated calibration maps are plotted in Fig. 21. In general, good equalization figures can be achieved, but there is still some room for improvement (e.g. the selection of the optimum GFET bias point). Also, the overall distribution of equivalent input noise profiles including the combined effects of the GFET sensor and the ROIC channel are shown in Fig. 21(e), which returns 32 μV$_{rms}$ from 1 Hz to 100 Hz.

The ROIC headstage has been also tested with 32×32 GFET probes in agar substrate and under bipolar current stimulation following the specific laboratory setup of Fig. 18. The Multi Channel Systems STG 4002 generator is employed here to generate a $\pm$100-μA$_p$ 10-Hz bipolar current injection located at the opposite corners of the GFET probe, as marked in Fig. 22. In contrast to the

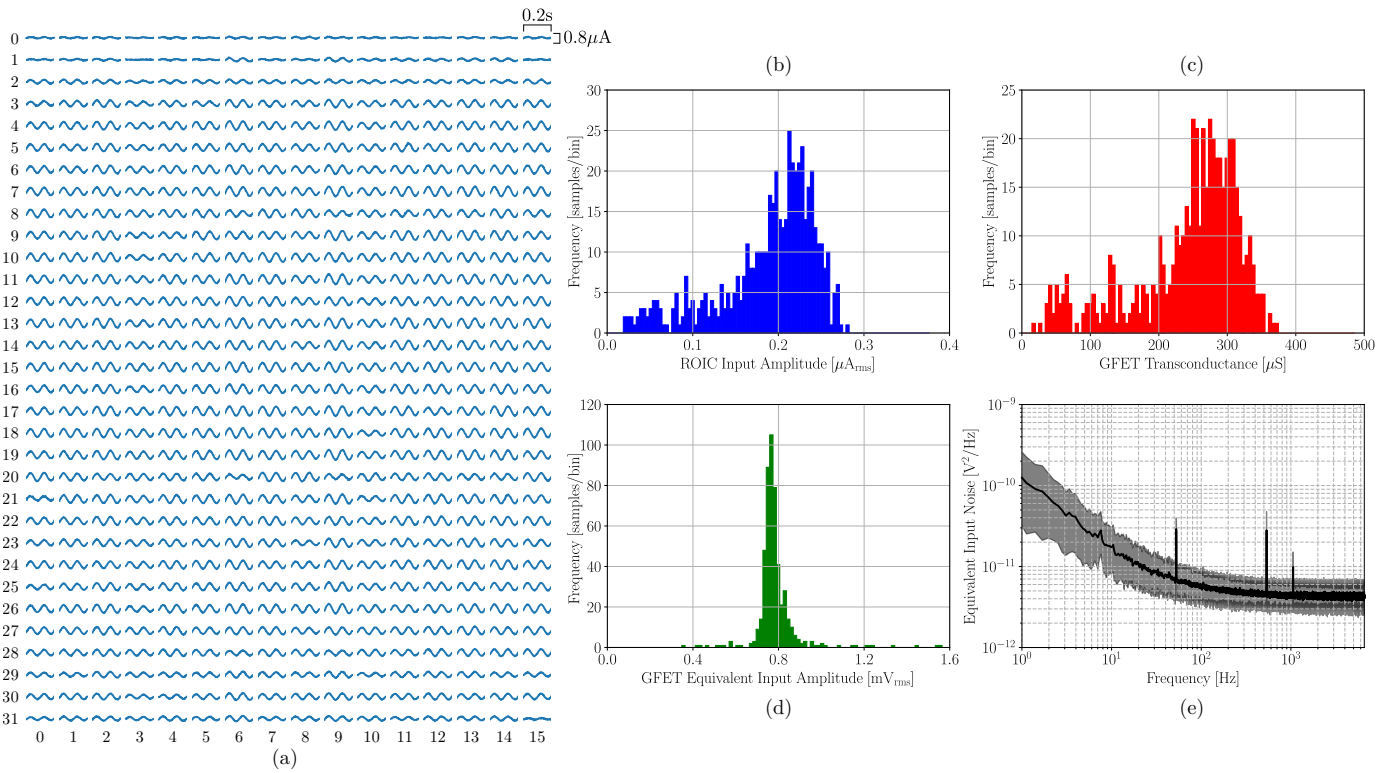

Figure 21. Waveforms (a) and distribution (b) measured by the ROIC headstage with a 16×32 GFET array in saline solution under 1-mV_p 10-Hz uniform stimulation; GFET transconductance distribution from extracted maps (c); equivalent input amplitude distribution (d) and channel noise (e) after calibration.

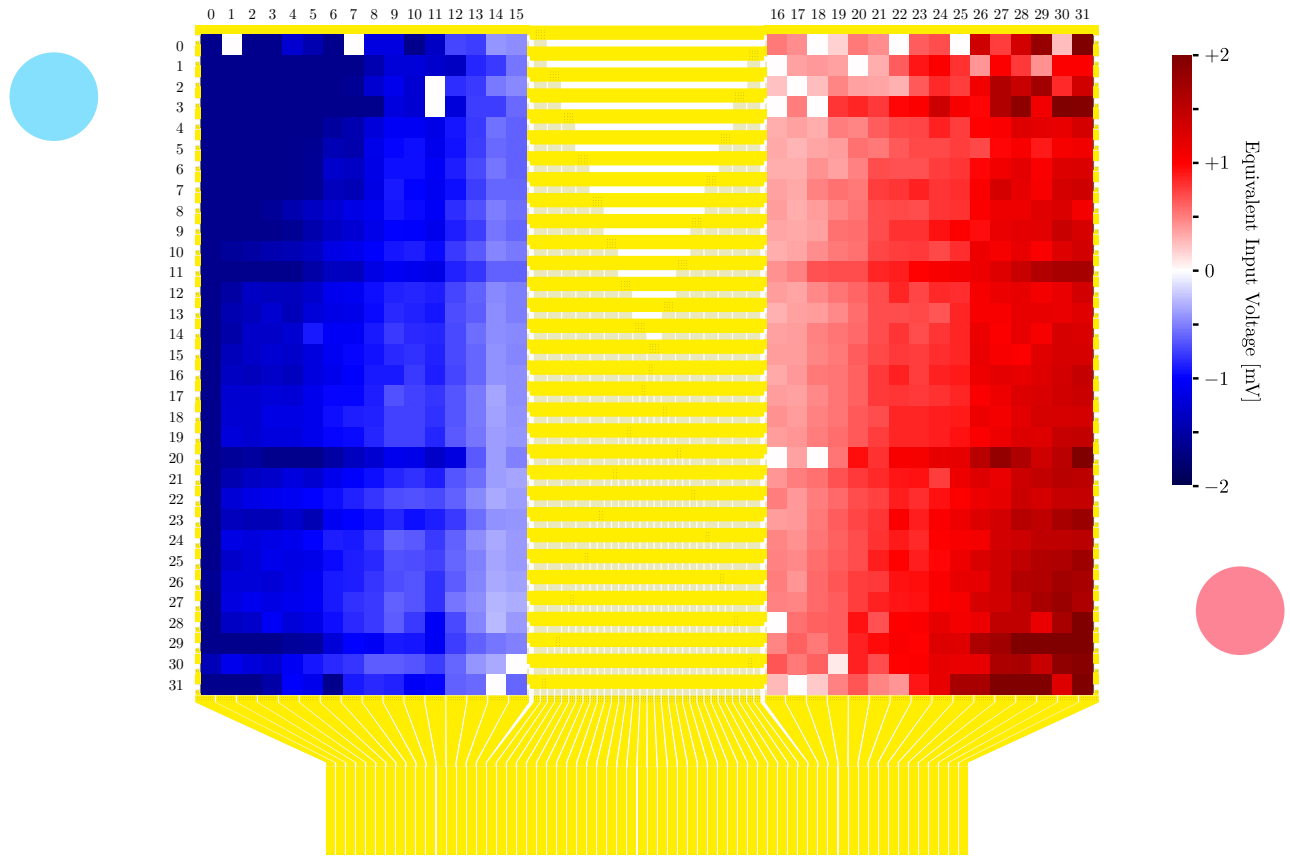

Figure 22. Input peak values measured by the ROIC headstage with a 32×32 GFET array on agar substrate under 100-μA_p 10-Hz bipolar stimulation.

Table II
COMPARISON WITH RELEVANT STATE-OF-ART NEURAL ROICS.

	[5] JSSC'14	[6] JSSC'17	[27] TBCAS'17	[30] Sensors'17	[13] ISSCC'18	[26] Biosens'19	This work	
Application	cell culture	cell culture	penetrating	penetrating	cell culture	penetrating	μECoG	
Architecture	muxed	muxed	muxed	muxed	muxed	muxed	muxed	
Integration	monolithic	monolithic	monolithic	monolithic	monolithic	monolithic	hybrid	
CMOS technology	custom	180	130	130	130	180	180	nm
Channels / chip	1024	2048	384	1356	1024	512	1024	
Bandwidth	10	10	10	10	10	12.5	5	kHz
Dynamic range	10	10	10	10	10	12*	10	bit
Power / channel	31	16	49	45	93	6*	36	μW
Area / channel	0.033	0.052	0.120	0.120	0.188	0.012*	0.018	mm^2

Note: *ROIC with external ADC.

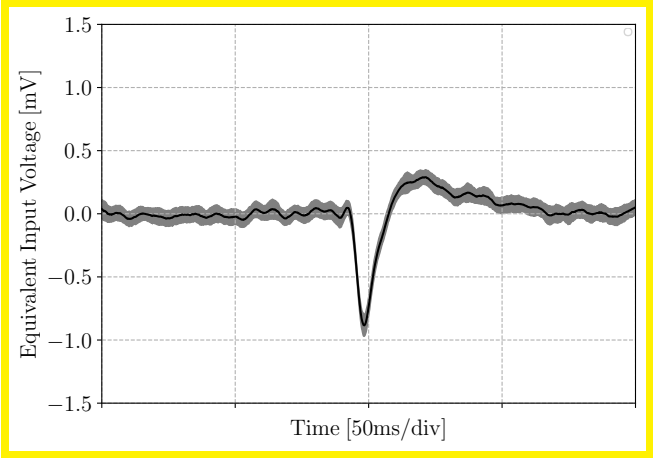

Figure 23. Median waveform and distribution measured by the calibrated ROIC headstage with a 16×32 GFET array in saline solution and with 1-mV$_{\mathrm{p}}$ synthesized excitatory postsynaptic potential signal applied to the reference electrode. Results after 150-Hz low-pass filtering.

setup of Fig. 21, this type of characterization generates different input stimulus along the full array of recording sites thanks to the spatial voltage potential gradient between the two electrodes, so finer studies like crosstalk analysis can be conducted. The experimental maps of Fig. 22 show the typical gradients of input amplitudes, being the zero-input transition area located in the gap between the two physical hemispheres of the 1024-channel GFET probe. As it can be noticed in the same figure, some rows exhibit read-out amplitudes locally higher than expected probably due to an excess of contact resistance at the corresponding ZIF connector pin of Fig. 17(b), which does not allow the proper voltage biasing of that specific array rows by their ROIC preamlifiers causing an excess of crosstalk in that particular location of the GFET probe.

Finally, the ROIC headstage with 16×32 GFET probe has been tested with synthesized electrophysiological waveforms in saline solution to validate its overall functionality in real scenarios. For this purpose, the Multi Channel Systems MEA-SG signal generator is configured to apply a 1-mV$_{\mathrm{p}}$ excitatory postsynaptic potential waveform at the reference electrode. The resulting measurements shown in Fig. 23 are consistent with the synthesized signal model.

X. CONCLUSIONS

A 1024-channel neural read-out IC for solution-gated GFET sensing probes in massive μECoG brain mapping has been presented. The proposed time-domain multiplexing scheme of these active sensors in GFET-only arrays enables a low-cost and scalable hybrid integration with custom CMOS circuits. In this sense, a modular ROIC architecture has been introduced for this purpose oriented towards headstage power reduction and parallel channel upscaling. Specific low-power CMOS circuits have been also proposed to integrate all the required signal processing at ROIC row level, from the GFET input analog frontend to the output A/D conversion. Furthermore, a minimalist circuit solution based on CDS has been designed to compensate the increase of the row preamplifier noise figures due to the GFET array upscaling. The complete 1024-channel ROIC has been fabricated in a standard 1.8-V 0.18-μm CMOS technology.

Beside the ROIC device, an automated calibration methodology has been proposed to account for channel-to-channel mismatching caused by technological deviations between GFET sensors of the array and also between CMOS row modules. Indeed, the ROIC itself can be used not only for the read-out of neural signals but also as a micro-instrument for the in-situ characterization of each GFET active sensor of the array probe prior to the recording session.

A custom headstage for μECoG experiments with rodents has been also developed combining one or more 1024-channel ROIC modules with a single FPGA module for its integration in standard electrophysiology recording systems. Experimental results have been also reported of the resulting ROIC headstage with 16×32 and 32×32 GFET probes in saline solution and agar substrate. In particular, harmonic stimulation experiments both at the reference electrode and using bipolar currents show the expected results along the full GFET array.

A comparison of the presented chip and the relevant state-of-art neural ROICs is listed in Table II. As it can be noticed, this work shows competitive figures compared to existent monolithic solutions and achieves the largest scalability in hybrid neural ROICs, as marked in Fig. 1(b). Finally, it is worth to highlight that unlike the rest of ROICs for passive micro-electrodes, this integrated μECoG platform with GFET active sensors is DC coupled so it is capable of recording infra-slow neural signals.

ACKNOWLEDGMENT

This work has been partially funded by the European Commission under the project BrainCom H2020-FETPROACT-2016-732032.

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A 1024-Channel 10-bit 36-μW/ch CMOS ROIC for Multiplexed GFET-Only Sensor Arrays in Brain Mapping

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Answers to the Review of TBioCAS-2021-May-0197-ICECS2020.R1

Following the request of Editor in Chief, what it follows is a detailed description of all the modifications made in the original manuscript to incorporate the comments and/or suggestions from the Associate Editor and the Reviewers.

Associate Editor

According to the reviewers' comment, I suggest to include some relevant reference for noise comparison, also consider to justify using sin wave to validate the implemented system.

Thanks for your feedback.

Following the reviewer's request, ROIC headstage measurements of synthesized μECoG signals have been added to Section IX (p. 12, Fig. 23 and par. 2).

Concerning noise figures, a reasoned answer on comparable figures is given to the reviewer.

Reviewer Number 1

All my concerns were well addressed.

Thanks for your positive feedback.

Reviewer Number 2

I thank the authors for their extensive revisions. I have no further comments.

Thanks for your positive feedback.

Reviewer Number 3

I appreciate the authors' efforts in revising the paper. While most of my concerns have been addressed, there are two remaining ones.

Thanks for your positive feedback.

1. This revision still fails to demonstrate any experimental results in a real ECoG recording. The authors argued using sinusoidal input signal is a standard characterization of readout chip. This is certainly true, but please be aware that characterizing with sine signals is necessary but not sufficient. I believe to be published in TBCAS, experiment in a biomedical setup close to the real application is compulsory. The authors should at least demonstrate the GFET and the ROIC when combined can read out playbacks of pre-recoded ECoG signals through the solution.

Thanks for highlighting this missing test. Following your request, ROIC headstage measurements of synthesized μECoG signals have been added to Section IX (p. 12, Fig. 23 and par. 2).

2. Regarding the noise of the device, I appreciate that the authors added more clarifications in this revision and added a relevant citation (Chiang, 2020). In fact, the paper the authors cite clearly mentioned the 58 uVrms noise is very high and is a major limitation. Merely comparing with that paper does not justify the noise performance of this work. For example, the multiplexed ECoG reported in [75] (Uehlin, TBCAS 2020) already achieved way better noise, which conforms to the 1 5uVrms typical noise requirement in ECoG recording (see S. Ha et al., "Silicon-Integrated High-Density Electrocortical Interfaces," in Proceedings of the IEEE, vol. 105, no. 1, pp. 11-33, Jan. 2017, doi: 10.1109/JPROC.2016.2587690.).

Thanks for your comments. There is a clear trade-off between scalability and noise performance, which has been discussed in Sections III and V. For this reason, we understand that noise comparisons should be done on a channel count basis. In this sense, the state-of-art multiplexed system [90] with 1008-ch and 58-μV figures is comparable to the presented work, as highlighted in Section II (p. 2, par. 4). Conversely, reference [75] is limited to 64 channels only and it employs a point-to-point connectivity between each recording site and the ROIC frontend circuit, so it is definitely not suitable for large scalability. Reference [90] is not included in the comparison of Table II since its read-out electronics are not integrated in a ROIC.