Comparison of OFF-State, HCI and BTI degradation in FDSOI Ω-gate NW-FETs

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1. Abstract

In this work, the degradation of N-type FDSOI Ω-gate NW-FETs caused by OFF-State stress under different conditions has been experimentally studied and compared with the effects of positive/negative BTI and HCI aging. The experimental observations show that HCI and OFF-State are the most damaging aging mechanisms in these devices while N/PBTI produce negligible degradation. Moreover, for large enough stress conditions, OFF-State aging largely distorts the I_D-V_G curves of the transistor, leading to an almost linear dependence on V_G.

2. Introduction

Device degradation caused by Bias Temperature Instability (BTI) or Hot Carrier Injection (HCI) is still relevant in deeply scaled CMOS technologies [1-6]. The changes introduced into the dielectric and/or channel properties reduce the device reliability and, therefore, the circuit performance and lifetime [7]. In the last years, the interest in the degradation induced by an OFF-state stress has grown and reported [8-10], showing the importance of accounting for the diverse biasing configurations that FETs may experience when they operate in digital circuits such as CMOS inverters or logic gates [11-13]. In this work, the impact of the OFF-state degradation in short channel FDSOI transistors (Fully-Depleted Silicon On Insulator) N-type FDSOI Ω-gate Nanowire transistors (NW-FETs) [14] under different stress bias conditions is studied. Moreover, the impact of negative/positive BTI and HCI degradations are also experimentally studied and compared to that linked to the OFF-state degradation. Finally, the OFF-state ON and OFF Drain Current degradation dependence on the stress voltage and stress time were analyzed.

3. Device description and measurement procedure.

The FDSOI N-type Ω-gate NW-FETs studied in this work were fabricated at CEA-LETI [15] and had a high-K Ω-Gate (HfSiON/TiN) with EOT=1.3nm, H_{NW}=11nm and a buried oxide thickness of 145nm (Fig. 1). Devices were fabricated using a multi-finger structure, with W=300nm splitted in 10 fingers and had L=20nm.

To analyze the impact of the N/PBTI, HCI and the OFF-State degradations, different experiments were carried out. For BTI, both biasing, negative and positive, were analyzed applying the stress voltage (2.4Volts) to the gate terminal while source, drain and back-gate terminals were grounded (as shown in Fig. 2). For HCI, the worst case was considered (i.e., V_G=V_D), so that the stress voltage (2.4Volts) was applied to the gate and drain terminals, while source and back gate were grounded. For OFF-State, the stress voltage was applied to the drain terminal, keeping the rest of terminals grounded. In this case, the stress voltage was varied from 1.7V to 2.5V. A Measurement-Stress-Measurement sequence was used, so that the stress sequence was interrupted to evaluate the stress impact and its time evolution by measuring the I_D-V_G curves of the stressed devices.

4. Results and Discussion.

Fig. 3 shows the I_D-V_G curves of fresh devices (black line) and after 1500s (red circles) of (from left to right) OFF-State, NBTI, PBTI and HCI stress at 2.4Volts in linear scale (top) and log scale (bottom). For the fresh devices short channel effects are evidenced by the large drain current (I_D) in the subthreshold region and the small threshold voltage (~0.25V). For the PBTI and NBTI stresses, no significant changes on the I_D-V_G curves can be appreciated beyond a small reduction of $I_{D\text{-}ON}$ (current at V_G = 1.2V). However, for HCI and OFF-State the consequences of the stress are clearly

observed. For the HCI, there is a large increase of the threshold voltage (~1V) and the mobility is strongly reduced. Therefore, the damage that $I_{D\text{-}ON}$ experiences (~90% reduction) is so detrimental (the largest, when compared to the other stress cases). Note that, though the I_D-V_G characteristic is extremely modified, the subthreshold and linear regions are still distinguishable. In the case of the OFF-State stress, for this stress voltage, the changes in the curves are much dramatic. As in the case of the HCI stress $I_{D\text{-}ON}$ is large reduced, but the decrease is smaller (~50%). However, the subthreshold current increases significantly and the I_D-V_G characteristic is completely distorted being not possible to clearly identify the subthreshold region: I_D exhibits an almost linear dependence on V_G for large stress voltages (see Fig. 5).

In order to clarify how the NW-FDSOI transistors analyzed have been damaged by the different stresses shown in figure 3 the I_G-V_G characteristic was also analyzed. Figure 4 shows the I_G-V_G curves of the fresh devices (black line) and after 1500 seconds of 2.4V stress (red circles). As observed, for the PBTI and NBTI stresses the gate dielectric doesn't suffer significant damage and the leakage current remains around 10pA (fresh value). However, for the HCI and OFF-State stresses larger affectations on the isolation properties of the device dielectric can be observed after the stresses, increasing sustancialy the leakage current through the gate dielectric to 1μA at V_G=1V. The results on both, N/PBTI and HCI/OFF-State clearly indicates that high current densities are the main cause of the dielectric aging, but not the high electric fields also present during N/PBTI stresses.

Because the large I_D-V_G distortion caused by the OFF-State degradation, threshold voltage and mobility are not useful parameters to quantify the device degradation. Therefore, $I_{D\text{-}OFF}$ (i.e., I_D @ V_G = 0V) and I_{ON} (i.e I_D @ V_G = 1.2V) were used as parameters with this purpose. Figure 4 shows the relative $I_{D\text{-}ON}$ and $I_{D\text{-}OFF}$ reduction suffered after OFF-State (blue triangles), PBTI (black squares), NBTI (red circles) and HCI (pink triangles) stresses. As observed in Fig. 3, Negative and Positive BTI produce the smallest variations on $I_{D\text{-}ON}$ (< 7% after 2000 seconds). On the other hand, HCI provokes the largest reduction of $I_{D\text{-}ON}$, mostly induced within the first 100 seconds of the stress, indicating that, in this technology, HCI is extremely harmful. Finally, for the OFF-State stress, $I_{D\text{-}ON}$ shift suffers a fast increase at the beginning of the stress and then evolves smoothly with the stress time from ~20% (after the first inspection at 80s) to ~50% after 2500s, also exhibiting a saturation effect for larger stress times. Concerning $I_{D\text{-}OFF}$, there is no change for N/PBTI, a large reduction for the HCI (~100%), but a large increase for the OFF-State case (~1000%, i.e., 10 times with respect the fresh $I_{D\text{-}OFF}$).

The stress voltage dependence of the OFF-State degradation has been also analyzed. Figure 5 shows some examples of the I_D-V_G curves measured after 2600s of stress for different stress voltages together with the fresh I_D-V_G. Note that $I_{D\text{-}ON}$ decreases respect of the fresh value being larger with the stress voltage applied during the OFF-State stress. On the other hand, $I_{D\text{-}OFF}$ and the subthreshold slope increases with the stress voltage being critical for the largest stress voltages (>2.3V). However, the observed $I_{D\text{-}OFF}$ degradation is very small for the lower stress voltages (1.7V to 2V). The combination of both degradations, $I_{D\text{-}ON}$/$I_{D\text{-}OFF}$ increase/decrease, extremely distorts the I_D-V_G characteristic, as previously highlighted in figure 3.

The temporal evolution, together with the voltage dependences, are further analyzed in Figure 6. For $I_{D\text{-}ON}$, as expected, the larger the stress conditions (voltage and time), the larger the $I_{D\text{-}ON}$ degradation, reaching a 60% reduction after 2600s at 2.5V. On the other hand, for $I_{D\text{-}OFF}$, only for large enough stress voltages/times, an increase is observed. However, $I_{D\text{-}OFF}$ is 30 times the fresh value, for the stress at 2.5V.

5. Conclusions

The degradation of N-type FDSOI Ω-gate NW-FETs induced by PBTI, NBTI, HCI and OFF-State stress was experimentally analyzed and compared. NBTI/PBTI have the smallest effect on the device performance, whereas HCI produces the largest $I_{D\text{-}ON}$ degradation, linked to a large increase/decrease of V_{TH}/μ. However, though the OFF-State stress induces a decrease of $I_{D\text{-}ON}$ smaller than for HCI, for large enough stress conditions (voltage/time), the large increase of the subthreshold current can lead to a complete distortion of the I_D-V_G characteristics and even to the loss of the device functionality. Furthermore, in both cases (HCI and OFF-State) the gate dielectric experiences a large degradation during the stress leading to large tunneling currents through the high-k based Ω-gate.

Acknowledgements

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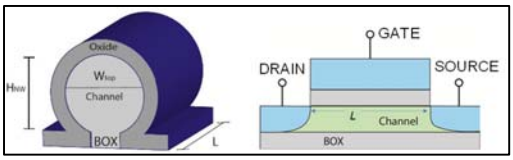

Figure 1. LEFT: 3D sckecht of the Ω-Gate architecture of the FD-SOI transistors (EOT=1.3nm, H_{NW}=11nm and Buried Oxide Thickness= 145nm). RIGHT: Cross-section of the FD-SOI transistors.

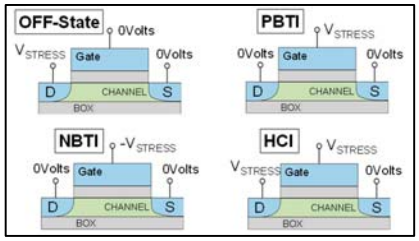

Figure 2. Biasing configurations for the study of the OFF-State, PBTI, NBTI and HCI degradations. The back-gate was always grounded.

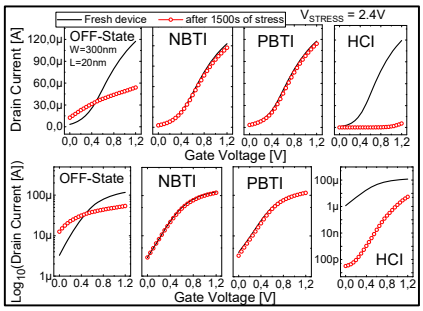

Figure 3. I_D-V_G curves (V_{DS}=50mV) of the fresh device (black line) and after 1500 seconds of 2.4V stress (red circles). Linear (top) and logarithmic (bottom) plots are shown.

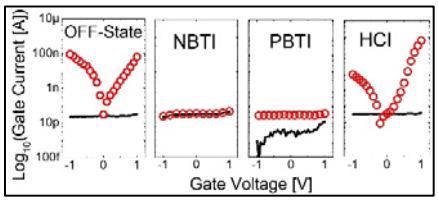

Figure 3-2. I_G-V_G curves of the fresh device (black line) and after 1500 seconds of 2.4V stress (red circles).

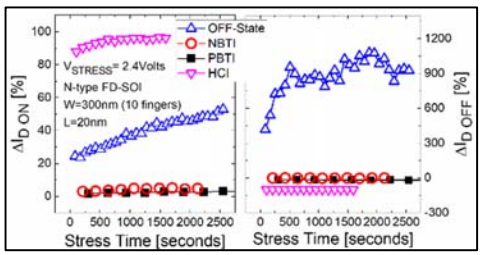

Figure 4. Relative $I_{D\text{-}ON}$ (left) and $I_{D\text{-}OFF}$ (right) variations for an OFF-State (blue triangles), PBTI (black squares), NBTI (red circles) and HCI (pink triangles) stresses at 2.4V, as a function of the stress time.

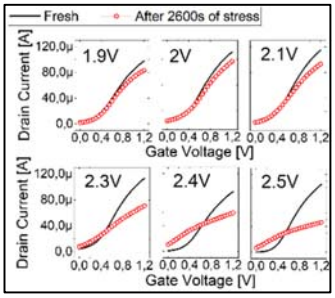

Figure 5. I_D-V_G curves (V_{DS}=50mV) of the fresh device (black line) and after 2600 seconds of OFF-State stress (red circles) at 1.9V, 2V, 2.1V, 2.3V, 2.4V and 2.5V.

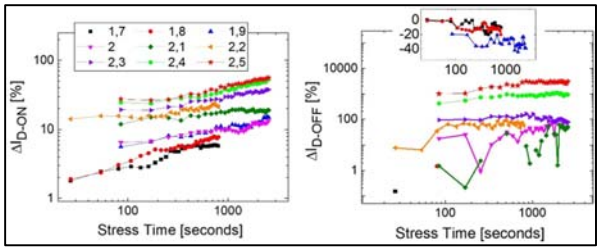

Figure 6. Relative variations of $I_{D\text{-}ON}$ (top) and $I_{D\text{-}OFF}$ (bottom) as a function of the stress time for OFF-State stresses at V_G ranging from 1.7V to 2.5V.