Real-time threshold voltage compensation on dual-gate electrolyte-gated organic field-effect transistors.

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Abstract

Electrolyte-Gated Organic Field-Effect Transistors (EGOFETs) offer many opportunities for the development of low-cost and low-power electronics suitable for applications like sensors and point-of-care tests; however, EGOFETs can be affected by the drift of their operative point that causes signals distortion and loss of information during sensing applications. Here, a blend of 2,8-Difluoro-5,11-bis(triethylsilylethynyl)anthradithiophene (diF-TES-ADT) and polystyrene (PS) is used as the active material for the fabrication of dual-gate EGOFETs. We exploited the dual-gate architecture to improve EGOFETs stability by implementing digital feedback that uses the back-gate electrode to compensate dynamically for the transistor threshold voltage allowing us to fix its operative point for prolonged tests (> 10 hours) with different aqueous solutions (Milli-Q water, NaCl 0.1M and a physiological solution). The presented real-time threshold voltage compensation does not only allow to steady EGOFETs DC output current, but it also preserves EGOFETs sensing capability for the detection of signals with frequencies as low as 1 Hz.

Keywords: organic electronics, electrolyte-gated organic field-effect transistors, dual-gate EGOFETs, electrolyte gating, threshold voltage compensation

1. Introduction

Since the pioneering works of Tsumura et al. [1] and Horowitz et al. [2] about the implementation of polymers and small molecules into a transistor, organic electronics have experienced exceptional breakthroughs in terms of well-suited organic semiconductors (OSCs) [3] and customized architectures that comply with the stringent requirements of different fields of applications such as portable and/or flexible devices, hand-held ones, sensors, and neural interfaces [4,5].

A particularly interesting branch of organic electronics consists of transistors operating in aqueous environments that can be coupled with physiological relevant solutions allowing the transduction of (bio-)chemical events. This large class of transistors, generically termed water-gated organic transistors, can be divided into two families: organic electrochemical transistors (OECTs), and electrolyte-gated organic field-effect transistors (EGOFETs). OECTs are typically made by using conducting or semiconducting polymers and their working principle relies on the electrochemical doping of the semiconducting film [6]. Conversely, EGOFETs usually employ non-permeable semiconducting small molecules like pentacene and its derivatives where, similarly to a conventional field-effect transistor, a two-dimensional electronic channel forms at the interface with the aqueous medium that plays the role of the dielectric in the metal-insulator-semiconductor architecture. Therefore, current modulation in OECTs is achieved by a massive permeation of ions into the organic layer, whereas it is induced by capacitive coupling in EGOFETs [7]. For this reason, EGOFETs usually feature larger electrochemical stability and faster switching speed than OECTs; furthermore, they can also operate with Milli-Q water, which is a clear advantage to study their working mechanisms while preserving the semiconductor from the undesired percolation of ions [8].

Despite these properties, EGOFETs based on small molecule organic semiconductors cannot be defined as reliable yet, since they typically exhibit a constant current drift during prolonged measurements [9]. From an engineering point of view, such current drift reflects a shift of the transistor operative point, with a direct consequence on the value of the current signal during analog applications. For instance, during the recording of cellular activities, *e.g.* cells' action potentials (APs), in which EGOFETs can be used as sensors translating input APs signals into output currents signals (i.e. drain-to-source current), the shift of the transistor operative point would slowly affect the recording introducing signal distortions.

In this framework, it is essential to implement a compensation mechanism capable of stabilizing EGOFETs operative point. Regarding standard electrochemical sensors, the shift of the DC operative point is often caused by capacitive fluctuation, temperature drift, and variation of the analyte concentration, and it is typically fixed by using a potentiostat in a three-electrode cell configuration [10,11], or by adjusting the operative bias in voltage controllable capacitive sensors [12]. Concerning solid-state transistors, the major cause of drift is a shift in the threshold voltage (V_{th}). This requires mandatorily the development of compensation circuitries able to control periodically the transistor gate voltage in order to drive a constant current (*e.g.* thin-film-transistors pixel drivers for AMOLED displays) [13,14]. The performance of such circuitries can be significantly improved by exploiting dual-gate TFTs that allow reducing the compensation time below 10 μs [15]. Moreover, dual-gate architectures can be coupled with separated compensation circuits, thus allowing real-time

compensation of the TFT V_{th} during operation [16]. This is an extremely interesting and unexplored scenario for EGOFETs, especially in the framework of biological sensing, where continuous and stable monitoring of cells activity is required. Furthermore, dual-gate EGOFETs have been already demonstrated to enable the tuning of the device V_{th} in order to improve sensing of cells activity [17].

Here, we exploit the chemical robustness of the diF-TES-ADT:PS blend along with the support of an additional gate electrode to demonstrate real-time compensation of the transistor operative point in dual-gate EGOFETs. The dual-gating does not only allow us to extract the capacitance of the OSC/water interface, but also to exert a higher control on prolonged measurements (> 10 hours) with no electrical drift and/or clear deterioration of the semiconducting material. This has been successfully achieved by using dynamic control of the back-gate voltage, which affords to select of a well-defined output signal while preserving the sensing capability of the device that we demonstrated by superposing slow AP signals to the DC water-gate bias.

2. Materials and Methods

2.1. Substrate fabrication

The substrate of choice is silicon (purchased from Si-Mat, p+ doped, σ = 0.005 – 0.02 Ωcm), whose thickness is 525(±25) μm, and it is covered by a thermally-grown SiO_2 (nominal thickness 200 nm). The transistor layout was drawn using CAD. The photolithography entailed the following steps: i) spin-coating of a positive photoresist (Shipley S1813); ii) light exposure by using the Micro-Writer ML3; iii) photoresist development (Shipley Microposit MF-319). The Cr/Au (5 nm/40 nm thick, respectively) electrodes were evaporated by means of the Metal Evaporator System Auto 306. The final lift-off was performed by using acetone. Concerning the overall geometry of the transistor, the channel length (*L*) and width (*W*) were chosen equal to 30 μm and 8476 μm (i.e. *W/L* ratio equal to 282), respectively. Further details can be found in the supporting information (Figure S1).

2.2. Organic semiconductor deposition

The substrates were activated by using UV Ozone cleaner for 25 min, and afterwards, they were immersed in a solution of 2,3,4,5,6-pentafluorothiophenol (PFBT, 2 μL/mL in isopropanol) for 15 minutes [9]. Then, the substrates were further rinsed with isopropanol and dried using nitrogen.

Prior to the OSC deposition, a thick layer of dextran (*i.e.* drop-casted from a dextran solution 10 mg/mL) was deposited on the areas that had to be not covered by the OSC thin-film, such as the coplanar gate electrode and contact PADs [18,19].

The deposition method is the so-termed “Bar-Assisted Meniscus Shearing” (BAMS) [20], Shortly, a blend of 2,8-Difluoro-5,11-bis(triethylsilylethynyl)anthradithiophene (diF-TES-ADT) and

polystyrene (Mw = 10000 g/mol) was dissolved in chlorobenzene 2% wt. with a ratio 4:1 (diF-TES-ADT:PS). The solution was deposited at 10 mm/s at 105°C as previously reported. Finally, the silicon substrate was immersed in bi-distilled water to remove the dextran coating.

The whole characterization of the diF-TES-ADT has been performed by using the following techniques: i) optical polarized microscopy (Figure S2); ii) atomic force microscopy (Figure S3); iii) X-ray diffraction (Figure S4) and iv) time-of-flight secondary ion mass spectroscopy (Figure S5). This multi-methodological approach allowed us to verify homogeneity, thickness, anisotropy, crystallinity and vertical phase separation of the semiconducting thin-film.

The thickness has been characterized by using 5100 SPM system from Agilent Technologies and subsequent data analysis was done using Gwyddion software (http://gwyddion.net/), as shown in Figure S3. The overall homogeneity and anisotropy of the thin film have been checked by an optical microscope (Olympus BX51) equipped with polarizer and analyzer (Figure S2). The crystallinity of the thin film has been analyzed by using a PANalytical X'PERT MRD system (Figure S4).

According to Temiño et al. [20], diF-TES-ADT blended with PS undergoes a vertical phase separation, where most of PS (approx. 10 nm thick) is sandwiched between the SiO_2 and the OSC crystalline layer. Therefore, the back-gate capacitance is given by the in-series capacitances related to the SiO_2 (200-nm thick) and PS (10-nm thick), resulting in an overall capacitance of 16 nF/cm^2. This has been verified by checking the vertical chemical composition of the thin film by using time-of-flight secondary ion mass spectrometry (ToF-SIMS). In particular, the surface sputter etching of the surface was accomplished with Cs^+ beam, over a 300 µm × 300 µm area using 1 keV energy settings raster. A pulsed beam of 25 keV Bi(1) ions scanned over a 50 µm × 50 µm region centered within the sputtered area was used. The analysis cycle time was 100 µs and the sputtering cycle was 1.6 s and 500 ms flood gun compensation. A high current beam of low energy (<20 eV) electrons was employed for charge compensation, and negative ions were analyzed (Figure S4).

2.3. Characterization procedures

The whole batch of electrical characterizations has been performed in dark using an Agilent B1500 parameter analyzer equipped with two high-power and two high-resolution source measurement units (SMUs).

Concerning the Back-Gate measurements (i.e. without the liquid medium on top of the device): i) Quasi-Static (QS) $I_{DS}V_{DS}$ output characteristics were taken by scanning V_{DS} from 0 V to –10 V with a constant V_{BG} = –10 V and a scan rate of 1 V/s; ii) *QS-*$I_{DS}V_{BG}$ transfer characteristics were taken by scanning V_{BG} from +5 V to –10 V with a constant V_{DS} = –10 V and a scan rate of 1 V/s; iii) *Pulsed-*$I_{DS}V_{DS}$ output characteristics were taken by scanning V_{DS} from 0 V to –10 V while V_{BG} is pulsed from 0 V to –10 V for each measurement point with a period of 110 ms and a pulse width of 10 ms (Figure

S2); iv) *Pulsed-$I_{DS}V_{BG}$* transfer characteristics were recorded by scanning V_{BG} from +5 V to –10 V in a pulsed fashion while keeping a constant V_{DS} = –10 V. For each measurement point, V_{BG} is pulsed from 0 V to its measurement values with a period of 110 ms and a pulse width of 10 ms.

Regarding the Top-Gate characterizations (*i.e.* devices operated in the liquid medium by using the coplanar gate electrode, whereas the back-gate is fixed to 0 V), $I_{DS}V_{DS}$ (quasi-static) output characteristics were recorded by scanning V_{DS} from 0 V to –500 mV with constant V_{TG} = 0 V, –250 mV, –500 mV and a scan rate of 50 mV/s. Furthermore, $I_{DS}V_{TG}$ (quasi-static) transfer characteristics were taken by scanning V_{TG} from +200 mV to –500 mV with constant V_{DS} = –50 mV, –500 mV, and a scan rate of 70 mV/s.

Dual-gate (DG) characterizations have been performed as follows: *DG-$I_{DS}V_{TG}$* transfer characteristics were taken by scanning V_{TG} from 200 mV to –500 mV with a constant V_{DS} = –500 mV and a scan rate of 70 mV/s. Each transfer curve was repeated at a different value of V_{BG} that ranges from 0 V to +50 V.

Lastly, Current vs Time (I-time) measurements, as well as the dynamic V_{th} compensation, were performed by means of two Agilent E5263A, both equipped with two high-speed SMUs. The two instruments (*viz.* Agilent E5263A) were remotely controlled by a Desktop Computer by using Matlab®. During the I-time measurements, the EGOFETs are operated in a saturation regime, and the I_{DS} current is recorded with a sampling time T_S = 200 ms for as long as 11 hours (Figure S6). The whole test consists of using constant biases, namely V_{DS} = -500 mV (V_S = 0 V), V_{TG} = –500 mV and –200 mV and V_{BG} was initially set either at 0 V or +5 V.

According to our experimental setup, we simultaneously measure the current flowing through all four terminals (*viz.* I_S, I_D, I_{TG}, I_{BG}). Hence, we verified that both the TG and BG leakage current (I_{TG} and I_{BG}) are much lower than the source and drain currents (see Figure 2), thus we can safely assume that $|I_S| = |I_D| = |I_{DS}|$. Thereafter, we will refer only to I_{DS} to indicate the drain-to-source current recorded either at the Source electrode or at the Drain electrode.

Regarding the electrical characterization of EGOFETs, three types of liquids have been selected: i) Milli-Q water, ii) 0.1M NaCl and HeLA solution. The first liquid allowed us a standard characterization, namely our internal benchmark, whereas the other two liquids offer a relevant number of ions involved during the EGOFET operation. In particular, HeLA solution is composed of the following components: i) NaCl 150 mM, ii) KCl 5 mM, iii) $CaCl_2$ (anhydrous) 2 mM, iv) $MgCl_2$-$6H_2O$ 1 mM, v) sodium pyruvate 2 mM, vi) 4-(2-hydroxyethyl)-1-piperazineethanesulfonic acid (HEPES) 10 mM, vii) glucose 5 mM and viii) NaOH aliquots are used to adjust the final pH.

2.4. Dynamic threshold voltage compensation

To dynamically compensate the EGOFETs V_{th}, digital feedback has been set up, whose input data is the I_{DS} value (namely, the output signal of our device recorded at the source electrode), and it affords the dynamic control of the back-gate (*viz.* V_{BG}) in order to fix the I_{DS} at a value of interest. We set a target current value, I_{DS}^{*}, that corresponds to the output current at a given device working bias. Moreover, two control variables have been defined such as ΔI and ΔV.

Within the time scale of the I-time plot, the digital control acts on $V_{BG}(t + T_S)$ fulfilling this rule:

$$\begin{cases} if\ |I_{DS}(t)| < |I_{DS}^{*}| - \Delta I \quad then\ V_{BG}(t + T_S) = V_{BG}(t) - \Delta V \\ if\ |I_{DS}(t)| > |I_{DS}^{*}| + \Delta I \quad then\ V_{BG}(t + T_S) = V_{BG}(t) + \Delta V \\ \qquad\qquad V_{BG}(t + T_S) = V_{BG}(t) \quad otherwise \end{cases} \tag{1}$$

in other terms, every time $|I_{DS}|$ decreases below the given threshold $(|I_{DS}^{*}| - \Delta I)$, V_{BG} becomes more negative, so increasing the $|I_{DS}|$ current. Vice versa, if $|I_{DS}|$ increases (above the given threshold $|I_{DS}^{*}| + \Delta I$) V_{BG} becomes more positive, thereby reducing the $|I_{DS}|$ current. In such a way, the EGOFET I_{DS} current can be fixed at an arbitrary value.

3. Results and Discussions

3.1. Electrical characterization of the back-gate and top-gate conductive channels

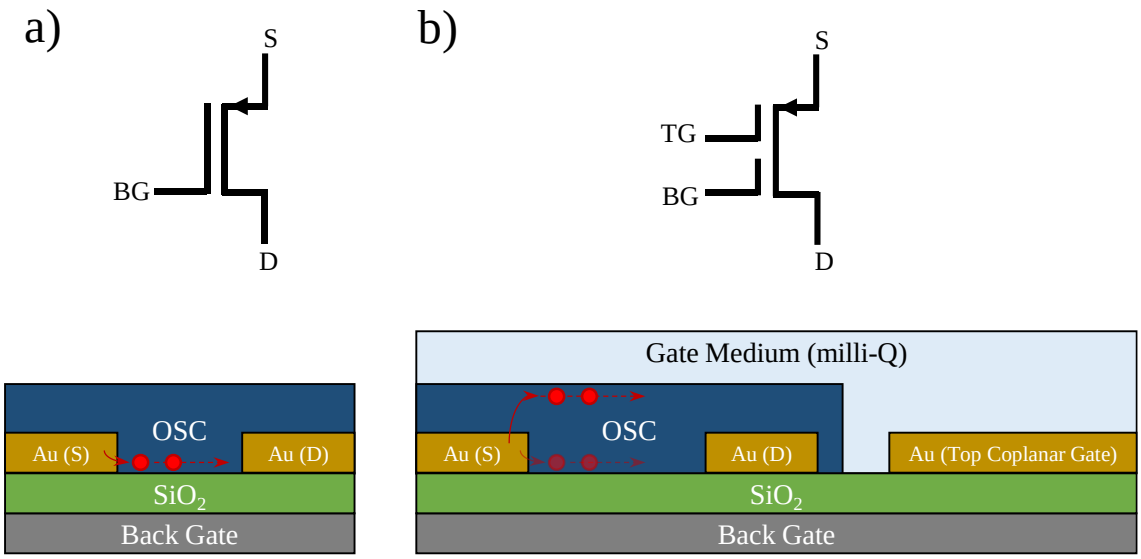

Figure 1 a) Back- and **b)** dual-gate configuration of the transistor of interest.

Although this manuscript is mainly focused on the dual-gate operation of diF-TES-ADT:PS based EGOFETs, a complete characterization of this semiconducting blend has been assessed by using different techniques before any electrical measurement (see Experimental Section 6.2 and Supporting Information Figures S3, S4, S5 and S6).

Concerning the electrical characterization of the diF-TES-ADT:PS EGOFETs, we decided to characterize separately the two conductive channels, namely the back-gate (*i.e.* located at the OSC/SiO_2 interface) and the top-gate (*i.e.* placed at the OSC/MilliQ water interface) ones (Figure 1). The former relies on the Back-Gate (BG) configuration of organic field-effect transistors (OFETs), whereas the latter relies on the standard configuration of EGOFETs, as shown in Figure 1a and Figure 1b, respectively. Firstly, quasi-static back-gate output and transfer characteristics (black dashed lines in Figure 2a and Figure 2b, respectively) have been recorded. A clear clockwise hysteresis is observed during *QS*-$I_{DS}V_{BG}$, suggesting that positive charges (*viz.* holes) are trapped at the SiO_2/OSC interface [21], thereby causing a negative V_{th} shift of the transistor threshold voltage that decreases the I_{DS} current during the electrical characterization. Our hypothesis is further corroborated by the *Pulsed*-$I_{DS}V_{BG}$ and *Pulsed*-$I_{DS}V_{DS}$ characterizations, where a pulsed gate voltage is used instead of a *QS* one. According to Petit *et al.* [22], such a strategy allows for an alternate trapping period (V_{BG} value at the corresponding measurement point) with a de-trapping period (V_{BG} = 0 V), thus keeping the OSC in a charge neutrality-like state in which the effect of charge trapping becomes negligible. This leads to hysteresis-free I-V characteristics, as well as to a more efficient modulation of the I_{DS} current (solid red lines in Figure 2a and Figure 2b).

Conversely, the same device exhibits negligible hysteresis during quasi-static Top-Gate (TG) characterizations (with no need for pulsed measurements), suggesting a predominant field-effect behavior typical of EGOFETs [7], in which there are no evident signs of charge trapping or extensive electrochemical doping in both Milli-Q water and 0.1 M NaCl.

From the data reported in Figure 2, we can therefore assume that the current-voltage relationship for both the Back-Gate and the Top-Gate configurations can be described by the equations of a classic p-type field-effect transistor:

$$I_{DS} = \begin{cases} -\frac{W}{L} C_i \mu_{FET} \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right] & Linear\ regime \\ -\frac{1}{2} \frac{W}{L} C_i \mu_{FET} (V_{GS} - V_{th})^2 & Saturation\ regime \end{cases} \quad (2)$$

where μ_{FET} is the field-effect mobility, V_{th} is the transistor threshold voltage, V_{GS} is the gate-to-source voltage (equal to either V_{BG} or V_{TG}; V_S = 0 V), and C_i is either the back-gate capacitance C_{BG} = 16 nF/cm^2 (see experimental section) or the top-gate capacitance C_{TG}.

Therefore, we extrapolated both V_{th} and μ_{FET} from the saturation region of the transfer characteristics by applying equation (2), *i.e.* V_{th} = –0.85 V and μ_{FET} = 0.33 cm^{2}V^{-1}s^{-1} (V_{BG} = –10 V) for the back-gate configuration, whereas they are V_{th} = –116 mV and μ_{FET} = 0.04 cm^{2}V^{-1}s^{-1} (V_{TG} = –500 mV) for the top-gate configuration (C_{TG} = 4.6 µF/cm^2).

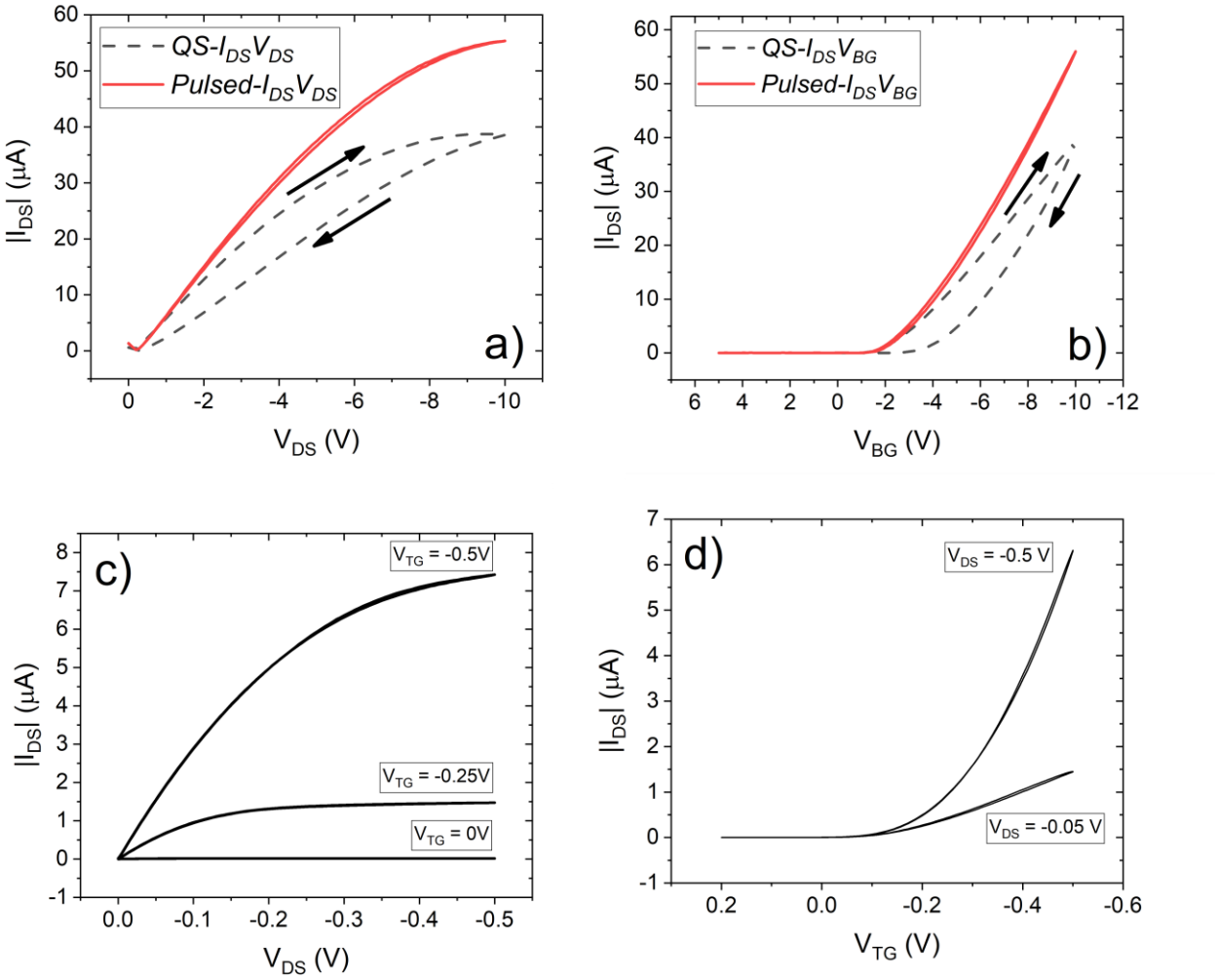

Figure 2 a), b) I-V output and transfer characteristics related to the back-gate configuration, where V_{GS} = -10 V and V_{DS} = -10 V respectively. The black arrows show both the forward and backward scans. **c), d)** I-V output and transfer characteristics related to the top (coplanar) gate configuration.

3.2. Dual-Gate characterization

According to these electrical characterizations, our EGOFETs can be effectively operated in a dual-gate mode, *i.e.* both the Back and the Top gates can be used simultaneously to control the I_{DS} current. In such a configuration, the coplanar gate acts to polarize the top-gated channel, and the back-gate polarizes the back-gated one. The choice of a printed coplanar gate instead of a metal wire placed manually into the droplet makes the device layout more compact and reliable, because it avoids a certain extent of variability due to the gate area directly immersed into the droplet (Figure S1) [23]. The simultaneous use of the two gates does not only exert a more efficient tuning of the transistor current but also enables the extraction of the top gate capacitance (C_{TG}). Aiming at this purpose, a

positive operative V_{BG} range has been selected (0 V < V_{BG} < +50 V), where no free carriers should be accumulated at the back-gated channel (*i.e.* the back-gate OFET is in an OFF state), whereas the top gate voltages are the same used for the previous characterization (0.2 V < V_{TG} < -0.5 V). In particular, an I-V transfer has been recorded for each step of the V_{BG} (namely, from 0 V to +50 V with a step of 5 V), as shown in Figure 3a and Figure 3b. Since the back-gate does not switch on the back-gate channel, its electric field is not screened, hence the top-gate channel can be simultaneously tuned by the V_{TG} together with the V_{BG} [24].

The EGOFET dual-gate operation in the saturation regime can be described by the following equation:

$$I_{DS} = -\frac{1}{2}\frac{W}{L} C_{TG}\mu_{FET}\left(V_{GS} - V_{th0} + \frac{C_S}{C_{TG}}V_{BG}\right)^2 \quad (3)$$

Where $C_S = \left(\frac{1}{C_{BG}} + \frac{1}{C_{OSC}}\right)^{-1}$ is the equivalent in-series capacitance, namely the back-gate capacitance, C_{BG}, coupled to the semiconductor capacitance, C_{OSC}, and V_{th0} is the threshold voltage for V_{BG} = 0 V [25]. Therefore, the EGOFET V_{th}, is dependent on the capacitance ratio C_S/C_{TG} and V_{BG} as follows:

$$V_{th} = V_{th0} - \frac{C_S}{C_{TG}}V_{BG} \quad (4)$$

where V_{th} is expected to show a linear dependence on the applied V_{BG} (Figure 3c). Higher V_{BG} values lower the I_{DS}, according to the p-type behavior of diF-TES-ADT.

The slope of this trend gives us a C_{TG} value equal to 4.6 μF/cm^2, which is coherent with previous values extracted by using electrochemical impedance in a similar architecture [9]. Such calculation has been performed within a narrower V_{BG} range (from 0V to +30 V) because V_{BG} beyond 30 V can cause the accumulation of electrons at the SiO_2/OSC interface, thereby partially screening the electric field induced by V_{BG}, thus reducing its modulation of the EGOFET threshold voltage V_{th} [26]. Furthermore, the electric field across the 200-nm thick SiO_2 (back-gate dielectric) becomes larger than 1.5 MV/cm. At such high voltages, electron tunnelling can occur through SiO_2 thereby causing the release of hydrogen, which yields in the formation of new interface states as well as other localized

defects [27], explaining both the turnaround of the subthreshold slope in Figure 3b and the faster decrease of the EGOFET field-effect mobility as highlighted by the two slopes in Figure 3d.

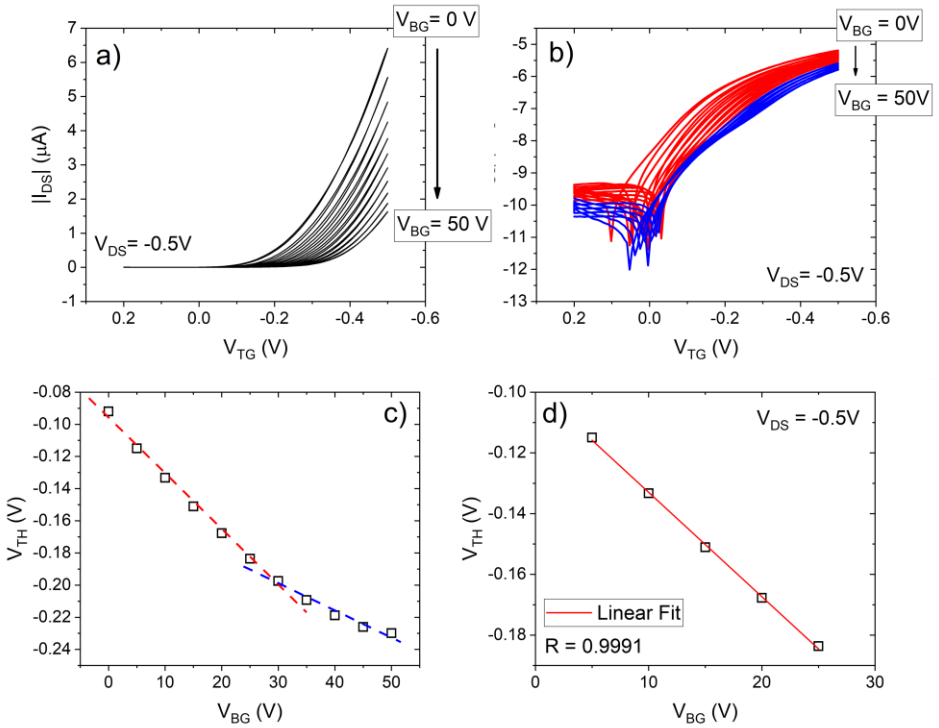

Figure 3 Dual-gate characterization: **a,b)** I-V transfer characteristics by sweeping the back-gate from 0 V to 50 V at steps of 5 V. Red curves are I-V transfer characteristics featuring 0 V ≤ V_{BG} ≤ 30 V **c)** Threshold voltage and **d)** mobility vs. back-gate voltage.

In addition, we also ruled out the possibility that high V_{BG} potentials could alter the electric field in the aqueous solution by monitoring the TG and BG leakage currents during all measurements. As reported in Figure S7, the top-gate leakage current does not increase with the increase of V_{BG}, confirming that the top-gate conductive channel can be approximated as a conducting lamina screening the electric field stemming from the BG.

3.3. Real-time V_{th} compensation

Among the possible applications, EGOFETs have been exploited as chemical and biochemical sensors [28,29]. These kinds of complex tests do not only require robust stability of the materials exposed directly to biological fluids but also to be operated at low voltages in order to avoid any redox interference towards the biological event. Both technological aspects are fundamental for these experiments because they usually last from minutes up to several hours (and some cases require days or even weeks). Although diF-TES-ADT based EGOFETs have achieved excellent results, their long-term stability is still an issue. For instance, such devices have been successfully used as electrical

transducers for cardiomyocyte cells activity [35], however, they are affected by an electrical drift for prolonged tests at constant bias [9].

In particular, the drain to source current, $I_{DS,}$ shows a continuous downward drift when driven by constant biases (Figure 4a). Two main reasons can give such a result: i) V_{th} and/or ii) μ_{FET} changes. According to our characterizations, we assume that the former is the main one responsible for this drift since slow charge trapping/de-trapping phenomena occurring at the BG interface can induce a V_{th} shift at the TG channel[30]. Aiming to clarify and solve this issue, we implemented the compensation feedback described in section 2.4 to mitigate this detrimental behavior (Figure 4b). This allows us to fix the desired I_{DS}, previously defined by simple I-V transfer characteristics, and to tune dynamically the EGOFET V_{th} through the back-gate of the transistor, thereby fixing the device operative point (constant I_{DS} in Figure 4c).

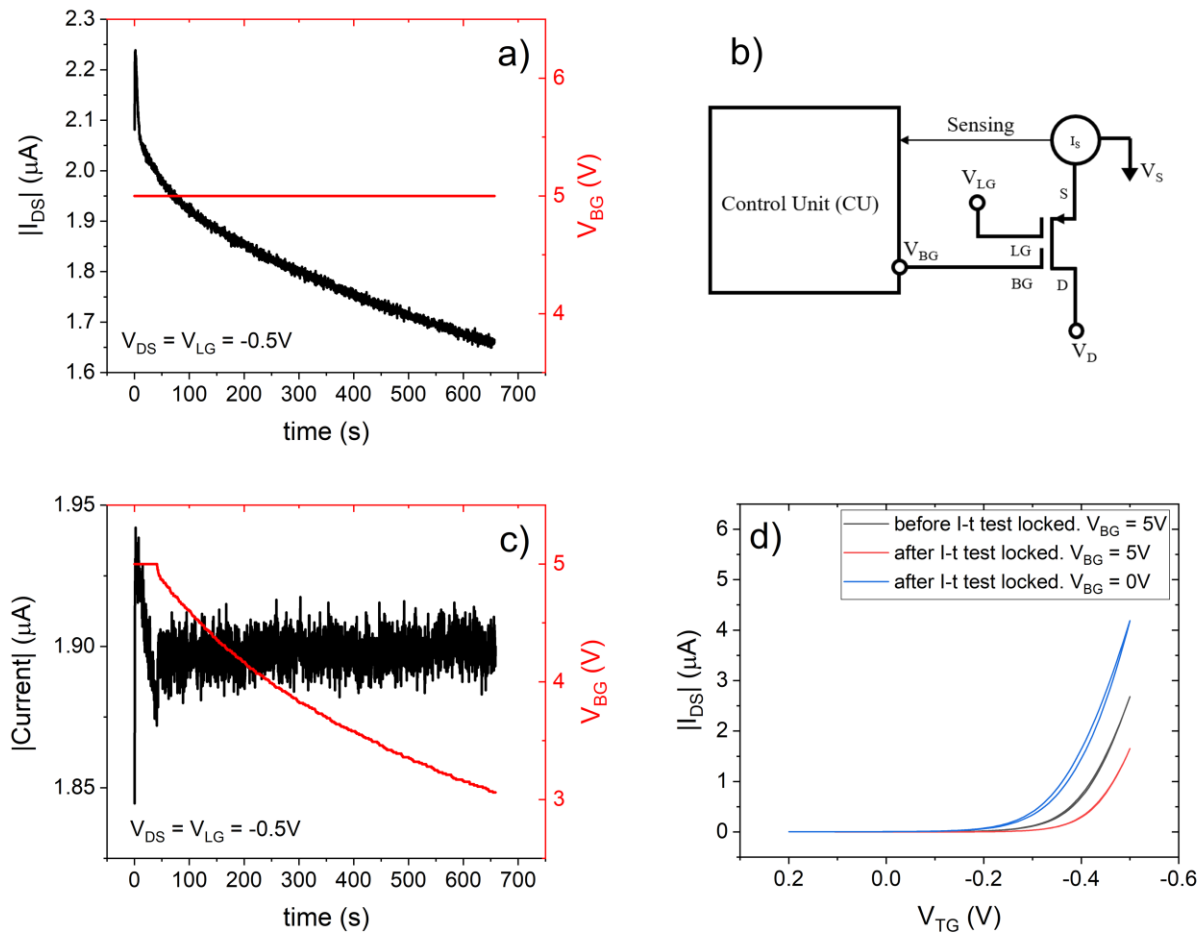

Figure 4 a) I vs. time with V_{BG} fixed at 5 V using MilliQ water as gate medium. **b)** Scheme of the back-gate feedback to keep the drain-source current fixed at an arbitrary value. **c)** Overlay of I_{DS} (black solid line) and V_{BG} (red solid line) vs. time, whose current is fixed at 1.9 µA using ΔI = 10 nA

and ΔV = 10 mV. **d)** Overlay of I-V transfer characteristics before (black solid line) and after the I-t test at V_{BG} equal to 5V and 0V.

It is important to notice that, in order to compensate for the current drift while preserving EGOFETs sensing capabilities, the compensation feedback should be optimized by tuning its design parameters. In particular, the feedback should be fast enough to compensate for the V_{th} drift, whereas it should act sufficiently slow to avoid overcompensating the input signals to be sensed. Consequently, such real-time compensation cannot be implemented for the detection of signals whose time constant is comparable to the drift of the device; however, it can extend the strength and application fields of EGOFETs in detecting relatively fast events like APs. Notably, the current drift reported in Figure 4a has a time constant within the range of 10 s - 100 s, therefore the dynamic compensation of dual-gate EGOFETs can allow detecting signals with frequencies larger than 0.1 Hz.

We validated this analysis by superposing to the top-gate DC bias a slow signal resembling the presence of APs with a characteristic frequency of approximately 1 Hz. AP signals were built starting from the Hodgkin-Huxley model [31] and applied to the EGOFET top-gate by means of a waveform generator (Rigol DG1022) every 10 s (Figure 5a). Figure 5b shows that, even though the input signal changes slowly (typical APs have characteristic frequencies around 1 kHz), our digital feedback is perfectly capable of compensating for the EGOFET current drift. It is clear that the information is preserved for every single recorded AP by exploiting the same operative condition.

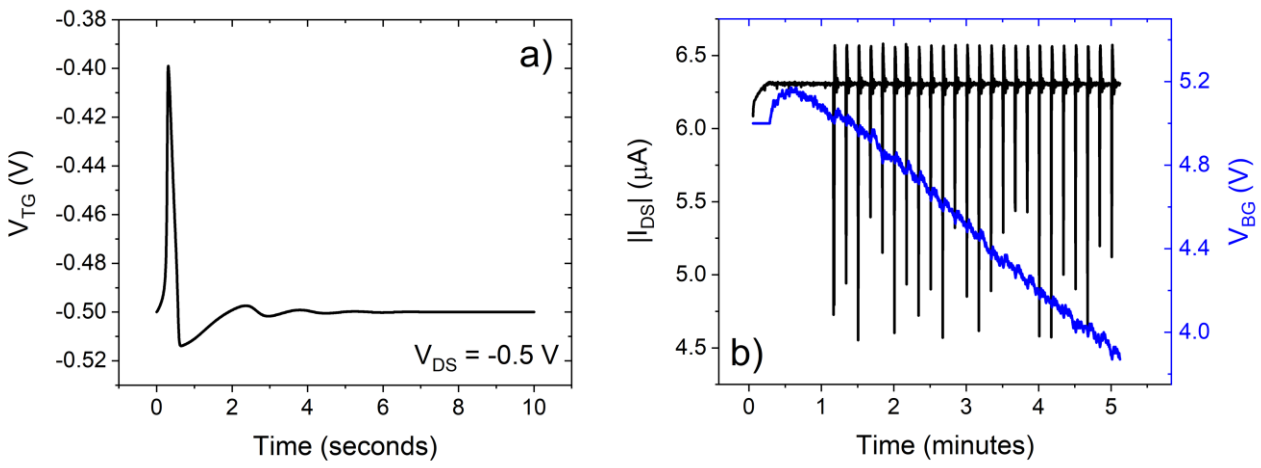

Figure 5 a) Emulated AP. **b)** Emulation of an APs train applied to our EGOFET (the different amplitude of the recorded APs is due to the low sampling rate of our setup).

For what concerns the V_{BG} range, we managed to use only positive values to guarantee the OFF state of the back-gate channel, therefore V_{BG} acts exclusively on the compensation of the EGOFETs V_{th}, which is the main cause of current drift. This allows us to successfully operate our transistor for prolonged tests. Furthermore, the overlay of the initial I-V transfer compared to the ones after the implementation of the digital feedback at different V_{BG} shows unambiguously that V_{th} is the main responsible for the above-mentioned drift (Figure 4d). No major degradation phenomena are taking place, because these I-V transfer characteristics are free of hysteresis and the back gating can still tune the charge carriers density: if one applies less positive V_{BG}, higher I_{DS} are recorded, coherently with the fact that our device is based on a p-type semiconductor. Such reasoning is also in agreement with the hysteretic back-gate characteristics discussed above (Figure 2a and Figure 2b). In fact, a source of negative V_{th} shift is due to positive charge trapping at the SiO_2/OSC interface. Such charge trapping does not induce only a change in the BG V_{th}, but also in the Top-Gate one, as demonstrated by the Dual-Gate operation of the device. Moreover, it is worth noticing that the trapping of positive charges at the SiO_2/OSC interface is not induced exclusively by the application of V_{BG}, but charge trapping and de-trapping phenomena are dependent also on the V_{TG} operation of the device. Therefore, one possible cause of long-term current drift in EGOFETs can be ascribed to the V_{th} shift induced by charge trapping at the interface between the organic semiconductor and the device substrate [30].
The hypothesis of OSC degradation is further ruled out by morphological analysis of the semiconducting layer before and after a prolonged electrical test (*i.e.* approximately 10 hours), hence no delamination or de-wetting phenomena have been observed (further details are presented in the Supporting Information, Figure S8).

To further demonstrate the efficacy of the proposed compensation, we repeated our experiments using the extracellular (HeLA) solution as a gate medium, thus emulating a more realistic scenario in which ion percolations and electrochemical doping can induce both positive and negative V_{th} shifts

as well as fluctuations in the field-effect mobility [7,32]. Figure 6 shows how our dual-gated devices operated *via* dynamic compensation can stabilize the EGOFET operative point for several hours even in the harsh environment provided by such an electrolyte. Similar experiments have been performed by testing different aqueous solutions (namely MilliQ water, NaCl 0.1 M, and HeLA solution) and different operative voltages (Figures S9). The control was always able to fulfil the goal of fixing the transistor operative point, thus proving to be excellent support even in those cases where very low voltages are required to prevent damaging or artefacts (*e.g.* damaging of tissues or unwanted redox reactions).

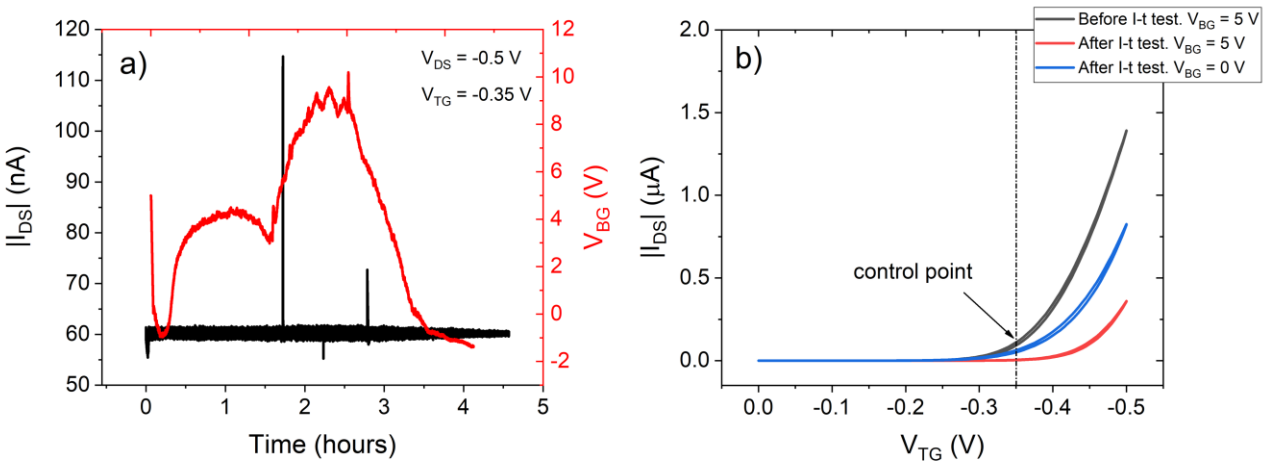

Figure 6 a) I-t test for 4.5 hours in saturation mode with ΔI = 100 pA and ΔV = 10 mV using HeLA solution as gate medium; **b)** I-V transfer before and after the I-t test at different V_{BG}. The dot-dashed line is a guide for the eye to highlight the operative point of the I-t plot.

4. Conclusions

In this work, we fabricated dual-gate EGOFETs employing diF-TES-ADT blended with PS as high-performing organic semiconducting material. The top-gating was achieved using a coplanar electrode that simplifies our experiments providing an easy and reliable way to contact the liquid-gate medium. Both conductive channels (*viz.* back-gate and top-gate channels) have been separately characterized, showing that, although the back-gate suffers from hysteresis due to charge trapping, the top-gate channel is free of hysteresis, which is a fingerprint of a well-performing EGOFET.

Despite the high performance, our devices suffer from an undesired current drift also during Top-Gate operation, limiting their usage because many applications require a stable operative point to avoid signal distortions and loss of information.

Since EGOFETs have been extensively used as (bio-)chemical transducers, we decided to empower their use by introducing digital feedback that counteracts charge trapping by acting on the device threshold voltage. As a result, we have demonstrated how the current drift can be removed, and the electrical stability preserved during long experiments even with strong electrolytes (> 10 hours).

The threshold voltage compensation allowed us to demonstrate how Dual-Gate EGOFETs can be operated stably for a prolonged time. However, for a real application (*e.g.* analog amplifier and bio-chemical sensing), the digital feedback must be designed considering the band frequency of the input signal to be detected to preserve its properties (namely signal shape and phase) in the output current (I_{DS}). To do so, the digital controller can be devised to act at lower frequencies than the characteristic frequencies of the input signal. A proof of concept has been provided by superposing AP signals to the top-gate DC bias, thus demonstrating that the compensation system presented in this manuscript can provide a stable operative point while allowing the detection of signals with characteristics frequencies larger than 1 Hz. Alternatively, a band-pass filter can be implemented to selectively remove the input signal frequencies from the control signal, allowing the design of fast and reliable compensations systems.

In conclusion, our approach shows the successful implementation of EGOFETs into long term experiments that require stable and reproducible recording of chemical and biological signals, thus extending the application fields of such devices.

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Supporting Information

Real-time threshold voltage compensation on dual-gate electrolyte-gated organic field-effect transistors.

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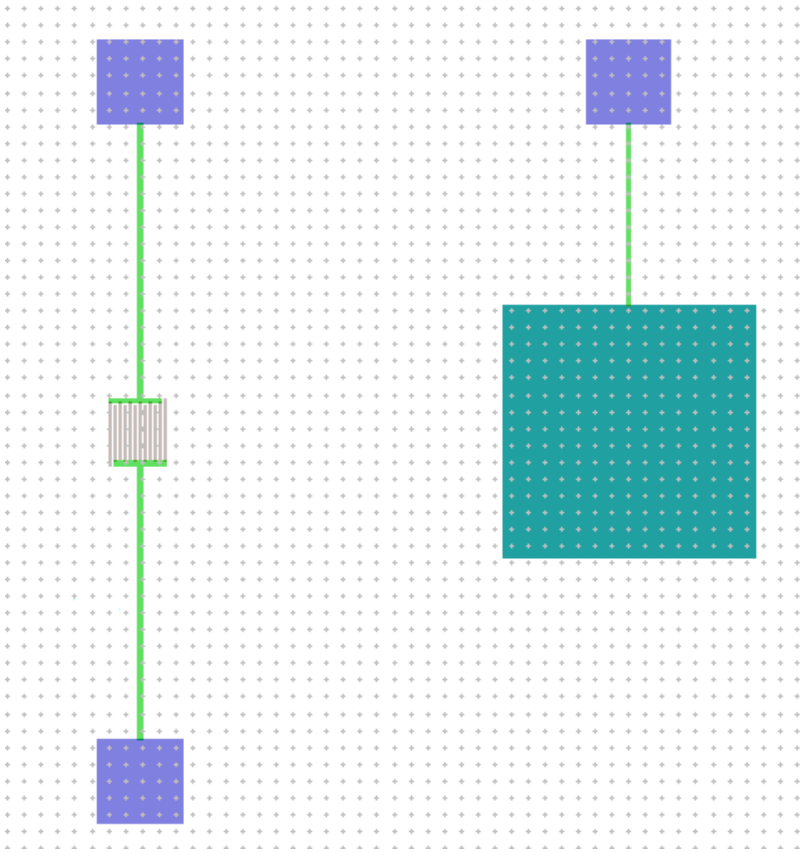

Figure S2 CAD drawing of the EGOT layout featuring the planar gate

Here the details of this layout:

1) Electrode gate area: 3x3 mm^2
2) Electrode width (fingers): 30 um

3) Channel length (*L*): 30 um
4) Number of fingers: 12
5) Channel width (*W*): 8476 um
6) Channel-gate ratio: 1:1000
7) Distance between gate electrode and interdigitated electrodes (IDEs): 4 mm
8) Distance between PADs and IDE: 3.2 mm
9) Distance between PADs and Gate electrode: 2.1 mm

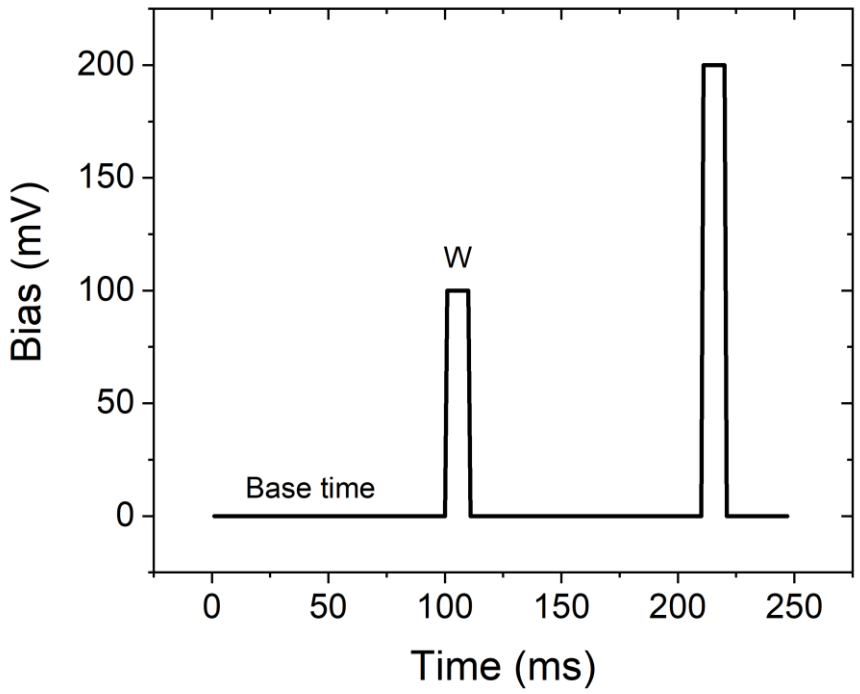

Figure S2 Voltage ramp for the Pulsed I-V characteristics

Figure S2 shows the standard pulsed protocol applied to the Pulsed I-V output and transfer characteristics. The base time is fixed at 0 V to keep the EGOFET in its resting state, and *W* is the gate pulse. The total period *T* is the sum of the base time plus the *W* equal to 110 ms. The *W* step is set around 100 mV.

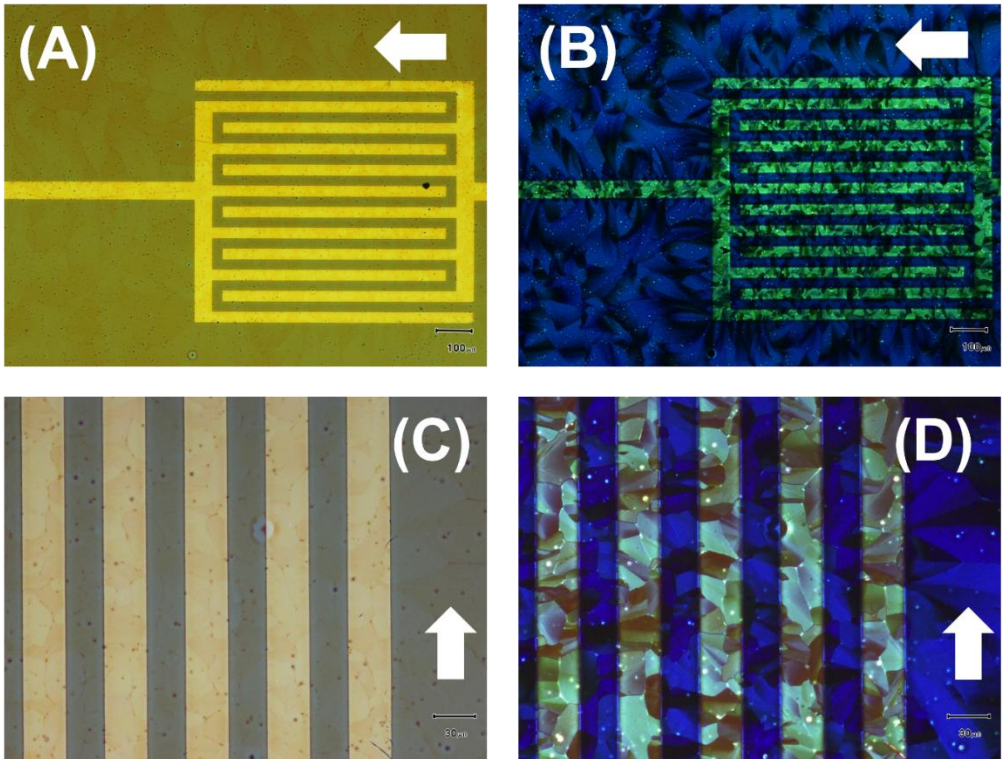

Figure S3 (A) Optical image of the interdigitated electrodes and, **(B)** the corresponding polarized image. **(C)** Magnification of the interdigitated electrodes and, the corresponding polarized image **(D)**. The white arrows show the shearing direction of BAMS.

Optical microscopy highlights the high grade of homogeneity of the thin-film. No cracks are visible at the macroscale both onto the silicon and the Au electrodes. The polarized images show the size of the crystallites coherent to what was previously published. Finally, the anisotropy is preserved, as highlighted by the white arrows in Figure S1.

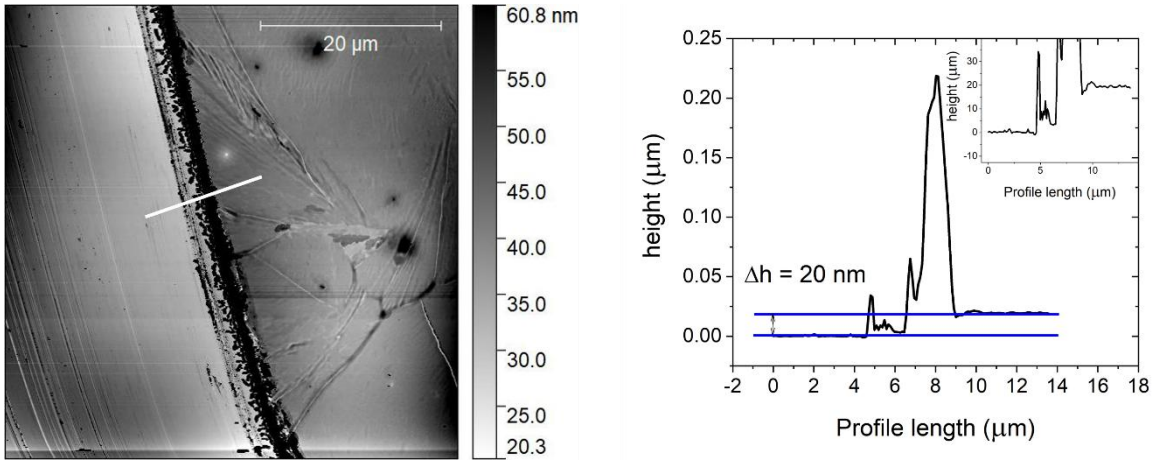

Figure S4 AFM image. On the left, the step of the diF-TES-ADT:PS thin film, where the white line represents a morphological profile. On the right, the height profile of the film border. The inset is a magnification of the profile related to the morphological step.

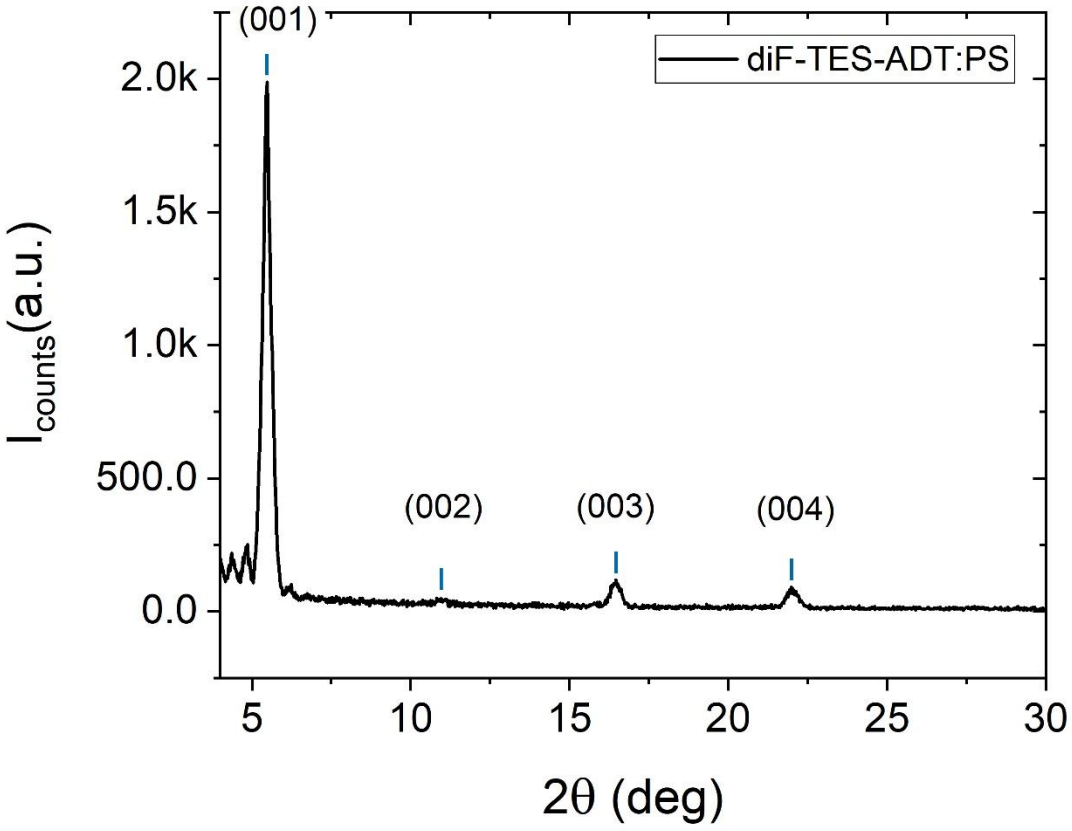

Figure S5 X-ray diffractogram of the diF-TES-ADT thin film.

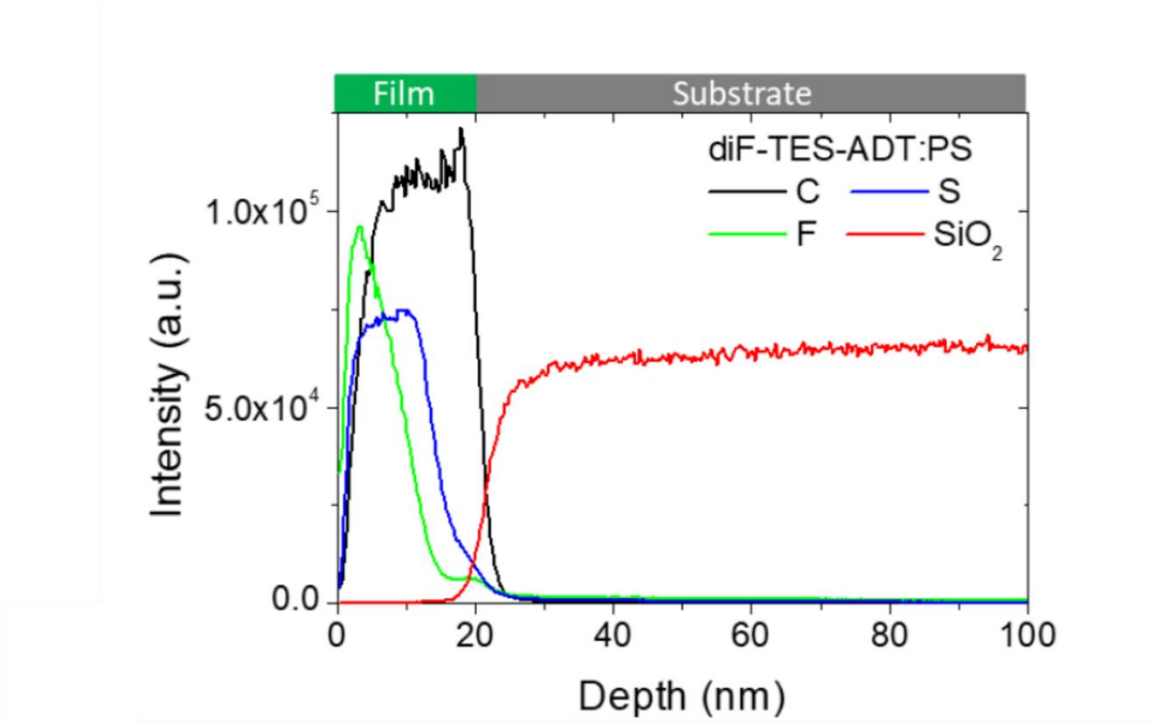

Figure S6 Depth profile of the diF-TES-ADT with respect to C (black), S (blue), F (green) and Si (red) recorded by using the time-of-flight secondary ion mass spectrometry.

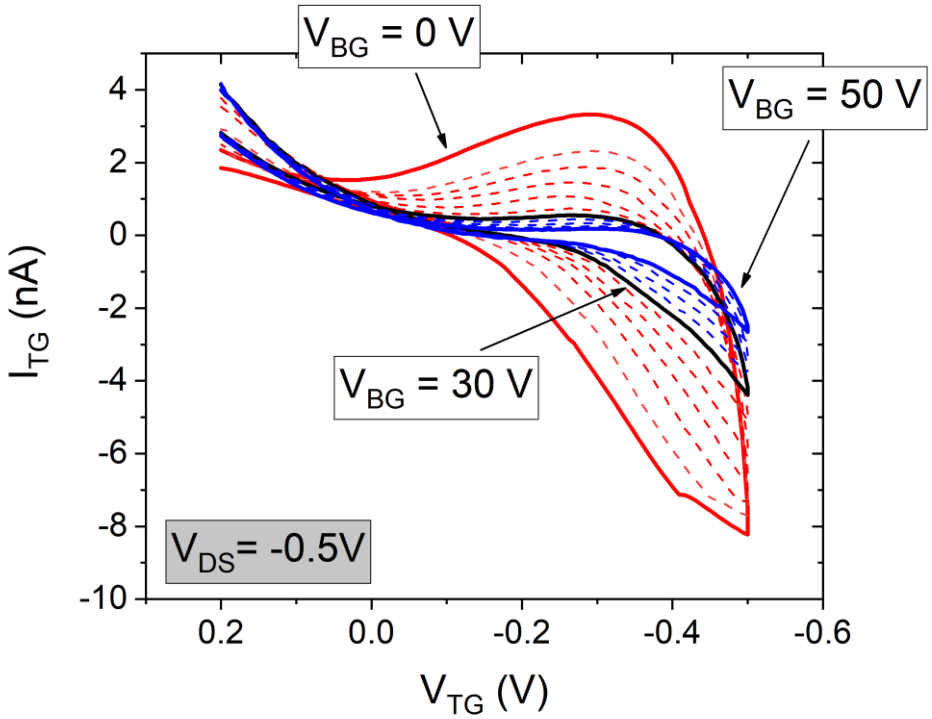

Figure S7 Leakage current (I_{TG}) related to sequential I-V transfer characteristics by changing systematically the BG voltage (i.e. from 0 V to +50 V).

If the BG voltage (V_{BG}) would alter the medium potential at the interface with the semiconductor, it

would also induce an increase of the top-gate (TG) leakage current (I_{TG}). As shown in Figure S6, the leakage current of the top-gate (I_{TG}) reduces by increasing the V_{BG} (likely due to a decrease in the electronic channel conductivity). This proves that no electrical perturbations are occurring during these measurements. Moreover, although ion percolation cannot be excluded by these experimental data, it is clear that no faradaic currents take place, hence we can safely exclude any electrochemical doping, which would damage irreversibly our organic semiconductor.

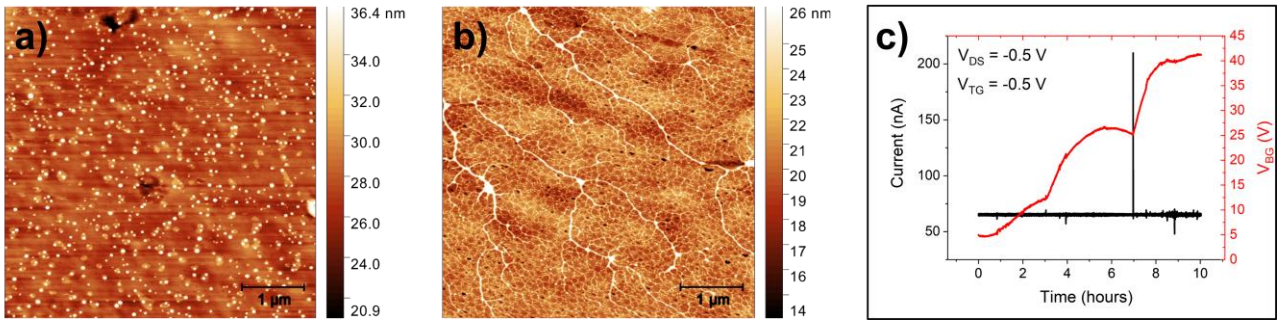

Figure S8 a) AFM image of diF-TES-ADT:PS layer (area equal to 5x5 µm^2) before the electrical test. **b)** AFM image of diF-TES-ADT:PS layer (area equal to 5x5 µm^2 and 1x1 µm^2) after the electrical test. **c)** Electrical test related to the morphological analysis.

Figure S8a shows white spots randomly distributed onto the surface, which are small agglomerates of PS (average height is equal to 38±3 nm). This morphological analysis shows a σ_{rms} = 2.7 nm that is coherent to the previous topographic studies of similar devices (Q. Zhang et al. Scientific Reports 2016, 6:39623). After the prolonged test (Figure S8c), the white PS spots are mainly reorganized in fibrils, whose height is averagely reduced to 22±1 nm and the σ_{rms} = 1.9 nm (Figure S8b). According to these data, we can safely state that the semiconducting layer is robust and no clues of delamination and dewetting are observed.

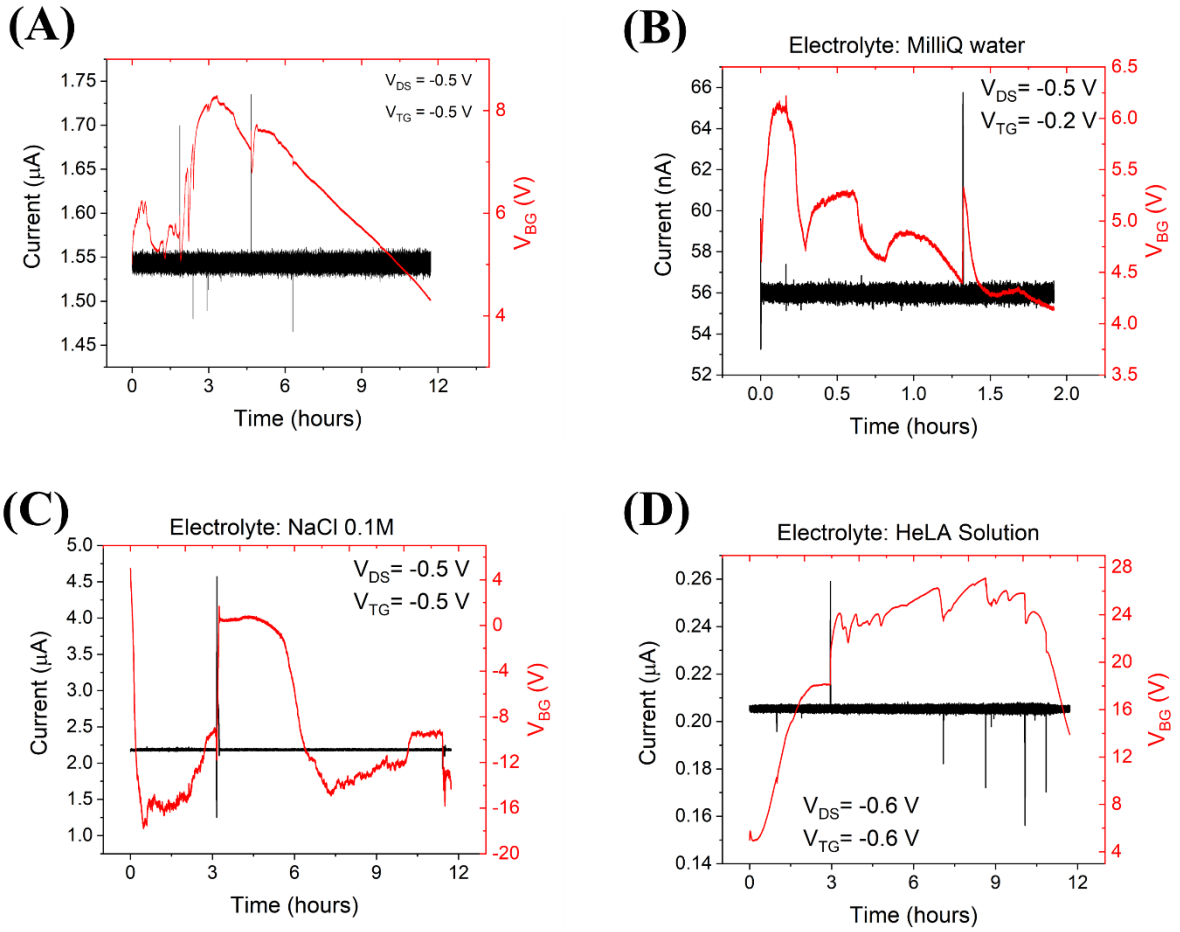

Figure S9 I vs. t tests in different aqueous solutions: **(A, B)** Milli-Q; **(C)** NaCl 0.1M and **(D)** HeLA solution. Different V_{TG} and V_{DS} are used.