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Pacheco-Sánchez, Aníbal [et al.]. «An Extraction Method for Mobility Degradation and Contact Resistance of Graphene Transistors». *IEEE transactions on electron devices*, Vol. 69, Num. 7 (July 2022), p. 4037-4041 DOI 10.1109/TED.2022.3176830

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An extraction method for mobility degradation and contact resistance of graphene transistors

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***Abstract*—The intrinsic mobility degradation coefficient, contact resistance and the transconductance parameter of graphene field-effect transistors (GFETs) are extracted for different technologies by considering a novel transport model embracing mobility degradation effects within the charge channel control description. By considering the mobility degradation-based model, a straightforward extraction methodology, not provided before, is enabled by applying the concept of the well-known *Y*-function to the *I-V* device characteristics. The method works regardless the gate device architecture. An accurate description of experimental data of fabricated devices is achieved with the underlying transport equation by using the extracted parameters. An evaluation of the channel resistance, enabled by the extracted parameters here, has been also provided.**

***Index Terms*—graphene FET, mobility degradation, contact resistance, channel resistance, Y-function.**

I. Introduction

One of the most popular approaches for the characterization of graphene field-effect transistors (GFETs) has been the description of experimental data by a device total resistance $R_{\rm tot}$ model [1]. This model considers the impact of vertical fields and impurities on the carrier transport and has enabled to obtain relevant device parameters since its proposal, e.g., a low-field mobility [2]-[4]. Recently, this well-known model has been adapted in order to explicitly consider mobility degradation effects in the performance description of GFET technologies [5]. This novel approach has been motivated by experimental observations of a carrier density-dependent mobility in GFETs under different scenarios [6]-[8]. Hence, a first-order mobility model considers both, short- and long-range scattering mechanisms in graphene devices by including an intrinsic mobility degradation coefficient $\theta_{\rm ch}$ into the mobility description, similarly to the approach used in MOSFET theory [9]-[11]. Additionally, a potential drop at the metal-graphene interface has been considered by a contact resistance $R_{\rm c}$ in order to describe the internal transport phenomena.

From a device characterization point of view, the fitting procedure relying on an initial guess of $R_{\rm c}$ towards obtaining the other three model parameters in [5] might become an important constraint for the characterization of GFETs at a large scale due to the computational burden and challenges related to randomly finding adequate initial values. A straightforward parameter extraction methodology considering experimental data is required to expand and ease the use of this novel modeling-based characterization approach. In this work, by following a methodical treatment of experimental data based on the concept of the well-known Y-function, a parameter extraction methodology for the mobility degradation-based transport model is proposed using individual device transfer characteristics of a given GFET technology with devices of different gated-channel lengths. In contrast to the original approach [5], the extraction methodology proposed here is more robust for device characterization purposes since it yields values of three out of four of the model parameters without needing any initial random assumption. The fourth parameter, related to charge-neutrality, is extracted by appropriately adjusting the model to experiments at very low transversal electric fields.

By considering the characterization of GFET technologies including sub-μm gate-lengths, the model-based characterization is proven here to be for general purposes and not only for long devices as shown in [5]. Further adaptations of the underlying model to include velocity saturation effects - relevant at high lateral fields- are out of the scope of this work, however, the extracted parameters here can be relevant for the extraction of velocity saturation related parameters. In contrast to previous GFET studies using *Y*-function-based methods [12]-[15], this work relies on a transport current description including a charge definition more related to GFETs physics rather than the conventional MOSFET charge equation. The extracted parameters enable an evaluation of the mobility and an accurate description of the drain current over a wide transversal electric field range including charge neutrality conditions.

This straightforward extraction methodology of contact resistance and mobility parameters of graphene technologies can be applied to any gate architecture. Hence, it is an immediate efficient alternative to test-structure-based extraction methodologies such as the transfer length method (TLM) [16], limited to global-back-gate (GBG) devices only. The latter limitation can mislead performance projections based on TLM for other device architectures in which the different electrostatics, e.g., from a top- (TG) [17] or buried-gate (BG) [18], might affect the Schottky-like potential barrier height at graphene-metal contacts [19], [20], i.e., the value of $R_{\rm c}$. Furthermore, the fabrication issues of individual TG and BG [18] graphene devices, implies a more challenging fabrication of TLM structures (including a series of individual devices) for such configurations. The TLM-related constraints are overcome by the method presented here since (i) the particular device electrostatics is considered in the underlying transport description and (ii) no fabrication of extra test structures is required.

This work has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreements No GrapheneCore3 881603, from Ministerio de Ciencia, Innovación y Universidades under grant agreement RTI2018-097876-B-C21(MCIU/AEI/FEDER, UE) and FJC2020-046213-I. This article has been partially funded by the European Union Regional Development Fund within the framework of the ERDF Operational Program of Catalonia 2014-2020 with the support of the Department de Recerca i Universitat, with a grant of 50% of total cost eligible. GraphCAT project reference: 001-P-001702.

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II. Parameters extraction methodology

The drain current $I_{\rm D}$ of GFETs given by a straightforward adaptation of a widely used *I-V* model [1] considering both an appropiate charge control description and an explicit contribution of the extrinsic mobility degradation coefficient θ [10], [21], [22] is expressed as[1] [5]

$$I_{\rm D} = \beta \frac{\sqrt{V_0^2 + V_{\rm GSO}^2}}{1 + \theta\sqrt{V_0^2 + V_{\rm GSO}^2}} V_{\rm DS}, \tag{1}$$

where β is a transconductance parameter associated to $\mu_{\rm app,0} C_{\rm ox} w_{\rm g}/L_{\rm g}$ [22] with $\mu_{\rm app,0}$ as an apparent low-field mobility, $C_{\rm ox}$ as the gate oxide capacitance per unit area, $w_{\rm g}$ as the gate width and $L_{\rm g}$ as the gated-channel length, $V_{\rm GSO} = V_{\rm GS} - V_{\rm Dirac}$ is the extrinsic gate-to-source voltage overdrive with $V_{\rm GS}$ as the extrinsic gate-to-source voltage and $V_{\rm Dirac}(= V_{\rm GS}|_{\min(I_{\rm D})})$ as the $V_{\rm GS}$ corresponding to charge neutrality conditions, $V_0 = qn_0/C_{\rm ox}$ the residual voltage with q as the electron charge, n_0 as the residual charge carrier density at $V_{\rm Dirac}$ [1], $\theta = \theta_{\rm ch} + \beta R_{\rm c}$ with $\theta_{\rm ch}$ as the intrinsic mobility degradation coefficient due to vertical fields [9]-[11] and the contact resistance $R_{\rm c}(= R_{\rm cs} + R_{\rm cd})$ embracing the phenomena at metal-channel interfaces (source and drain sides). Notice that Eq. (1) can be also obtained from the drift-diffusion transport description for graphene transistors [23] after neglecting the quantum capacitance and the local channel voltage at low $V_{\rm DS}$.

Based on Eq. (1) and by considering that $V_{\rm GSO} \gg V_0$, the transconductance $g_{\rm m} = \partial I_{\rm D}/\partial V_{\rm GS}$ is given by

$$g_{\rm m} \approx \beta \frac{1}{\left(1 + \theta\sqrt{V_0^2 + V_{\rm GSO}^2}\right)^2} V_{\rm DS}, \tag{2}$$

while the device total resistance $R_{\rm tot} = V_{\rm DS}/I_{\rm D}$, considering the definition of θ, reads

$$R_{\rm tot} = \underbrace{\left(\frac{1}{\beta\sqrt{V_0^2 + V_{\rm GSO}^2}} + \frac{\theta_{\rm ch}}{\beta}\right)}_{R_{\rm ch}} + R_{\rm c}. \tag{3}$$

A comparison with the general definition of $R_{\rm tot}$ as the sum of channel resistance $R_{\rm ch}$ and $R_{\rm c}$, and by considering that $\theta_{\rm ch}$ is associated to channel phenomena [9]-[11], leads to relate the term inside brackets in Eq. (3) as $R_{\rm ch}$ in the context of this work. The latter is confirmed by considering two channel scattering mechanisms (cf. Eq. (3) in [5]) in the underlying transport model (cf. Eq. (3) in [1])[2].

By applying the concept of the Y-function [22], [24], i.e., $Y = I_{\rm D}/\sqrt{g_{\rm m}}$, with Eqs. (1) and (2), this relation yields

$$Y \approx \sqrt{\beta V_{\rm DS}}\sqrt{V_0^2 + V_{\rm GSO}^2}, \tag{4}$$

while the product of Eqs. (3) and (4) corresponds to

$$R_{\rm tot} Y \approx \sqrt{\frac{V_{\rm DS}}{\beta}} + \frac{\theta}{\beta} Y. \tag{5}$$

The ratio θ/β and the parameter β can be extracted from the plots of $R_{\rm tot}Y$ vs. Y and Y^2 vs. $V_{\rm GSO}^2$, respectively, for different $L_{\rm g}$ and at a fixed low $V_{\rm DS}$. By following the definition of θ given above, $\theta_{\rm ch}$ and $R_{\rm c}$ are extracted from the intercept at zero and slope of a β-dependent plot of θ. While the extraction of β, $\theta_{\rm ch}$ and $R_{\rm c}$ is performed at an unipolar bias region away from $V_{\rm Dirac}$, the underlying model can be adjusted towards describing charge neutrality conditions. Hence, a unique value for V_0 is obtained from the best adjustment of the model to experimental data at the bias region close to $V_{\rm Dirac}$, upon extraction of all other parameters.

The extraction method yields a constant $R_{\rm c}$ value which can be of special interest for technology evaluation [3] as well as an initial guide for modeling purposes towards the design of specific applications at a fixed bias point, e.g., high-frequency circuits[3] [25], [26]. For the interested reader, a bias-dependent contact resistance model, which is out of the scope of this work, has been reported elsewhere [19]. Notice that despite Eq. (5) resembles the approach presented in [27] for silicon technologies, both the underlying transport equation and the extraction methodology are different in this work.

III. Characterization of GFET technologies

The parameter extraction methodology described above has been applied to the experimental data of GFET technologies with different device architectures such as GBG [28], [29], BG [17], [23] and TG [30] as well as with different sub-µm- and µm-long gate lengths. Device characteristics and extracted parameters are listed in Table I.

TABLE I
Characteristics and extracted model parameters of GFETs.

gate arch. & ref.	$w_{\rm g}$ (µm)	$L_{\rm g}$ (µm)	$\theta_{\rm ch}$ ($\rm V^{-1}$)	$R_{\rm c}\cdot w_{\rm g}$ ($\rm k\Omega\cdot\mu m$)
GBG, [28]	5	0.120, 0.225, 0.640, 2	0.025	2.9
GBG, [29]	20	5, 10, 15 20, 25, 30	0.034	1.6
BG, [17]	–	0.250, 0.450	1.5	$0.2\cdot w_{\rm g}$
BG, [23]	12	0.1, 0.2, 0.3	3.1	2.6
TG, [30]	3.4	0.1, 0.3, 1, 2	0.081	0.4

The extraction procedure is depicted in Fig. 1 with experimental data of GBG devices reported elsewhere [29]. Only the *n*-type region ($V_{\rm GSO} > 0$) has been used for the extraction. From the experimental transfer characteristics of GFETs with different $L_{\rm g}$ and at a given $V_{\rm DS}$, plots of $R_{\rm tot}$ and the Y-function have been obtained (Fig. 1(b)). The product of $R_{\rm tot}$ and Y has been ploted over Y (Fig. 1(c)) in order to obtain the ratio θ/β from the slope of the linear part of each curve (at $Y > Y|_{\min(R_{\rm tot}Y)}$), i.e., for each $L_{\rm g}$, as indicated by Eq. (5). Similarly, the slopes of the curves in the $Y^2(V_{\rm GSO}^2)$-plot (inset of Fig. 1(c)) yield the parameter β. The contact resistance and the intrinsic mobility degradation coefficient are obtained from the $\theta(\beta)$ plot (Fig. 1(d)). In order to validate the extracted parameters, the model with the extracted parameters succesfully describes the experimental transfer characteristics, provided V_0 is obtained, as shown in Fig. 1(a).

[1] Notice that θ has been called $\theta_{\rm eff}$ in [5].

[2] $R_{\rm tot} = (N_{\rm sq}/\mu_0)(1/qn + \theta_{\rm ch}/C_{\rm ox}) + R_{\rm c} \equiv R_{\rm ch} + R_{\rm c}$, with the number of squares $N_{\rm sq} = L_{\rm g}/w_{\rm g}$

[3] In general, GFETs are fixed at $|V_{\rm GS} - V_{\rm Dirac}| \gg 0$ in practical scenarios where a high transconductance in an unipolar region benefits the dynamic performance.

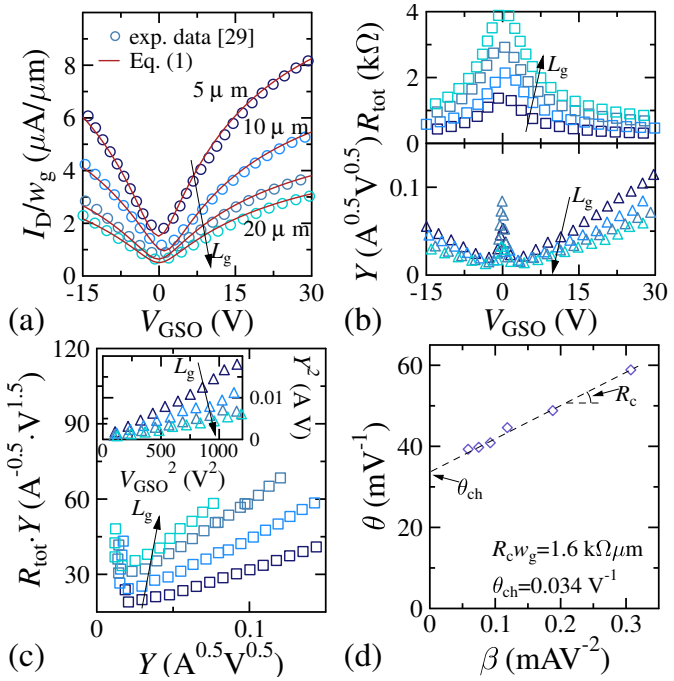


Fig. 1. Extraction methodology presented in this work applied to the GBG GFET technology presented in [29]. (a) Transfer characteristics, (b) total resistance (top) and Y-function (bottom) plots over V_{GSO}, (c) $R_{tot}Y$ and Y^2 (inset) over Y and V_{GSO}^2, respectively and (d) θ over β plot showing the extracted parameters R_c and θ_{ch}. Markers represent experimental data and solid lines represent Eq. (1) results by using the extracted parameters. Dashed lines are added as guides for the eyes in order to show the extracted parameters. $V_{DS} = 0.05$ V for all plots.

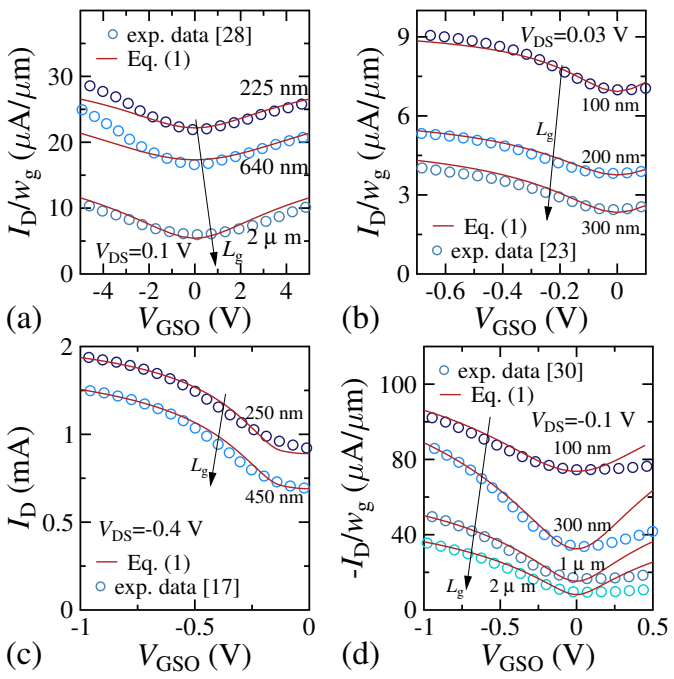


Fig. 2. Transfer characteristics of GFET technologies with different architectures: (a) GBG [28], (b) BG [23], (c) BG [17] and (d) TG [30]. Markers represent experimental data and solid lines represent modeling results by using the extracted parameters in Eq. (1).

By using the corresponding extracted parameters (cf. Table I), the mobility degradation-based transport model describes the experimental transfer characteristics of the other GFET technologies studied here within the bias region where the extraction methodology has been applied in each case as shown in Fig. 2. The values of $\mu_{app,0}$ for the shortest devices in the BG technologies presented in this work are of $2079\,\mathrm{cm^2V^{-1}s^{-1}}$ for [17] and of $2580\,\mathrm{cm^2V^{-1}s^{-1}}$ for [23]. These values are similar to the ones reported in the literature: 2000 to 2500 $\mathrm{cm^2V^{-1}s^{-1}}$ for the former one [17] and of $3250\,\mathrm{cm^2V^{-1}s^{-1}}$, reported with Hall measurements in [32], for the latter [23].

The impact of velocity saturation, out of the scope of this modeling approach, can further improve the model adjustment. E.g., if a simple velocity saturation model for an effective mobility $\mu_{eff}(=\mu/(1+E_x/E_c))$ is considered, where μ includes mobility degradation effects as Eq. (1) in [5] and E_x and E_c are the horizontal and critical electric field, respectively, the related velocity saturation parameters can be extracted at high V_{DS} regime provided that all the other parameters, i.e., θ, R_c and β have been estimated from a lower V_{DS} region with the extraction method presented here. A similar approach for the estimation of velocity saturation effects has been presented elsewhere [4].

The pronounced asymmetry in experimental transfer characteristics (cf. Figs. 2(a) and (d)) due to different mobility and contact properties observed in the devices of [28] and [30] is not captured by the model. Hence, slight discrepancies are observed in the unipolar region where the extraction has not been performed, i.e., *p*-type in [28] and *n*-type region in [30]. In this case, a new parameter set obtained by applying the extraction method at the bias conditions of interest can be used to overcome the disagreement due to asymmetric device features. For the GBG (TG) device in [28] ([30]), the extraction methodology applied for the *p*-type (*n*-type) region yields values of $R_c \cdot w_g$ equal to $0.8\,\mathrm{k\Omega \cdot \mu m}$ ($0.65\,\mathrm{k\Omega \cdot \mu m}$) and of θ_{ch} equal to $0.04\,\mathrm{V^{-1}}$ ($0.29\,\mathrm{V^{-1}}$). The different current levels in each part of the transfer curves (Fig. 2(a) and (d)) of the device in [28] ([30]) are associated to the lower (higher) $R_c \cdot w_g$ extracted value for the *p*-type (*n*-type) region in contrast to the one obtained for the *n*-type (*p*-type) region (cf. Table I). Additionally, the weaker gate control over the channel observed for the TG device [30] at $V_{GSO} > 0$ V than at $V_{GSO} < 0$ V is quantified by an extracted θ_{ch} value which is ~ 3.6 higher than the one extracted for the *n*-type region.

Regarding the extracted R_c values, for the GBG technology with relaxed dimensions, the extracted value of R_c (cf. Fig. 1(b)) is in good agreement with the one obtained by TLM in [29] considering the bias region where the methods have been applied, i.e., $9\,\mathrm{V} < V_{GSO} < 37\,\mathrm{V}$. In the case of the BG GFET reported in [23], the slight difference ($\sim 30\,\Omega$) between the extracted R_c value here and the one obtained by the adjustment of a compact model is related to different underlying transport equations. The extraction of R_c with this methodology for all kind of device architectures overcomes the challenging fabrication of TLM test structures which are generally limited to GBG devices [16], specially in graphene technologies [12], [29]. Values of θ_{ch} for GFETs have been rarely reported in the literature with other methods [14]. Regarding the GFETs analyzed here, GBG devices have the lower θ_{ch} owing to the full-gated channels in contrast to BG and TG devices, and hence, a better overall gate control over the channel is obtained with the former device architecture. It is worth to notice that in the device technologies studied here, θ_{ch} is not negligible for the definition of θ as suggested elsewhere for 2D-based

devices [31]. The latter is of key importance to determine whether the device performance is dominated by channel or contact phenomena [14].

The experimental device channel resistance BG GFET technology reported in [23], obtained upon extraction of R_c, is well described by the modeling approach followed here, i.e., considering θ_{ch} into its description (c.f. Eq. (3)), as shown in Fig. 3(a). The experimental R_{tot} curves have been included in the plot for comparison purposes. Modeling results of R_{ch} without including θ_{ch} fail to describe the experimental data: the maximum (minimum) error between model without θ_{ch} is of $\sim 60\%$ ($\sim 25\%$) in contrast to the $\sim 15\%$ ($\sim 0.5\%$) maximum (minimum) relative error for the R_{ch} model considering θ_{ch}, all values for the region where the parameter extraction has been performed for these devices, i.e., for $V_{GSO} < 0\,V$.

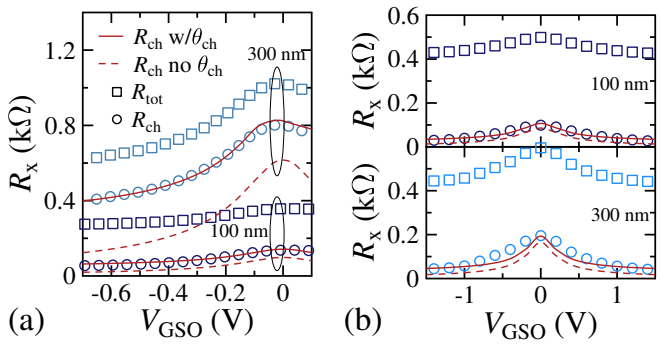


Fig. 3. Resistances of (a) fabricated ($V_{DS} = 0.03\,V$) [23] and (b) simulated ($V_{DS} = 0.1\,V$) GFETs with different L_g. Solid (dashed) lines are modeling results of R_{ch} considering (not considering) θ_{ch}. Legend in (a) applies to (b).

Numerical device simulations (NDS) have been performed in order to further explore the channel resistance description. The simulated GFETs under study have gated-channels (of lengths of $100\,nm$ and $300\,nm$ and a width of $1\,\mu m$) encapsulated in a hexagonal-boron nitride dielectric. Mobility degradation due to vertical fields has been considered. The contact resistance value is set to $400\,\Omega$. The model used in simulations consists in the self-consistent solution of the Poisson's equation together with the current continuity equation, where the properties of carrier transport have been previously extracted from Monte Carlo simulations [13], [33]. Simulation results, shown in Fig. 3(b), reveal that the devices total resistance is mainly due to the injection mechanisms ($R_c > R_{ch}$). The extraction method has been applied to the NDS data yielding an R_c value of $397\,\Omega$ and a θ_{ch} of $1\,V^{-1}$. The channel resistance obtained from the simulation data by $R_{ch} = R_{tot} - 400\,\Omega$ has been better described by an R_{ch} model considering θ_{ch} (maximum/minimum error of $\sim 30\%/3\%$ at the region used for extraction) in contrast to the approaches suggested elsewhere [5], [31] where θ_{ch} has been neglected as a channel transport parameter (maximum/minimum error of $\sim 55\%/30\%$ at the region used for extraction).

Hence, in addition to the conceptual relation of θ_{ch} to channel phenomena (and corresponding parameters) and the discussion provided above, the results presented here suggest that the term including θ_{ch} should be accounted for an accurate description of R_{ch}. The L_g independence of R_c, implied with the latter approach, has been also confirmed with experimentally calibrated physics-based contact models of GFETs [19], [20]. In other words, in contrast to a previous proposal where the R_c value varies with L_g, the effect of a gate electrostatics-dependent effective length of the potential step (in the transport direction) at metal-graphene interfaces [19], [34] has been associated in this approach to the transport within the channel rather than to contact effects.

IV. Conclusion

A parameter extraction methodology of a novel model considering mobility degradation effects in GFETs has been provided. The underlying transport model using the extracted parameters, namely R_c, θ_{ch} and β, describes accurately the experimental data of various short- and long-gate GFET technologies at different bias conditions regardless the gate architecture. The latter is of relevance for leveraging the challenging fabrication of test structures for parameter extraction. The engineering approach proposed with this extraction method relies entirely on a mathematical treatment of the experimental transfer characteristic enabled by a mobility degradation-based modeling proposal, i.e., no initial fitting parameters are required. The mobility degradation description enabled by the extracted parameters can be useful for technology evaluation and modeling purposes as shown in this work. A modeling approach including θ_{ch} in the description of the channel resistance has been proven to yield more accurate results than the case where θ_{ch} is not considered into R_{ch}. The extracted parameters can be included in compact models. The extracted constant value of R_c can be exploited in practical small-signal GFET modeling approaches where devices are biased at a certain operation regime.

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