Exploitation of OTFTs variability for PUFs implementation and impact of aging

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Abstract

Commercial Organic Thin Film Transistors (OTFT) have been characterized to evaluate their variability and reliability. The feasibility of implementing Physical Unclonable Functions (PUFs) based on these devices has been evaluated, taking advantage of the high variation in the electrical characteristics among different OTFTs. The eventual impact of device aging on PUFs reliability has been preliminary explored.

1. Introduction

The use of Organic materials in electron devices such as Thin Film Transistors (TFT) has increased during the last years due to their low-cost, sustainability and easy fabrication [1,2]. Their potential use in the Internet of Things (IoT) and wearable electronics has been explored, thanks to the possibility of fabricating smart and flexible electronic systems [3]. Due to the good characteristics of these materials/devices, many works have been focused on the study of the properties of the materials themselves [4-6] or the performance of the devices fabricated with them [7]. However, few works have been devoted to the study of the variability and reliability of OTFTs [4, 8, 9]. Since the fabrication of organic materials is not a mature process yet, the devices show high initial variability (i.e., Time-Zero Variability, TZV). TZV of OTFTs is improving as the technology matures, but it is possible to make devices with some larger variability, to be exploited for some security and cryptography applications. The randomness associated to the heterogeneous nature of organic materials and the fabrication processes can be used as a source of entropy for the implementation of Physical Unclonable Functions (PUFs) [10, 11]. Regarding the reliability of OTFTs, it is also an issue of concern. The usual operating conditions of this kind of devices can be a serious drawback, due to the high voltages needed (in the range of 10-30V). Therefore, the aging mechanisms activated during the device operation/stress and their impact on the organic layer and on the device performance must be studied in detail [12]. This task could be further complicated because of the large number of materials available, so different strategies are necessary to evaluate the origin of the possible reliability issues.

In this work, the TZV of OTFTs has been analyzed, to evaluate the feasibility of using them to implement PUFs. The effects of electrical HCI-like stresses have been also preliminary analyzed, and the eventual effects on PUF performance discussed.

2. Experimental

The analysed OTFTs are four-terminal transistors with a top gate configuration and multiple channels and gold contacts (Fig. 1) [7]. The devices were fabricated by SmartKem Ltd. (UK), using gold contacts, and their proprietary stack of materials TRUFLEX based on BL (Base Layer), OSC (Organic Semiconductor), OGI (Organic Gate Insulator), SRL (Sputter Resistant Layer, PL (Passivation Layer). The fabrication process combines sputtering, spin coating and photolithographic steps.

Devices with W=640µm and L=3µm have been studied in this work. I_D-V_G curves have been measured at V_{DS}=-20V in 74 OTFTs, for TZV evaluation. Back Gate was grounded in all stresses and measurements. Fig. 2a shows some examples of the measured I_D-V_G curves. Note the large device-to-device variability, which can be accounted for by the dispersion in the threshold voltage and carrier mobility. HCI-like tests (V_G= -30V, V_D= -30V) during 4500s have also been carried out to evaluate the aging of this kind of devices. The stress was periodically interrupted to measure I_D-V_G curves, from which the induced degradation was evaluated.

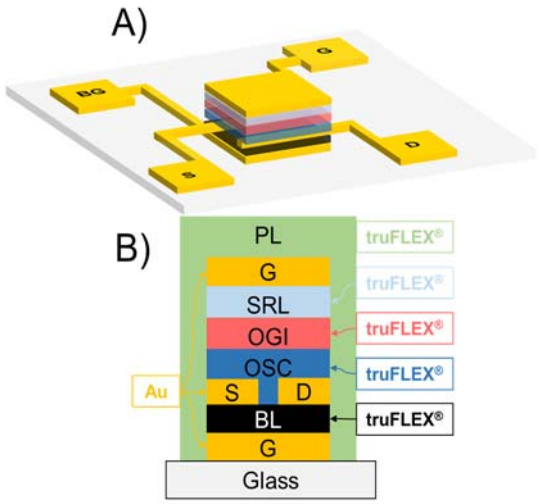

Fig.1. (a) 3D sketch of the OTFT and (b) its corresponding section.

3. PUF performance

For the PUF implementation, the current through the channel (I_D) at V_{DS}= -20V and V_{GS}=0V obtained from the transfer characteristics of OTFTs has been used as parameter to generate the digital key of the security primitive. Fluctuations in these currents show a Gaussian random distribution, as shown in Fig. 2b. For the evaluation of the PUFs quality, as one PUF contains one or several devices (depending on the PUF's

number of bits), a large number of devices is needed. For this reason many OTFT I_D-V_G curves have been generated, based on the experimental results. To do this, eq. (1) is considered to describe the I_D-V_G curves:

$$I_D = \frac{W}{L}\mu C_d \frac{1}{2}(V_{GS} - V_{th})^2 \quad \text{(Eq. 1)}$$

By fitting the data in Fig, 2a, the mobility (μ) and threshold voltage (V_{TH}) of the 74 experimentally measured devices has been obtained. Fig. 3 corresponds to the μ vs V_{TH} plot obtained from the experimental data. There is a high TZV, but no correlation between the parameters is observed.

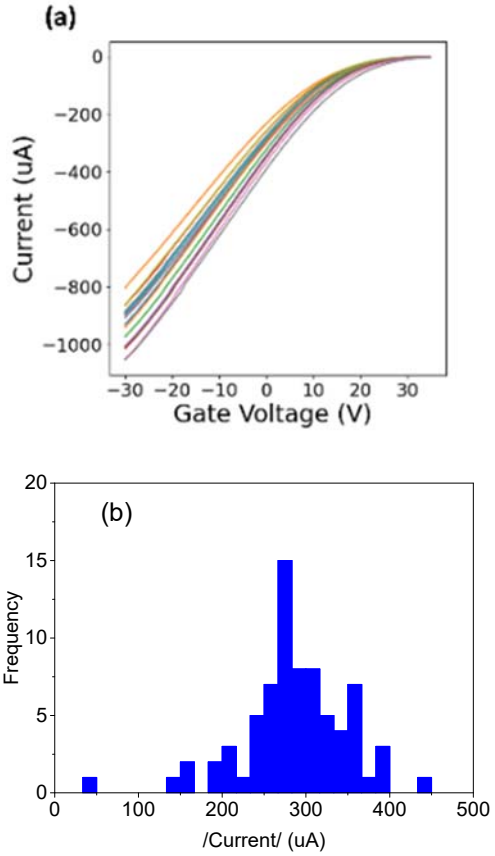

Fig.2. (a) I_D-V_G curves of some OTFTs for V_{DS}= -20V (L=3μm and W=640μm), and (b) Histogram of the I_D values at V_G=0V and V_{DS}= -20V.

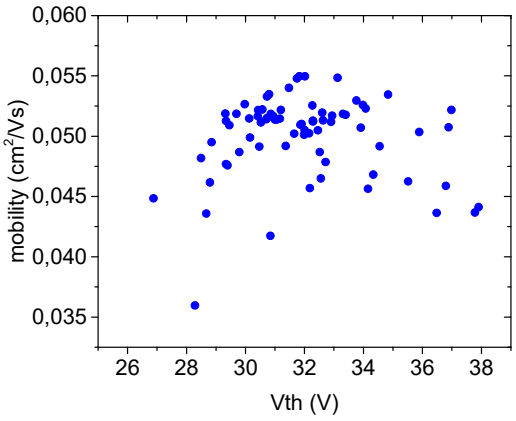

Fig. 3. Dispersion of μ vs V_{TH} corresponding to the experimental values.

The experimental μ and V_{TH} statistical distributions have been used to generate, using Montecarlo methods, the μ and V_{TH} of many OTFTs. From these values, the I_D at V_{GS}=0V and V_{DS}=-20V has been obtained using Eq. 1. The obtained I_D values were digitized into 8-bits binary words. From these 8-bit sequences, cryptographic keys of 8, 16 and 32 bits have been generated by using one or concatenating 2 or 4 digitized currents of different devices. In this regard, 200 PUFs with 8, 16 and 32 bits, were built, respectively. For the 8, 16 and 32 bits PUFs case, 200, 400 and 800 OTFT I_D-V_G were generated.

To evaluate the quality of the proposed PUFs, their uniformity and uniqueness have been analyzed. We have first evaluated the bit uniformity, which is a measure of the random distribution of "0s" and "1s", and should be ideally 0.5. The uniformity of a given PUF can be evaluated by dividing the number of 1-bits by the total number of bits of the key, using Eq (2):

$$PUF\ Uniformity = \frac{1}{s}\sum_{i=1}^{s} K_i \ x\ 100\%$$

Eq (2)

being *s* the key size and K_i is the bit at the position *i* of the PUF, which can be '0' of '1'. Table I shows the average and standard deviation of the uniformity of the 8, 16 and 32 bits PUFs. Note that its average value is very close to 50% in all cases, demonstrating the uniformity of the PUFs.

To determine the degree of correlation between two different PUFs, we have evaluated the device uniqueness. This parameter can be determined from the inter-device Hamming Distance (HD), which measures the number of bits that are different, with respect to the total number of bits of the key, when two different PUFs are compared. The inter-device HD between any two PUF devices can be defined with Eq (3):

$$Device\ uniqueness = \frac{2}{q(q-1)}\sum_{i=1}^{q-1}\sum_{j=i+1}^{q}\frac{HD\ (K_i, K_j)}{s}\ x100\%$$

Eq (3)

Where K_i and K_j are *s*-bit keys of the i[th] PUF device and the j[th] PUF device among *q* different PUFs, respectively. Table I also shows the average and standard deviation of the uniqueness of the 8, 16 and 32 bits PUFs. Again, the average value of this parameter is very close to 50% in all cases, demonstrating the uniqueness of the PUFs. Note, however, that in both cases (uniformity and uniqueness), the standard deviation depends on the number of bits, as expected. While for 8 bits the dispersion is quite high, it can be reduced by increasing the number of bits (although more devices are required to implement a PUF). Therefore, these results demonstrate that the fluctuations in carrier transport in OTFTs can be potentially used as an entropy source for the implementation of PUFs.

	8 bits		16 bits		32 bits	
	Unif.	Uniq.	Unif.	Uniq.	Unif.	Uniq
$\bar{X}$	0.48062	0.5094	0.4809	0.5095	0.5092	0.5060
σ^2	0.1596	0.1821	0.1113	0.1297	0.0743	0.0938

Table 1. Mean ($\bar{X}$) and standard deviation (σ^2) of the uniformity and uniqueness for the 200 PUFs of 8 bits, 16 bits and 32 bits generated words.

4. OTFTs Degradation Impact

After the analysis of the TZV, the impact of a HCI-like electrical stress has also been preliminary evaluated, to explore whether it may eventually impact the PUF performance. With this aim, a standard measurement-stress-measurement procedure was adopted. The stress (V_G= -30V, V_D= -30V, and a total stress time of 4500s) was periodically interrupted (at 300s intervals) to determine its impact on the device performance, by measuring the I_D-V_G curve. Fig. 4a shows an example of the typical evolution of I_D measured during the different stress phases and Fig. 4b the I_D-V_G curves registered during the interruptions. As observed from the I-t curve, there is a large relaxation of the current after the interruptions, so that the measured current could be strongly dependent on the time elapsed since the bias removal. Moreover, during each of the stress phases, large transients are observed, which lead to a net increase of the current.

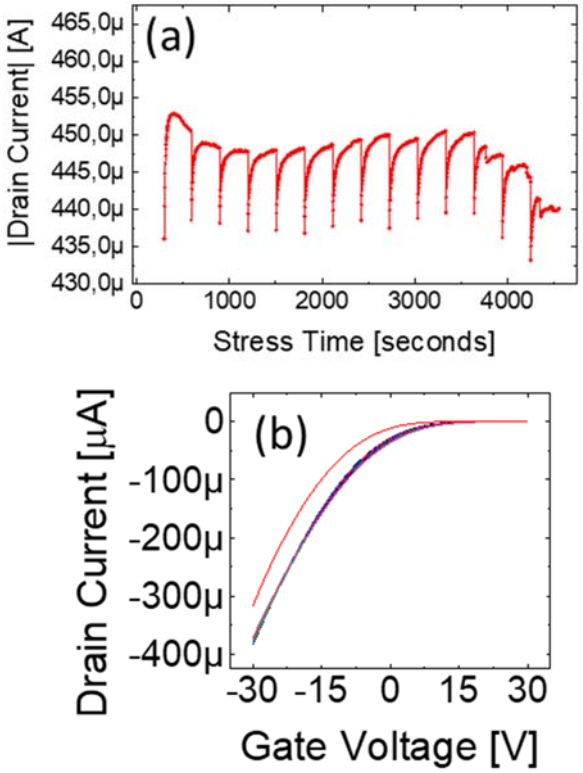

Fig. 4: Evolution of I_D during the interrupted stress (red circles), and (inset figure) the fresh I_D-V_G characteristics (red line) and the corresponding curves obtained during the stress interruptions.

Fig. 5 shows the I_D obtained from the I_D-V_G curves (V_{DS}= -20V) at V_G= 0V (blue circles) and V_G= -30V (red circles), as a function of the stress time. A rapid change is observed at short stress times. As expected, the value of I_D depends on V_G but note that the trend can also be V_G dependent, since the current can increase (V_G=0V) or decrease (V_G=-30V). In any case, the current tends to saturate for large enough stress time.

To show the impact of the I_D change during device operation on the PUF performance, the V_G=0V case has been considered; the binarized levels (6 bits for this example) are shown in figure 5 (top). Because of the stress, the device current shift can be large enough to drive I_D to other binarized levels (as observed in Fig. 5), producing the failure of the PUF functionality (i.e., the generated code has changed). The Error Time, which we have defined as the time needed to observe a change in the code because of aging, as a function of the number of bits (length of the binary key) has been analyzed.

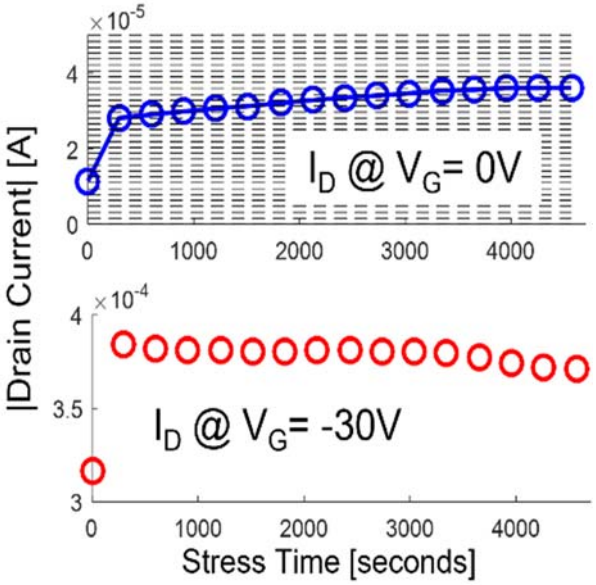

Fig. 5: Evolution of the I_D at V_G=0V (blue circles) and at V_G= -30V (red circles), obtained from the I_D-V_G (at V_{DS}= -20V) recorded when the HCI-like stress was interrupted as a function of the stress time. Dashed lines correspond to the binarized levels.

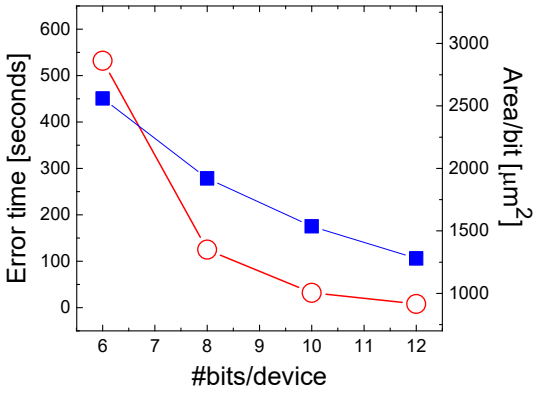

Fig. 6: Error time (red circles) and area per bit (blue squares) as a function of the number of bits per device. Device dimensions are W=640µm and L=3µm.

Fig. 6 (red circles) shows that the Error Time exponentially decreases with the number of bits per device, due to the power law dependence of the number of binarized levels on the number of bits. Therefore, to reduce code errors related to aging (see Fig. 5), I_D should be digitized with a smaller number of bits. But, to get a more reliable PUF (larger Error Time due to the aging) with a pre-determined number of bits, more devices should be used to implement the PUF, what means an increase of the area of the PUF. This is demonstrated in Figure 6 (blue squares), since the area per bit linearly decreases when the number of bits per device increases. So, Fig. 6 points out to a trade-off between the number of bits per device (to maximize the Error Time due to the aging) and the PUF area.

Finally, the Error Time as a function of the cumulative stress time was also analyzed. Fig. 7 shows this curve for the case of 8 bits, pointing out that the largest the device degradation, the longest the Error time. Though for this case, the error time continuously increases, a slight tendency towards saturation is observed since degradation slows down with the stress time (Fig. 5). This observation suggests that introducing some aging before the PUF is operated may be beneficial to implement reliable PUFs.

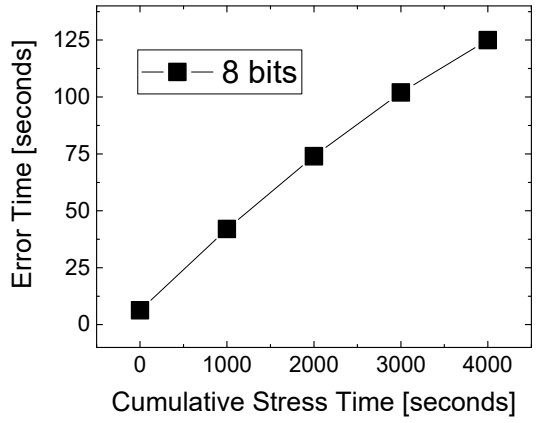

Fig. 7: Error Time dependence on the cumulative stress for the case of 8 bits.

5. Conclusion

The large TZV of OTFTs can be exploited to implement binarized I_D-based PUFs that exhibit good Uniformity and Uniqueness. The reliability of the PUFs has been preliminary evaluated, considering device aging during an HCI-like stress. Results show that the shift of the device current during its operation could be a drawback for this kind of applications and that its impact depends exponentially on the number of bits used for the binarizing process. However, these preliminary results show that the current shift decreases with the stress time. So, the application of a stress previously to the PUF operation may be beneficial to its reliability. Further work is needed to evaluate the performance of such 'aged' PUFs.

Acknowledgements

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