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Investigating the Device Performance Variation of a Buried Locally Gated Al/Al_2O_3 Graphene Field-Effect Transistor Process

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Abstract: In this study, a process is developed for the fabrication of buried top-gated graphene transistors with Al_2O_3 as a gate dielectric, yielding devices that can be suitable for not only flexible electronics but also laser-induced graphene (LIG)-based technology implementations. A new processing option is presented with the use of tetraethyl-orthosilicate (TEOS) as an etch stop for contact via etching of Al_2O_3. Buried locally gated Al/Al_2O_3 graphene field-effect transistors (GFETs) are fabricated with Dirac points as low as 4 V, with a metal-to-graphene contact resistance as low as ~1.7 kΩ·µm, and an average hole mobility of 457.97 $cm^2/V{\cdot}s$ with a non-uniformity of 93%. Large device variation and non-uniformity in electrical performance are not uncommon for graphene-based devices, as process-induced defects play a major role in such variation. AFM, SEM, Raman spectroscopy, and model fitting indicated that the rough Al/Al_2O_3 surface was the main factor for the observed device variation. AFM analysis indicated a graphene surface roughness Ra of 16.19 nm on top of the buried Al/Al_2O_3 gate in contrast to a Ra of 4.06 nm over Al_2O_3/SiO_2. The results presented indicate the need to reduce device variability and non-uniformity by improving transfer methods, as well as the use of smoother surfaces and compatible materials. The presented analyses provide a framework with which other researchers can analyze and correlate device variation and non-uniformities while methods to reduce variability are investigated.

Keywords: graphene; graphene field-effect transistors; 2D materials; gate dielectric; mobility; Dirac point; fabrication

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1. Introduction

Graphene is a low-dimensionality material which offers several advantages as an emerging electronic material in terms of high mobility (200,000 $cm^2/V{\cdot}s$) [1], high carrier concentration [2], high tensile strength (125 GPa) [3], and high thermal conductivity (~4000 $W{\cdot}m^{-1}{\cdot}K^{-1}$) [4]. In addition, graphene is inherently flexible, transparent, and chemically inert. Moreover, it has been adopted in several applications, such as bendable display technology, electrochemical energy storage devices, metal corrosion inhibitors, and signal processing and signal modulation applications [5–8]. Graphene does not have a bandgap; as such, it has found limited applications as a logic gate [9–12], although attempts have been made to form a bandgap with a bilayer graphene (BLG) structure [13]. On the other hand, due to its high mobility, there have been significant efforts toward the fabrication of graphene field-effect transistors (GFETs) for their application in high-frequency amplifiers, modulators, and resonators [14–16]. In addition, due to the sensitivity of graphene to physical and chemical stimuli, there are numerous reports of graphene-based physical and chemical sensors [17–20].

There are several reported fabrication methods of graphene-based devices [21–25]. The choice of the fabrication method comes down to the final application and the required performance, as well as the available resources. High-performing GFETs typically consist of nanometer-length channels and reduced S/D capacitance techniques [26], and reported studies have achieved an extrinsic cutoff frequency (f_T) of 34 GHz, as well as an extrinsic maximum oscillation frequency (f_{max}) of 37 GHz with gate lengths <350 nm fabricated via electron beam lithography [26]. Gate electrodes for these devices are generally fabricated with a top [27], buried [28], or trench-filled (damascene process) [29] structure. Gate dielectric materials of ultrathin AlO_x (naturally grown or ALD), hBN (transferred), and other high-k materials are used in order to maximize the performance of these devices [30–32]. Additionally, the substrate that creates an interface with graphene is carefully selected to minimize adverse effects [33]. Published reports have shown that, even though high-volume production of such transistors results in a reasonably high number of working devices (high yield), the device-to-device variation and non-uniformity of their electrical characteristics remain quite high [34–38]. Non-uniformity (NU) is a value of device variation and can be calculated as NU = (max − min)/average. The value of non-uniformity can be used as a figure of merit of variability when not enough data exists to obtain a statistical meaningful normal distribution. For example, Smith et al. reported the fabrication of 4500 top-gated GFETs with a yield of 75%, a median Dirac point of 4 V, and mobility of 40 $cm^2/V{\cdot}s$, but non-uniformity of 150% and 300% [34]. The observed device variation was explained by graphene defects during transfer, the strain of graphene, transfer polymer residue, and interface substrate effects [34–36,39].

In contrast, in the design and fabrication of graphene-based THz resonators for communication systems and chemical/physical sensors, the dimensions of the proposed devices are in the micrometer range (1–100 $s{\cdot}\mu m$) to meet the required performance of the application. THz resonators have been proposed through the hydrodynamic electron fluid concept applied to the Dyakonov and Shur (DS) instability [40–42]. THz radiation has been predicted in structures with high electron density and high-carrier-mobility materials with certain boundary conditions. The dimensions of these THz resonators are designed to match the targeted wavelengths at resonance [43]. Likewise, the design and fabrication of graphene-based chemical and physical sensors require devices with graphene dimensions in the micrometer range [44] to provide enough sensing area [17]. While sensors do not require large mobility, they do require repeatability between devices for robust and consistent signals [18]. In both cases, due to the larger relative dimensions of the graphene channel (1–100 μm), it is expected that these large-area devices will be more susceptible to material variations that have been observed and reported in the graphene transfer and/or synthesis process [24,34]. For example, Lerner et al. reported the fabrication and testing of >12,000 global back gate GFET sensors with an average Dirac point and hole mobility of 22.5 V and 4959 $cm^2/V{\cdot}s$, but non-uniformities of 88% and 200% [36].

The fabrication methods for larger-area sensor devices require that graphene be exposed to the stimuli; as such, a back-gated or buried-gate process is preferred. A buried-gate process not only provides the extra advantage and flexibility of being able to access each sensor individually on the same substrate but also assists in the decrease in parasitic source-to-gate and source-to-drain capacitance in comparison to global back gates. In a buried-gate process, aluminum can be used as the gate material as it is readily available, is inexpensive, and can be deposited in multiple ways (sputter, thermal, and e-beam evaporation). In addition, the gate dielectric does not need to be ultrathin, as higher bias levels may be required to obtain more robust signals [24]. As such, atomic layer-deposited (ALD) Al_2O_3 is often used as a dielectric as it generally provides lower interface traps than other CVD-based dielectrics, a lower Dirac point, and more repeatable results [24]. The integration of a buried aluminum gate with an ALD Al_2O_3 dielectric presents the challenge of etch compatibility when accessing the buried aluminum gate electrode. Although some have reported that the top Al_2O_3 can be simply scratched away during testing [45], the general approach is to apply the Al_2O_3 layer in a fluorine-based plasma etch, as it has excellent

selectivity to the underlying aluminum [46,47], a wet chemical etch in BOE, or a diluted resist developer [26,48]. As a downside, the fluorinated plasma etch of Al_2O_3 is slow with only CF_4 gas at an etch rate of 4.5 nm/min [47]. The inclusion of O_2 in etch gas can increase the etch rate [49] but it may become challenging to complete with a standard photoresist mask as the etch selectivity to any organic materials decreases.

There are several methods to synthesize graphene [50]. Among these, chemical vapor deposition (CVD) on a copper substrate results in large-area and high-quality single-layer graphene [51]. This CVD-grown graphene on Cu can then be transferred onto any needed substrate through wet, dry, or other alternative methods, thus providing process flexibility [52]. Another synthesis method, laser-induced graphene (LIG), has recently attracted extensive interest for chemical and biological sensors [19,50,51]. LIG can be integrated with both resistive-based [19] and field-effect transistor-based devices [53], where the graphene channel is exposed for sensing applications. One of the great advantages of LIG synthesis is that it completely eliminates the need for a graphene transfer process. Graphene formed directly on a polyimide (PI) [54] or any cross-linked hybrid lignocellulose [55] substrate via a laser writer offers the ability to achieve a minimum spatial resolution of 12 µm and has been reported by Stanford et al. [56]. The synthesized LIG consists of multilayer graphene with a high porosity characteristic that provides a much larger surface area when compared to monolayer graphene, which is favorable for chemical sensing applications. As with other graphene-based devices, the reported variation in sensitivity and performance remains a significant challenge of this method that must be investigated. For instance, Tour et al. reported the fabrication and test of LIG gas sensors with an average gas sensitivity ($\Delta R/R_{He}$) of 2.99 with a non-uniformity of 206% [19].

There is a need to understand device variability of micrometer-size GFETs, as well as the sources of variation. The work presented in this paper focuses on a large area process for devices with a 1–10 µm channel length and a buried aluminum local gate electrode aimed at applications such as graphene-based THz modulators and sensors. An alternative method to integrate an ALD Al_2O_3 gate dielectric using chlorine chemistry and an etch stop is presented. A large number of fabricated devices are electrically tested in order to analyze device variability in terms of electrical performance. In addition, SEM, Raman spectroscopy, and AFM are used to investigate the sources of variation as they relate to the process and electrical results. Lastly, the conclusions provide insights into the sources of variation and possible solutions that can be used to improve variability.

2. Materials and Methods

2.1. Device Fabrication

Shown in Figure 1 is a step-by-step process diagram of the device fabrication. The devices presented in this work were processed on a 6″ Si wafer to demonstrate the scalability of the proposed process. Alignment marks were first etched into n-type silicon wafers (100) for the ASML PAS 5500 i-line stepper, where all standard and lift-off lithography steps were performed thereafter. Following a standard RCA clean, 90 nm of SiO_2 was thermally grown at 1000 °C. Next, 200 nm of aluminum was thermally evaporated and patterned through a lift-off lithography process to serve as a gate electrode. The evaporation was conducted using a CVC thermal evaporator with 99.95% purity aluminum pellets. A 45 nm layer of PECVD TEOS was then deposited directly on top of the patterned gate electrodes to serve as an alumina etch stop when opening up contact vias. TEOS was patterned and etched away in a Trion Phantom III RIE with 60 sccm of CF_4, CHF_3 and 8 sccm of O_2 with RF power of 200 W to expose the aluminum gate electrode in the active area. Next, 15 nm of Al_2O_3 was deposited using an Ultratech S200 G2 Savannah atomic layer deposition (ALD) system with 150 cycles. High-quality CVD-grown monolayer graphene on copper foil (6″ × 6″) was commercially purchased from Graphenea, Inc. An area of 3″ by 2″ was cut out and transferred onto the surface of the wafer with a double PMMA-assisted process, described in detail in the next section. Graphene was then patterned through standard lithography by oxygen plasma via Trion Phantom III RIE for 60 s. The resist was removed by acetone soak

and rinsed with DI water. Ni and Au (5 and 95 nm, respectively) were thermally evaporated sequentially and patterned for source and drain contacts via a lift-off process. Finally, the wafers were coated with photoresist, and contact vias were patterned and etched away to expose the aluminum gate contact pads. This was performed in a two-step process, first etching the Al_2O_3 in the Plasmatherm ICP Etcher with chlorine-based chemistry and then the etch-stop TEOS layer in the Trion Phantom III with fluorine-based chemistry (details in Section 3). Individual chips containing several graphene FETs and test structures were cut into 1 cm by 1 cm chips using an ADT Dicing Saw 7120 prior to removing the photoresist protecting the graphene in the previous step.

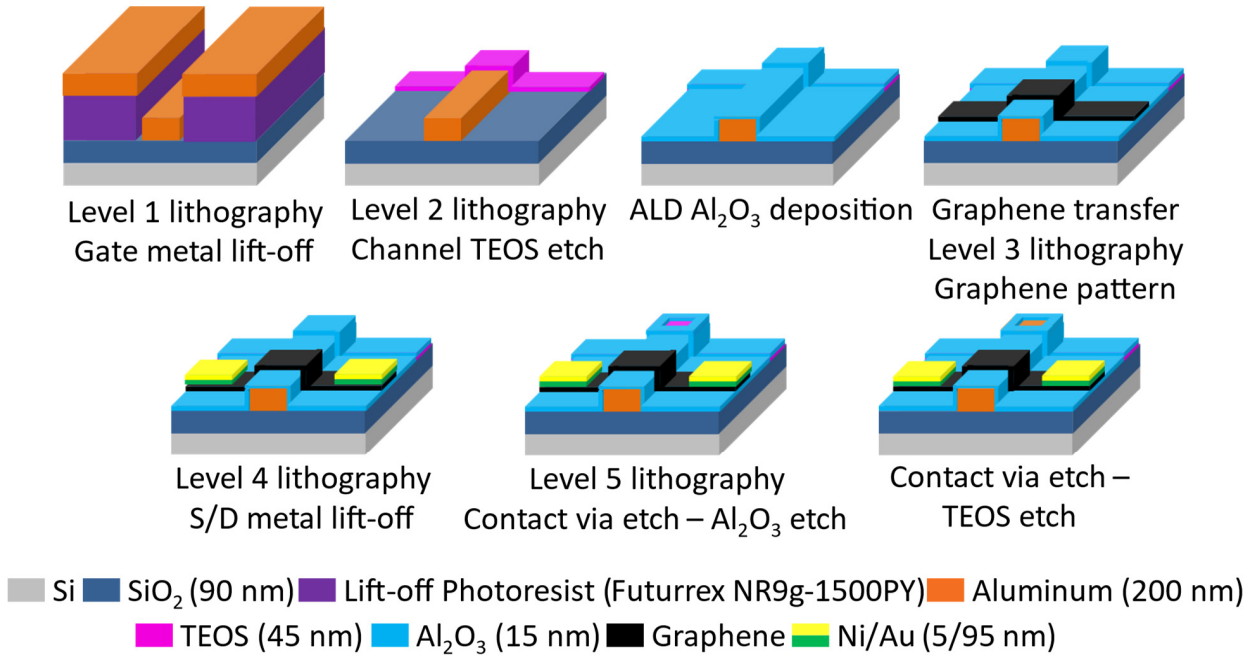

Figure 1. Buried locally gated Al/Al_2O_3 GFET fabrication process showing the multistep process to etch the out-of-plane contact to the gate electrode.

2.2. Graphene Transfer

High-quality CVD-grown monolayer graphene on copper foil was commercially purchased from Graphenea, Inc., Cambridge, MA, USA. [57]. An area of 3″ by 2″ was carefully cut out, and a modified PMMA-assisted graphene transfer, depicted in Figure 2, was used to transfer the monolayer graphene to the destination substrate [12,13]. Graphene on copper foil was taped onto a carrier wafer using Kapton tape. Two different PMMA solvents, 495 A2 and 950 A4 manufactured and purchased from Kayaku Advanced Materials, were used to compensate the stress of the stack of hard-baked polymer. The spin speeds for both PMMA 495 A2 and 950 A4 were kept at 1000 rpm for 30 s, each with a goal of obtaining a thicker coat (0.6 µm thickness in comparison to 0.25 µm at a 3000 rpm spin speed). PMMA was used to prevent the polymer/graphene stack from folding, warping, or ripping during transfer steps. The transfer process also consisted of baking the PMMA/graphene/copper stack on a hotplate at 200 °C for 2 min after each coat. The graphene was stored under vacuum overnight as reported from Langston et al. for a better adhesion of graphene to its substrate and for PMMA removal [58]. The PMMA was then removed by soaking the transferred wafer in an acetone bath at room temperature overnight, followed by baking the transferred sample stack on a hotplate at 200 °C for 10 min.

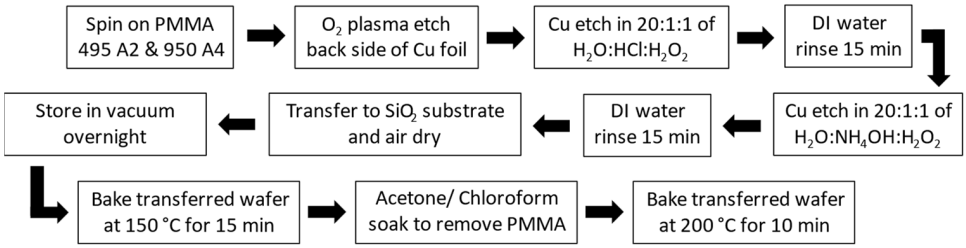

Figure 2. Block diagram description of a double PMMA assisted transfer process of graphene.

2.3. Test Methods

Electrical testing was conducted with a semi-automated RK probe card station, an HP-4156 parameter analyzer, and a manual SUSS electrical testing station with an HP-4145B parameter analyzer. Working devices were mapped out over 100 devices on the fabricated wafer across two dozen dies. Experimental data were collected for I_DV_G sweep and hysteresis tests with and without a pulse. Pulsed measurements were operated in a manner such that, after each applied V_{GS} bias, a constant voltage was applied with the purpose of removing trap charges.

Raman spectroscopy was carried out with the JY Horiba Labram-HR Raman spectroscope for further analysis on the quality of post-processing transferred graphene at multiple interest points within the active device area. A red 633 nm laser was used for the spectroscopy measurement with a measurement accumulation time of 30 s per data point.

Contact resistance estimations were obtained using a well-known total resistance model of GFETs presented elsewhere [59]. The goal of the estimation of contact resistance is to understand the key factor of device performance determinants. This method provides an immediate and straightforward approximation of the device performance, as well as eliminates the need for building and designing transfer length measurement structures (TLMs).

3. Results and Discussion

As presented in Section 1, the integration of a buried aluminum gate with an ALD Al_2O_3 dielectric presents the challenge of etch compatibility when accessing the buried Al gate electrode. Although Al_2O_3 can be etched in a fluorine-based chemistry, with very high selectivity to Al, this etch is slow and requires nonstandard lithography, such as the use of a hard mask or a thicker photoresist. A selective method to etch the Al_2O_3 gate over the buried Al gate electrode using standard lithography has been developed and is shown in Figure 3. The proposed method includes a thin etch-stop TEOS layer between the Al and the Al_2O_3. This TEOS layer is 45 nm thick and deposited after the Al gate has been patterned. After deposition, the TEOS is patterned and etched in a fluorine-based dry chemistry as to only remain over the gate electrode contact locations away from the active channel area of the GFET, as shown in Figure 1. A 15 nm Al_2O_3 gate dielectric is then deposited via ALD and remains on the entire wafer. The graphene is then transferred and patterned, and the metal contacts are deposited and patterned, as described in Section 2. Finally, the contacts must also be patterned and etched to access the Al bottom gate. This is accomplished via a two-step etch process as shown in Figure 3a,b. The contact vias are patterned using conventional lithography with a 1 µm AZ-MiR 701 positive photoresist. The Al_2O_3 is then etched in the Plasmatherm ICP Etcher with 30 sccm of BCl_3 for 23 s under a chamber pressure of 4 mTorr and 500 W of ICP source along with a 50 W RF bias where the high-selectivity to TEOS makes this layer act as an etch stop, as shown in Figure 3a. This BCl_3 etch has an etch rate of 40 nm/min and allows the process to complete with the photoresist still remaining for the next step. The etch-stop TEOS layer is removed in the Trion Phantom III with 60 sccm of CF_4, 70 sccm of CHF_3, and 6 sccm of O_2 for 60 s under 130 mTorr chamber pressure and 200 W of RF power as shown in Figure 3b, thereby exposing the Al gate contact.

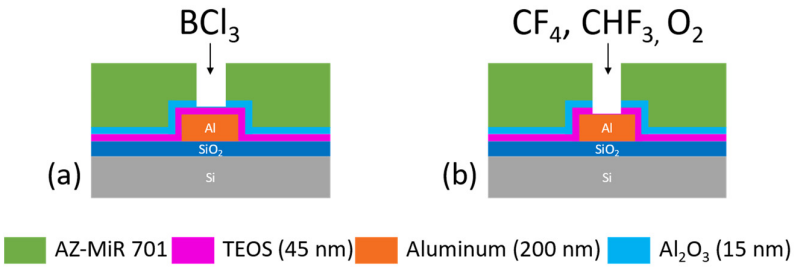

Figure 3. Cross-sectional depiction of the TEOS etch-stop method to selectively etch (**a**) Al_2O_3 and (**b**) PECVD TEOS over the buried Al gate electrode.

Moreover, the proposed process may also be applicable to other etch materials for similar device structures to this work. Other published studies have demonstrated the use of other high-k atomic layer deposited materials such as HfO_2 and TiO_2 [29,60] for graphene or 2D material-based devices. While most high-k ALD dielectric materials can be etched with chlorine-based gas chemistries, the proposed etch process provides great value with minimum process optimization, and it can be easily adapted for a wide variety of device structures.

A schematic top view of the tested GFETs is shown in Figure 4a indicating the gate length (L_{gate}), width ($W_{channel}$), and source/drain-to-gate gap ($Gap_{S/D\ to\ Gate}$). Although the fabricated devices are designed as dual-gated transistors, only one gate was tested at a time. Presented in Figure 4b are the I_{DS}–V_{GS} curves for 24 devices with identical device footprints with a channel width of 11 µm, a gate length of 12 µm, and a 1 µm source/drain-to-gate gap. The drain current levels range between 200 and 400 µA with a Dirac voltage between 5 and 8 V across the 24 reported devices. The average and standard deviation for the drain current at $V_{GS} = -10$ V are 292 µA and 54.5 µA, respectively, with a range of 106 µA and a non-uniformity of 63%. The average and standard deviation of the Dirac point are 6.6 V and 1.05 V, respectively, with a range of 3.8 V and a non-uniformity of 59%. Figure 4c shows a cross-section of the active area of the transistor, showing that the graphene goes over the 200 nm thick Al gate and under the Ni/Au source/drain metal contact pads.

Mobility was calculated using Equation (1) from the point of maximum transconductance, gm, of the I_{DS}–V_{GS} curves shown in Figure 4b. W is the width of the transistor, L the length, and C_{ox} is the capacitance per unit area of the gate dielectric. An estimated dielectric constant of 9.8 was used for mobility calculation. As a first approximation to characterize the entire batch of devices of this technology, the hole mobility was calculated with $V_{ch} = V_{DS}$, without taking into account the contact resistance. The average and standard deviation for hole mobility are 457.97 $cm^2/V{\cdot}s$ and 110.35 $cm^2/V{\cdot}s$ with a range of 396 $cm^2/V{\cdot}s$ and a non-uniformity of 93%. Figure S1 shows the histograms of Dirac voltage and hole mobility for these devices. The shape of the distributions confirms that the values obtained are not normally distributed; as such, it is justified to use the value of non-uniformity as a figure of merit to assess variability.

$$\mu = \frac{gm}{\frac{W}{L} \times V_{ch} \times C_{ox}} \quad (1)$$

The measured variation in the device electrical characteristics is typical of other similar reported graphene-based transistors [19,24,34,36,38,61,62]. The non-uniformity reported can be as large as 200% in some cases. In order to understand and investigate the large non-uniformity of the electrical characteristics of the tested devices and their correlation to the two-dimensional material qualities and properties, SEM, Raman, AFM, and electrical model fitting of trapped charged particles were performed on characteristic devices with high, medium, and low drain current levels, labeled as Devices 1, 2, and 3, respectively, in Figure 4b.

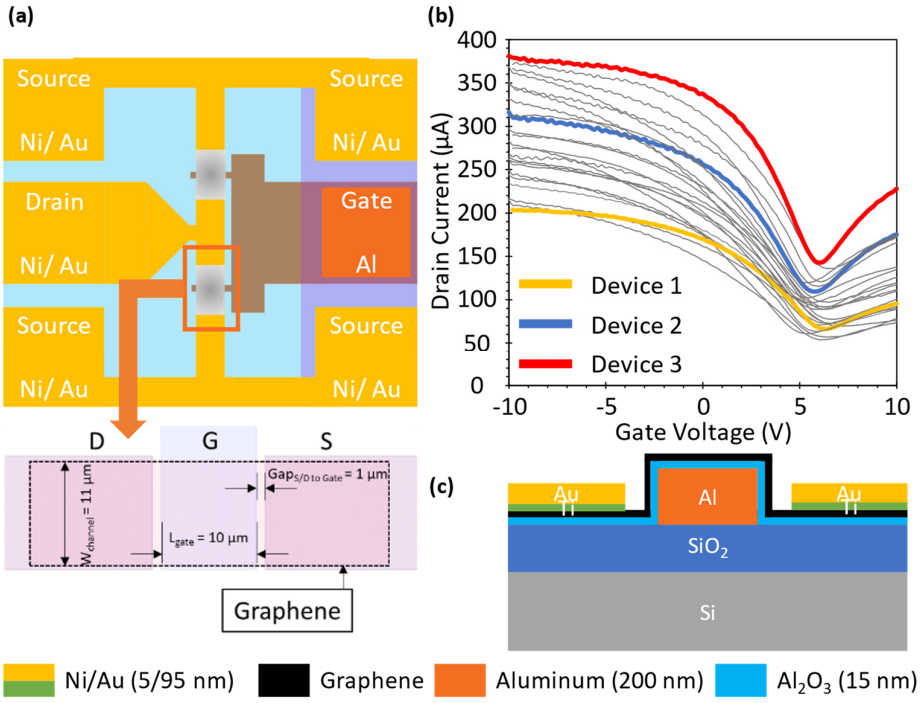

Figure 4. (**a**) Top view of a general GFET structure indicating the electrodes, gate length (L_{gate}) and width ($W_{channel}$), and channel gap ($Gap_{S/D\ to\ Gate}$). (**b**) Overlay of I_{DS}–V_{GS} of 24 identical devices. V_{DS} = 1 V for all these tests. Devices 1, 2, and 3 were selected for further analysis as representative of low, medium, and high current, respectively. (**c**) Cross-section of GFET channel structure where graphene (black) goes over the gate electrode step.

Figure 5 shows the SEM pictures and the related Raman spectra at different locations of three different devices on three separate die areas. These devices correspond to devices with low current (∼200 µA, Dirac point at 6.2 V), identified as Device 1, (Figure 5a,b), medium current (∼310 µA, Dirac point at 5.8 V), identified as Device 2 (Figure 5c,d), and high current (379 µA, Dirac point at 6.0 V), identified as Device 3 (Figure 5e,f), with current levels at a $V_{GS} = -10$ V and V_{DS} = 1 V. The SEM of Device 1 in Figure 5a shows that the source and drain are connected with graphene, and approximately 50% of its width is missing. Device 2 and Device 3 illustrate a relatively continuous graphene connection in the SEM image across the channel when compared to Device 1. However, some micro-tears between the gap of source and gate of Device 2 in Figure 5c may be observed, thus resulting in a slightly lower current readout than Device 3.

Traces A, B, and C in Figure 5b,d,f correspond to Raman spectra data of graphene collected in the regions on top of the gate, at the edge of the gate electrode, and in the gap between the source and gate electrode, respectively. The graphene supplied by Graphenea Inc., Cambridge, MA, USA. was inspected prior to transfer and showed a comparable Raman spectrum with Trace C confirming a monolayer of graphene as shown in Figure S2. The ratio of D (∼1350 cm^{-1}) and G (∼1600 cm^{-1}) peaks provides information on the state of disorder in the graphene crystal lattice [63]. A high D peak can be easily observed in Traces A and B in comparison to Trace C, indicating an increase in defect density wherever the Al is present. The increased defect density in these areas correlates to areas with rougher surfaces as observed with SEM in all three devices. In addition, the reduction in the 2D peak (∼2650 cm^{-1}) with respect to the G peak on the regions over the Al/Al_2O_3 (Trace A) indicates that the quality of the monolayer nature of the graphene is lost when compared to the regions away from the Al surfaces (Trace A) and even at the step edge (Trace B), as the Raman resonance may be influenced by the rougher surface. Further analysis of the defect density and separation is presented in the Supplementary Materials [64,65].

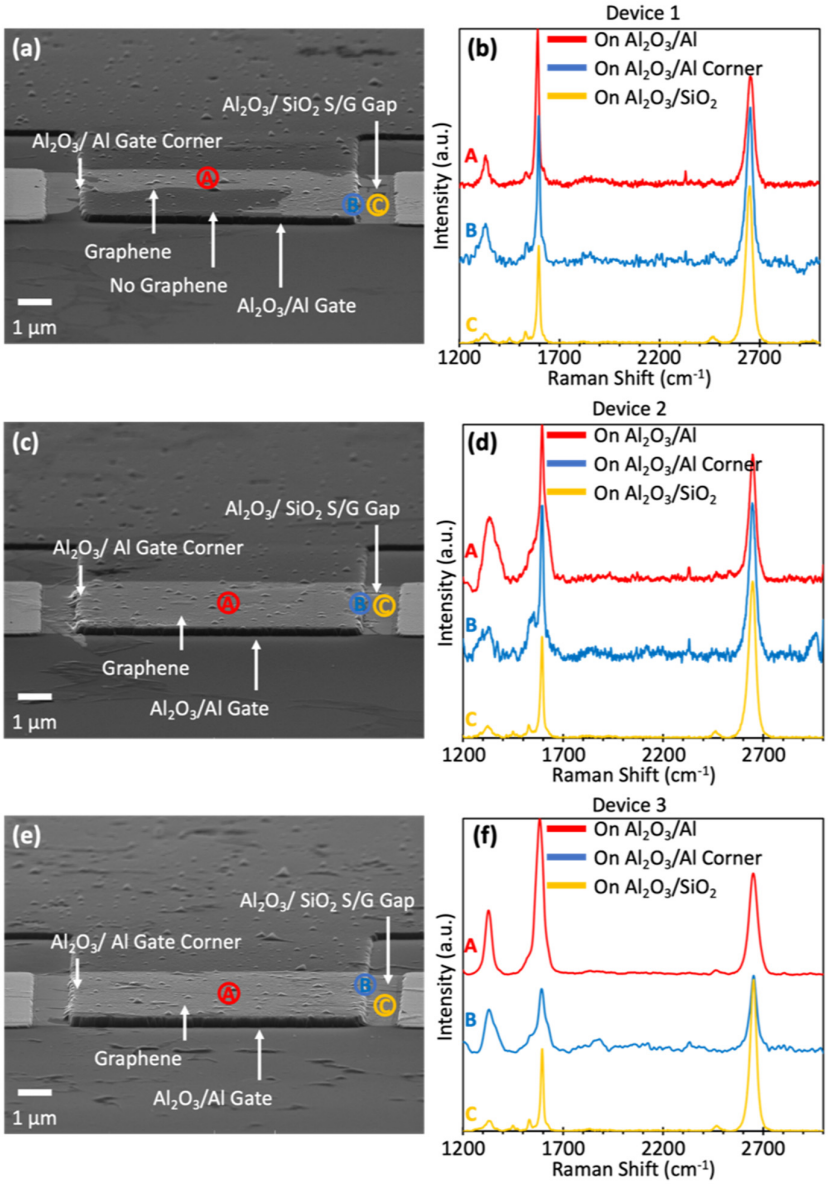

Figure 5. SEM pictures of fabricated GFETs, and Raman spectroscopic measurements of graphene at each indicated point (A, B, and C) in the fabricated devices for (**a**,**b**) Device 1 with a low current level of 200 µA (**c**,**d**) Device 2 with a medium current level of 310 µA, and (**e**,**f**) Device 3 with a high current level of 379 µA; all devices had $V_{GS} = -10$ V and $V_{DS} = 1$ V.

Atomic force microscopy (AFM) results are shown in Figure 6. These measurements were taken on the Al gate electrode (Figure 6a), at the gap between source/drain to gate (Figure 6b), and in an area without graphene (Figure 6c) for a surface roughness analysis comparison. The surface roughness R_a was 16.19 nm for graphene on the Al/Al_2O_3 gate electrode and 4.06 nm for the gate-to-source gap on the Al_2O_3/SiO_2 surface. Additional AFM on the Al_2O_3/SiO_2 surface without graphene yielded an R_a value of 1.06 nm. Thus, AFM analysis showed that the Al_2O_3 layer was not the cause of roughness on the aluminum gate electrode. With the Al gate electrode taking up more than 80% of the channel area, it is evident that the mobility of the devices may be heavily degraded due to the rough Al surface. Such results are in agreement with published work showing a decrease in mobility from 10^6 $cm^2/V{\cdot}s$ to 10^3 $cm^2/V{\cdot}s$ with just a modest increase in substrate surface roughness amplitude from 0.25 nm to 0.3 nm [66].

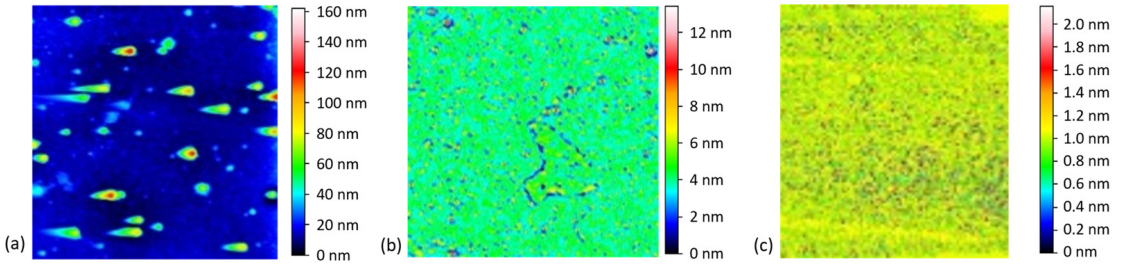

Figure 6. Atomic force microscopy (AFM) images with color scale bar indicating measured data of (**a**) graphene on Al_2O_3/Al gate electrode with arithmetic mean height (R_a) of 16.19 nm, (**b**) graphene on Al_2O_3/SiO_2 source and gate gap with R_a of 4.06 nm, and (**c**) bare Al_2O_3/SiO_2 with R_a of 1.06 with no graphene present in region.

SEM, AFM, and Raman analyses show that the surface of the aluminum gate electrode is not smooth and presents hillocks and irregularities when compared to the other material surfaces on the devices. In addition, the edge of the aluminum gate electrodes is rough, and the graphene layer does not appear to conform to this edge, resulting in wrinkles and/or a gap in some regions for all three devices. The leading factor contributing to the low mobility and large electrical non-uniformity reported here is attributed to graphene's underlying surface roughness of the Al gate electrode that can also be observed from AFM, Raman spectroscopy, and SEM imaging. It has been previously reported that the underlying surface roughness has a great effect on the mobility of graphene [66]. The random and non-uniform nature of the roughness results in carriers that are more prone to scattering effects traveling through defect sites in the graphene channel.

In order to show the impact of traps on the variation and non-uniformity of the fabricated buried top-gated graphene FETs, forward and backward V_{GS} sweeps with a staircase scheme and different bias stress conditions prior to the acquisition of the measurement data were performed. The Supplementary Materials show the results of this analysis for low, high, and medium devices, while the data presented here correspond to an additional device with high current level. The stress was set by applying V_{GS} pulses of 0 V and −10 V before measuring the drain current within a pulse of 500 µs duration. The total device resistance curves obtained under such conditions are shown in Figure 7. Data obtained with the 0 V pulse reveal a slight improvement in the hysteresis window with respect to the staircase, i.e., no pulse, scheme, whereas the case with higher stress (−10 V pulse) reduces the impact of traps. A hysteresis window is the result of trap charges on the gate dielectric interface. It is inherent to graphene field-effect transistors due to traps within channel, substrate, and high-k dielectric materials, as well as the interfaces between them. Technological efforts, such as encapsulation within two-dimensional dielectrics [67], additional costly processes [68], and high-quality interface between the graphene and the dielectric [33], have shown success in reducing trap charges and, thus, mitigating hysteresis. A pre-charging condition of the traps benefits the reproducibility conditions of devices with high-k dielectrics such as GFETs [69]. A well-known unipolar resistance GFET model [59] has been used to describe the experimental data in Figure 7 toward obtaining key device parameters such as the contact resistance and low-field constant mobility. The model accurately describes the data at each unipolar region, as observed in Figure 7; hence, parameters for p- and n-type regions were obtained for each measurement condition, as reported in Figure 7.

As shown in the data of Table 1 and Tables S1–S3 in the Supplementary Materials, the extracted contact resistance values have a smaller variation than the extracted mobility values for each particular device when comparing each of the test conditions. This indicates that the traps along the channel have a minimum impact for device variation and non-uniformity. On the other hand, there is large variation in the contact resistance values and the mobility observed between the devices. For example, high- and low-current devices have an extracted p-type contact resistance of 1.4 kΩ and 4.2 kΩ, respectively, as well as a

hole mobility of 185 $cm^2/V{\cdot}s$ and 315 $cm^2/V{\cdot}s$ and an electron mobility of 240 $cm^2/V{\cdot}s$ and 445 $cm^2/V{\cdot}s$, respectively. As shown in other reports [70], contact resistance can be affected by the defect density of the graphene layer, as it is more favorable to contact the graphene edge than the top surface. The graphene contacts are made under the metal layers and, thus, cannot be analyzed with Raman spectroscopy, although visual SEM inspections indicate a smooth and uniform surface. On the other hand, graphene non-uniformity has been reported as a result of wet PMMA transfers and could also have been the cause of the variation of contact resistance observed here [71].

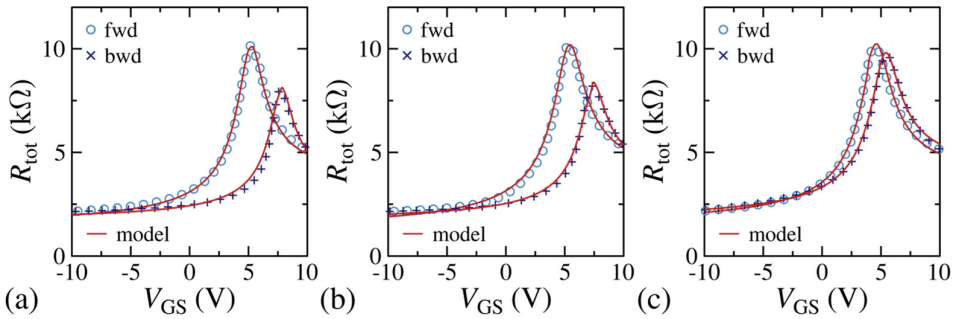

Figure 7. Total device resistance obtained with forward (fwd) and backward (bwd) sweeps of V_{GS} applied with (**a**) no bias stress, (**b**) a pulsed V_{GS} = 0 V prior to measurement, and (**c**) a pulsed V_{GS} = −10 V prior to measurement. Markers are experimental data and lines are modeling results.

Table 1. Extracted parameters of contact resistance, mobility, and density of carriers at Dirac point for a device from this technology.

Measurement Condition	$R_{c,p}$ (kΩ)	$\mu_{0,p}$ ($cm^2/V{\cdot}s$)	$R_{c,n}$ (kΩ)	$\mu_{0,n}$ ($cm^2/V{\cdot}s$)	n_0 (cm^{-2})
No pulse (forward)	1.37	185	3.45	240	3.52×10^{12}
No pulse (reverse)	1.67	285	3.07	355	3.18×10^{12}
Pulse 0 V (forward)	1.2	157	3.5	210	4.02×10^{12}
Pulse 0 V (reverse)	1.65	255	3.5	335	3.52×10^{12}
Pulse −10 V (forward)	1.41	165	3.5	215	3.92×10^{12}
Pulse −10 V (reverse)	1.65	182	4	255	3.81×10^{12}

As a point of comparison, Table 2 shows published large-scale integrated graphene-based devices, their process yield, and the most significant electrical results with their corresponding variation and non-uniformity. As seen in Table 2, variation and non-uniformity between devices can be observed across different graphene-based processes with typical NU values of 150% to 300%. Similar variation is reported across a broad range of processes including top, bottom, or buried gates and in processes targeting high-frequency performance and/or large-area sensors. This work, which is based on a buried local gate process, resulted in a non-uniformity as high as 93% on mobility values. In contrast, the work from Smith et al., which was based on a top gate process, reported a non-uniformity of 300% in mobility [34]. Lerner et al. reported the fabrication of global back-gate GFET sensors with hole mobility non-uniformities of 200% [36]. Tour et al. reported the fabrication and test of LIG gas sensors with a non-uniformity of 209% for device sensitivity to benchmarked gases [19].

Table 2. Reported high-volume fabrication results of GFETs.

Author	GFET Channel Structure	# of Devices	Non-Uniformity
This work, 2023	Local buried gate	24	Dirac point: 6.7 V, NU: 59% μ: 457.97 $cm^2/V{\cdot}s$, NU: 93%
Chen et al., 2021 [38]	Dual top gate	50	μ: 60 $cm^2/V{\cdot}s$, NU: 66.7%
Quellmalz et al., 2021 [24]	Top gate	18	μ: 2800 $cm^2/V{\cdot}s$, NU: 10.7%
Stanford et al., 2019 [19]	Back gate, LIG	10	Average sensitivity ($\Delta R/R_{He}$): 2.99, NU: 209%
Tian et al., 2019 [61]	Back gate	54	f_T: 8 GHz, NU: 75% f_{max}: 8 GHz, NU: 62.5%
Hong et al., 2018 [62]	Back gate	36	μ: 206 $cm^2/V{\cdot}s$, NU: 63% μPMMA: 180 $cm^2/V{\cdot}s$, NU: 542%
Smith et al., 2017 [34]	Top gate	4500	Dirac point: 4 V, NU: 150% μ: 40 $cm^2/V{\cdot}s$, NU: 300%
Lerner et al., 2016 [36]	Back gate	>12,000	Dirac point: 22.5, NU: 88% μ: 4945 $cm^2/V{\cdot}s$, NU: 200%

As show in this work through SEM, Raman, AFM, and model fitting, the roughness on the underlying surface of graphene plays a major role in the performance of the device as previously reported [66]. In addition, the graphene transfer process may induce defects or leave residues in the active and contact areas leading to additional variation. The presented analysis provides a framework with which other researchers can analyze and correlate device variation and non-uniformities while methods to reduce this variability are investigated. Device-to-device variability may be mitigated or improved with the use of smoother surfaces that would be beneficial for the fabrication of graphene-based FETs, as well as a more rigid transfer medium than PMMA that does not induce physical defects in the graphene during the transfer process. Advanced techniques such as thermal annealing and electron beam-induced cleaning have been reported to assist in an effective removal of PMMA residue that may induce device to device variabilities [72]. Techniques to obtain a smother surface include improved deposition techniques, electro-polishing, and/or the use of hBN [29,67].

4. Conclusions

In summary, a process was developed for the fabrication of buried locally gated graphene transistors with Al_2O_3 as a gate dielectric that can be suitable for not only flexible electronics but also LIG-based technology implementations. A new processing option was illustrated and presented with the use of TEOS as an etch stop for contact via etching of Al_2O_3. The proposed process is also compatible with other ALD materials such as HfO_2 and TiO_2. The process presented here resulted in Dirac points as low as 4 V with metal-to-graphene contact resistance as low as ~1.7 kΩ·μm. The hole mobility had an average of 457.97 $cm^2/V{\cdot}s$ with a non-uniformity of 93%. SEM, Raman, and AFM inspections were carried out to agree and validate that an inconsistent graphene channel area, degraded monolayer characteristic, and heavily roughened Al/Al_2O_3 surface were the main factors contributing to electrical performance non-uniformity. In addition, model fitting indicated that the extracted contact resistance values had a smaller variation than the extracted mobility values for each particular device when comparing each of the test conditions. This indicated that traps along the channel had a minimum impact on device variation and non-uniformity. On the other hand, there was large variation in the contact resistance values and mobility observed between devices, the latter still being a consequence of the Al roughness. The results presented demonstrate the need to reduce device variability and non-uniformity by improving not only transfer methods but also the use of smoother surfaces and compatible materials. The presented analysis provides a framework with

which other researchers can analyze and correlate device variation and non-uniformities while methods to reduce variability are investigated.

Supplementary Materials: The following supporting information can be downloaded at https://www.mdpi.com/article/10.3390/app13127201/s1: Figure S1. (a) Dirac point voltage and (b) mobility distribution of 24 identical devices; Figure S2. (a) Overlay of I_DV_G characteristics. (b) Raman of starting graphene on copper foil; Figure S3. IV curve of fabricated GFET without gate bias for ohmic behavior observation; Figure S4. I_D–V_G curve of (a) graphene GFET S-10 and (b) RIT Nanofab fabricated GFET with device dimensions of W/L = 100/80 µm; Table S1. Average defect separation and density of each inspected Raman sample; Table S2. Extracted parameters of a low max IDS (≤200 µA) sample device for contact resistance, mobility, and density of carriers at Dirac point for a device from this technology; Table S3. Extracted parameters of a medium max IDS (>275 µA) sample device; Table S4. Extracted parameters of a high max IDS (>350 µA) sample device.

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