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Impact of the W etching process on the resistive switching properties of TiN/Ti/HfO_2/W memristors

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ABSTRACT

In this work, we investigate the effects related to the etching process of the W bottom electrode (BE) on the breakdown voltages and the resistive switching (RS) characteristics of TiN/Ti/HfO_2/W memristors. Two different W-BE etching processes are compared: anisotropic dry etching and isotropic wet etching. In order to complete the analysis, scanning electron microscope inspections are used to investigate the profile of the patterned BE. Finally, the hysteretic current–voltage (I-V) characteristics are simulated using the Dynamic Memdiode Model (DMM).

1. Introduction

MIM structures can exhibit memristive properties under appropriate biasing conditions. The main feature of this phenomenon is the occurrence of a pinched hysteresis I-V loop associated with reversible changes of the device resistance state. This constitutes an emerging technology which is currently being investigated for a wide number of applications such as non-volatile memories, hardware security, as well as brain-inspired computing systems [1]. In recent years, numerous studies have explored different materials and structures to optimize the device performance [2]. Other research efforts have focused on developing memristor-based circuits for specific applications, such as pattern recognition and synaptic emulation. However, although the RS phenomenon has been observed in various material combinations in MIM structures, many issues are still open concerning the impact of the fabrication processes on the switching mechanism, and therefore on the overall device performance [3]. Therefore, a deep understanding of the influence of these fabrication processes is crucial in order to enhance the performance and reliability of memristor devices. The filamentary-type RS in Ti/HfO_2 devices [4–6] is attributed to the formation and partial rupture of a conductive filament (CF) formed by oxygen vacancies. In this case, the Ti capping layer serves as an oxygen scavenger, enhancing the RS performance. In this work, we evaluate the impact of the etching process of the W-BE on the RS characteristics of TiN/Ti/HfO_2/W memristors. Our aim is to gain valuable insights into how fabrication techniques, specifically the etching process, can effectively impact the resistive switching (RS) behavior and overall device performance through a systematic investigation. Additionally, for the sake of completeness, the experimental I-V characteristics are simulated using the DMM [7].

2. Experimental

The fabricated devices are TiN/Ti/HfO_2/W structures [4] in a cross-point configuration with a size of 5x5 μm^2 (Fig. 1 (a)). The devices were fabricated on silicon wafers with a thermally grown 200 nm-thick SiO_2 layer. A 100 nm-thick W-BE was deposited by magnetron sputtering and patterned by photolithography. Two different W-BE etching processes were evaluated (anisotropic dry etch and isotropic wet etch). For the anisotropic dry etching, the devices were patterned by using an Alcatel 601E inductively-coupled plasma reactive ion etcher with an SF_6 /O_2 plasma, whereas for isotropic wet etching, an H_2O_2 solution with a 30% concentration was used as the etchant [8]. Subsequently, the 10 nm-thick HfO_2 layer was deposited by atomic layer deposition at 225 °C

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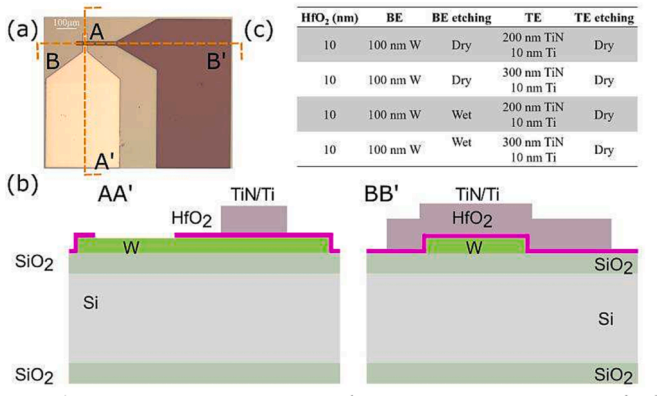

(c)

HfO_2 (nm)	BE	BE etching	TE	TE etching
10	100 nm W	Dry	200 nm TiN 10 nm Ti	Dry
10	100 nm W	Dry	300 nm TiN 10 nm Ti	Dry
10	100 nm W	Wet	200 nm TiN 10 nm Ti	Dry
10	100 nm W	Wet	300 nm TiN 10 nm Ti	Dry

Fig. 1. (a) Top view optical microscope image of the fabricated devices. (b) Schematic cross-sections AA' and BB' from the regions indicated by the dashed lines in (a). (c) Split table of the fabricated memristors.

using TDMAH and H_2O as precursors and N_2 as a carrier and purge gas. Next, the top electrode (TE), consisting of a metal stack of 200 nm or 300 nm-thick TiN on a 10 nm-thick Ti, was deposited by magnetron sputtering and patterned by photolithography and dry etching. A schematic cross-section of the fabricated devices is shown in Fig. 1(b). The split table of the fabricated devices is shown in Fig. 1(c).

The I-V measurements were performed using a *Keysight B1500 SPA* and controlled using Matlab. The electrical characterization has been complemented by structural characterization carried out with a *ZEISS Crossbeam 550 L* focused-ion beam-scanning electron microscope (FIB-SEM).

3. Results and discussion

To investigate the influence of the etching process on the profile of the patterned BE, top view and cross-sectional scanning electron microscope (SEM) inspections of the pristine devices were performed, as shown in Fig. 2. The obtained results show that, as expected, abrupt profiles of the pattern are obtained for anisotropic dry-etched devices (Fig. 2(a)), whereas, for the isotropic wet-etched cases, the BE profiles are gradual (Fig. 2(b)). This analysis reveals that the dry etching process leads to devices with potentially "weak" regions at their edges.

The typical conduction characteristics of the pristine devices are shown in Fig. 3. The results point out that the devices with the BE fabricated by wet etching show slightly higher leakage current compared to those fabricated by dry etching. The Weibull cumulative distribution function [9] for the breakdown voltage (V_{BD}) is defined as:

$$F(V_{BD}) = 1 - \exp[-(\frac{|V_{BD}|}{\alpha})^{\beta}] \quad (1)$$

where α is the voltage at which 63.2% of the devices break down, and β is the Weibull slope, which is a measure of the spread of the distribution. The Weibull distributions for V_{BD} (positive and negative polarities) are shown in Fig. 4. The results indicate that there is no substantial influence of the etching process and the TiN thickness on the V_{BD} distributions.

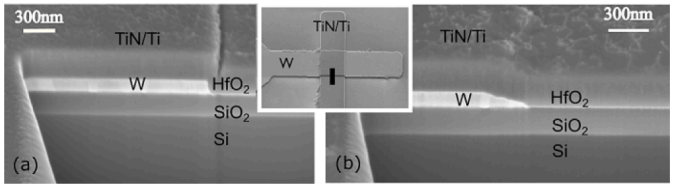

Fig. 2. Cross-sectional SEM inspections for devices with the W-BE patterned by (a) anisotropic dry etching and (b) isotropic wet etching. The inset shows a top SEM image (dry etch).

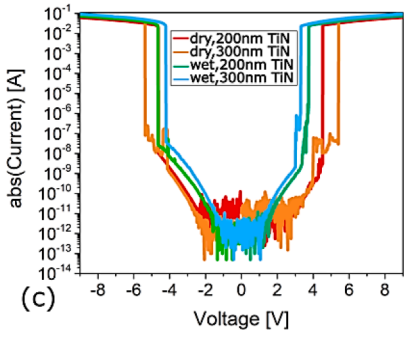

Fig. 3. Typical pristine I-V characteristics of the fabricated devices.

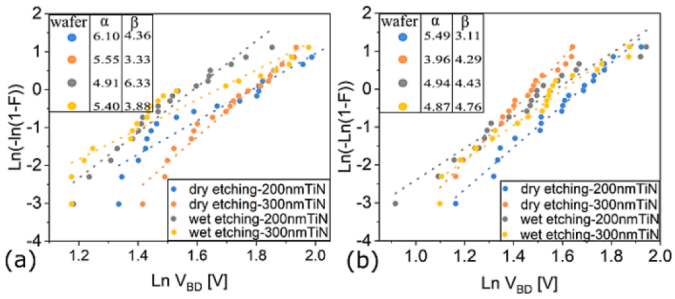

Fig. 4. Weibull plots of the breakdown voltage for 20 devices measured at (a) negative and (b) positive polarities. The inset shows the α and β parameters.

Fig. 5(a) shows typical I-V characteristics of the fabricated devices obtained by applying a voltage ramped stress (VRS) from 0 V to −12 V. The results show that, as expected, at the hard breakdown, a sudden current increase occurs. However, when the voltage is increased further, the current suddenly drops, indicating that the device has been disconnected [9,10]. This behavior was observed in about 30% of the cases for both kinds of devices under negative VRS.

To gain further insight into the failure mechanism, top-view SEM inspections were performed on stressed devices (Fig. 5(b-d)). The results reveal damage regions in all the devices subjected to negative VRS. In 80% of the tested devices, the damaged regions were located around the profile of the pattern of the BE, indicating that the device perimeter is more prone to suffer failure events. In contrast, only dry-etched devices showed damage when subjected to a VRS with a positive DC sweep from 0 V to 12 V.

For the characterization of RS, the initial step involves an electroforming process. This process entails applying a positive voltage ramp until the current reaches 1 mA. The purpose of the forming process is to transition the devices from a pristine state to a Low Resistance State (LRS). Following the forming process, a reset process is carried out to change the state to a High Resistance State (HRS) by applying a negative double sweep ramp from 0 to −1.4 V. After completing the forming and reset processes, a series of 100 cycles of set-reset cycles are performed. Fig. 6 shows the typical RS characteristics obtained for the different fabrication processes by applying DC double sweeps for the set and reset processes, with voltage limits of + 1.1 V and −1.4 V, respectively. The results reveal significant differences in the RS behavior exhibited by the devices fabricated with dry and wet etching. The wet-etched devices show less cycle-to-cycle (C2C) variability and more gradual reset transitions than dry-etched devices. These findings highlight the influence of etching conditions on the RS performance of the devices and emphasize the need for careful consideration of such process in device design and optimization. The abrupt reset transition observed in the dry-etched devices is influenced by the presence of an intrinsic series resistance (R_{series}), which is larger for the dry-etched devices ($R_{series_dry} \sim 210\ \Omega$)

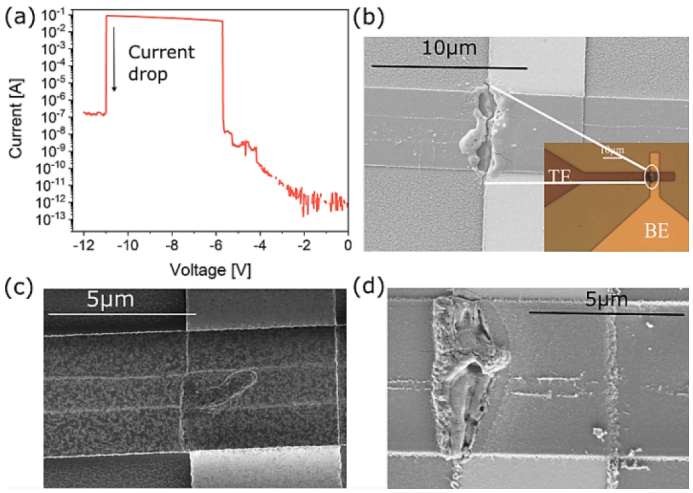

Fig. 5. (a) Typical I-V characteristic of melted structures in dry-etched devices after applying a voltage ramped stress. SEM images of melted devices fabricated using (b), (c) dry etch, and (d) wet etch.

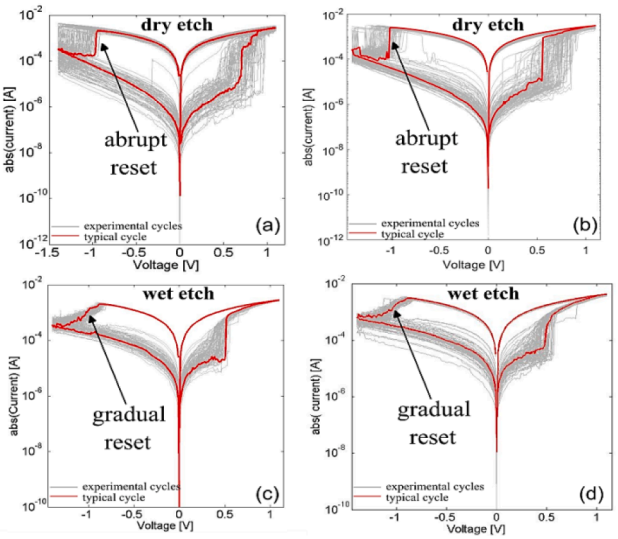

Fig. 6. Typical I-V characteristics for 100 RS cycles of devices fabricated with (a),(c) 200 nm and (b),(d) 300 nm TiN top electrode, and with the W BE patterned by (a),(b) dry etching and (c),(d) wet etching.

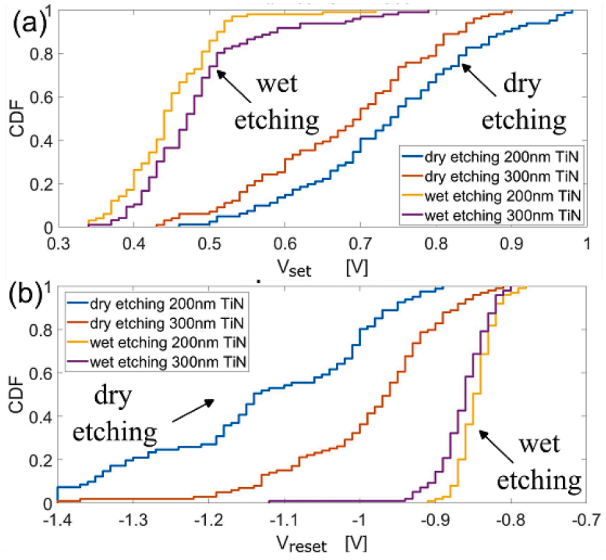

Fig. 7. Cumulative distribution functions of (a) V_{set} and (b) V_{reset} for 100 RS cycles of the different types of devices.

compared to wet-etched ones ($R_{series_wet} \sim 165\ \Omega$). Notice that R_{series} largely affects the shape of the reset curve [4]. Additionally, the Joule heating effect could be another factor that could impact the abruptness of the reset process in dry-etched devices. As a result of the larger set currents in these devices, the electric field and temperature-assisted oxygen ion migration processes may accelerate the partial dissolution of oxygen vacancy-rich conductive filaments at the reset point, leading to a sudden increase in resistance [11]. It is worth noting that a gradual reset behavior is highly desirable for analog applications, as it enables better control over the memristor resistance state.

The cumulative distribution functions of the switching voltages and the HRS and LRS resistances, extracted at −0.1 V, are represented in Figs. 7 and 8, respectively. It is important to note that the dry-etched devices show higher switching voltages (Fig. 7) and larger C2C variability of the RS parameters compared to the wet-etched structures (Figs. 7 and 8). Furthermore, the R_{HRS} in dry-etched devices is more than one decade larger than that in the wet-etched devices, and shows larger C2C variability, while the R_{LRS} is very similar for both types of devices (Fig. 8). These results point out that devices with the BE patterned by dry etching exhibit a larger memory window (see Fig. 6).

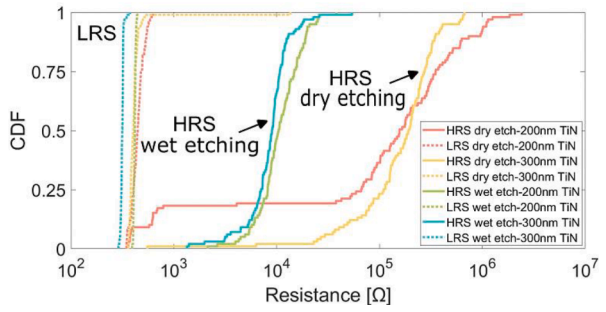

Fig. 8. Cumulative distribution functions of the HRS (solid line) and LRS (dotted line) resistances obtained at −0.1 V for 100 RS cycles of the different types of devices.

In order to investigate the impact of oxygen ion/vacancy migration processes on the resistance states, the connection between the R_{HRS} and R_{LRS} values in the cycle (i + 1) versus the values for the previous cycle (i) are evaluated (Fig. 9(a) and 9(b)). The results indicate that the dry-

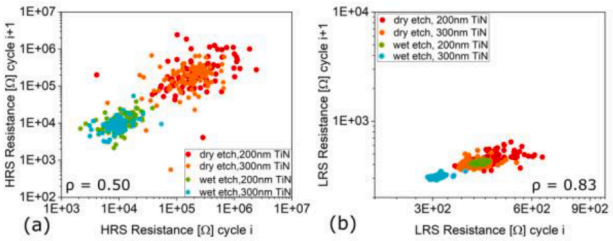

Fig. 9. Correlation plots between the (a) HRS and (b) LRS resistances at the cycle i + 1 versus the previous cycle i.

etched devices showed a larger dispersion of RS parameters compared to the wet-etched cases. It has been found that the R_{HRS} and R_{LRS} parameters are statistically correlated between successive cycles, with Pearson correlation coefficients (ρ) of 0.50 and 0.83, respectively. The correlation analysis suggests that the filamentary strength, given by the CF size and stoichiometry, plays a significant role in determining the RS parameters for the subsequent cycle.

4. Dynamic Memdiode model

The experimental RS I-V curves were modeled and simulated using the DMM. The model consists of two coupled equations: one for electron current that flows through a filamentary-type conducting structure (2) and a second equation representing the reversible movement of vacancies/ions within the dielectric layer caused by the application of an external electrical stimulus (3) [12]. The I-V relationship is given by the expression:

$$I(V) = I_0(\lambda) sinh\{\alpha(\lambda)[V - (R_C(\lambda) + R_{SB})I(V)]\} \quad (2)$$

where V is the voltage drop across the device terminals, I_0 is the current amplitude factor, α is the slope factor, R_{SB} is the snapback resistance and R_c is the constriction resistance. The memory state of the device, λ, is described by the following differential equation:

$$\frac{d\lambda}{dt} = \frac{1-\lambda}{\tau_S(\lambda, V_{CT})} - \frac{\lambda}{\tau_R(\lambda, V_{CT})} \quad (3)$$

where τ_S and τ_R are the set and reset characteristic times, respectively and $V_{CT} = V - I \cdot R_{SB}$.

Fig. 10 shows simulated curves using the DMM both for the gradual (analog) and abrupt (digital) reset transitions corresponding to wet-etched and dry-etched devices, respectively. The observed variations in the resistive switching (RS) behavior among the different devices can be attributed to the RS mechanism involving the migration and recombination processes of oxygen vacancies/ions. These processes are influenced by both the electric field and the temperature, with the latter being enhanced by Joule heating. It is worth noting that the fabrication processes of the devices play a significant role in defining the experimental electrical behavior, as well as the RS characteristics and the associated model parameters. Notice that good agreement between the experimental data and the model curves is obtained. These results indicate that the electrical behavior of memristors with abrupt or gradual resistance state transitions, and with different resistance levels, can be correctly reproduced using the DMM. These findings demonstrate that the premises of the DMM apply to the devices investigated in this work.

5. Conclusions

This work demonstrates that the profile of the pattern present in cross-point RS structures must be carefully considered, as these regions can strongly affect the operating conditions of memristive devices and their potential applications. It has been shown that the wet etching process for the W bottom electrode in TiN/Ti/HfO_2/W memristors presents a larger robustness compared to the dry-etched case. Additionally, wet-etched devices exhibit lower intrinsic series resistance, lower switching voltages, lower cycle-to-cycle variability, and a more gradual reset profile. The DMM modeling results provide a comprehensive analysis of the pinched hysteresis I-V loop of the devices fabricated under different processing conditions. This work highlights the impact of the etching process on the memristor performance and provides useful guidelines for optimizing the processing steps to achieve desired device properties for potential applications.

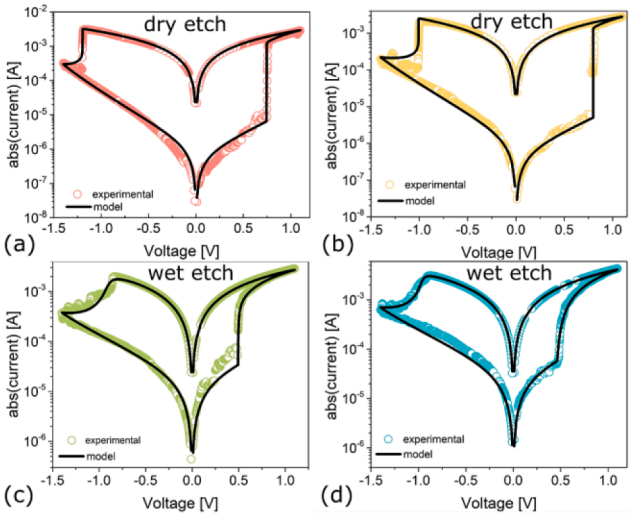

Fig. 10. Experimental (symbols) and modeled (solid line) typical I-V characteristics of devices fabricated with (a), (c) 200 nm and (b), (d) 300 nm TiN top electrode, and with the W-BE patterned by (a), (b) dry etch and (c), (d) wet etch.

Declaration of Competing Interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: Mercedes Saludes reports financial support was provided by Microelectronics Institute of Barcelona..

Data availability

Data will be made available on request.

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