A smart measurement system for the combined nanoscale and device level characterization of electron devices: implementation using ink-jet printing technologies

Sergi Claramunt, Javier Arrese, Ana Ruiz, Marc Porti, Albert Cirera, Montserrat Nafria

***Abstract*—In this work, the integration into a single measurement system of device level and nanoscale measurement equipment is presented and applied to the electrical characterization of emerging electron devices. This system is a smart solution to simplify the test procedure, since it allows a fast switching between measurement modes (device or nanoscale level), also featuring an enlarged testing capability. Key in the system is a custom-made inkjet-printed circuit board (I-PCB) that connects the device terminals to the proper instrumentation. The flexibility offered by inkjet-printing technologies is a clear advantage, since many kinds of devices can be tested, without the need of expensive hardware modifications. As a particular case of study, the proposed strategy is demonstrated by implementing a system that alternates between standard electrical measurements with a Semiconductor Parameter Analyzer (SPA) and Conductive Atomic Force Microscopy (CAFM) nanoscale measurements on back-gate graphene field-effect transistors.**

***Index Terms*— ink-jet printing, graphene transistor, electrical measurements, CAFM, HCI degradation**

I. Introduction

EMERGING devices that take advantage of the electronic properties of alternative materials or of low-cost fabrication techniques (as for example, 2D materials-based devices [1, 2], Thin Film Transistors (TFTs) [3, 4, 5], or inkjet-printed devices [6, 7]) are preferred to their Si-Based counterparts in some applications because they offer, among others, higher mechanical flexibility [8, 9], transparency [10, 11] or mobility [12]. However, these technologies are still in their infancy, and understanding issues such as their device-to-device (or time-zero) variability and reliability is essential to introduce suitable countermeasures into the fabrication processes, device architecture and/or circuit design. Taking as example graphene-based devices, nanoscale defects, as Grain Boundaries (GB), wrinkles and corrugations, can appear in the graphene layer, which have been proved to hinder its electrical properties [13], negatively affecting the corresponding device performance. This kind of variability can be studied at two different levels. We can analyze the variability at device level (Fig.1a) on fully developed devices using standard electrical characterization techniques (which require wafer probe stations and instruments such as Semiconductor Parameter Analyzers, SPA) [14, 15] to evaluate the impact of the fabrication processes on the device performance. On the other hand we can study the variability at material level. In this case, we can measure some properties of the material that may impact on the device electrical characteristics, like crystal structure [16], chemical content [17] or morphology [18]. In this regard, measurement techniques with nanoscale resolution (Fig. 1b), as Atomic Force Microscopy (AFM) related techniques, have

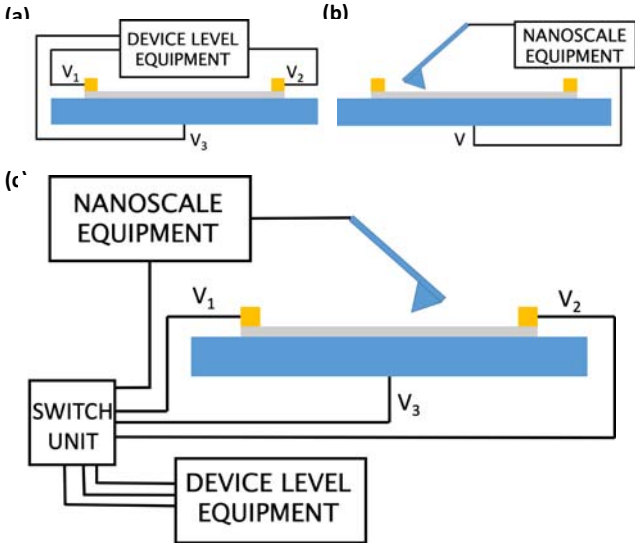

Fig. 1. (a) Scheme of the configuration corresponding to typical device level measurements. A back-gate GFET is shown, as a particular device example (b) Configuration corresponding to the nanoscale electrical measurements. (c) Schematic diagram of the presented general connection strategy for combined device and nanoscale level electrical measurements

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been shown to be very powerful to get topographical and electrical information at the nanoscale of materials and devices [19, 20, 21]. Among them, the Conductive AFM (CAFM) allows to measure, simultaneously to the topography, the conductivity of the sample under study [22-28]. When the CAFM tip is in contact with a given material it plays the role of the top electrode (Fig. 1b), with a contact area that corresponds to the contact region between the tip and the sample [29]. Since this area can be very small (~100 nm^2, on dielectrics [30]), the technique allows the nanoscale electrical characterization with a resolution of ~10 nm. In these tests, the vertical current through the materials stack is measured when a voltage difference is applied between the bottom electrode and the conductive tip (Fig. 1b) [31, 32, 33]. Although the current dynamic range of a standard CAFM was limited to only three orders of magnitude (from, for example, ~pA to ~nA), it was extended from nA to mA [34, 35] in order to spread the capabilities of the technique and be able to study, for example, the reliability of gate oxides [36]. In spite of that, this configuration may be not enough in some cases.For example, for devices with more than two electrodes (as Graphene Field-Effect Transistors (GFETs) or TFTs) where the lateral conduction through the channel plays a key role. Some works have already studied the lateral conduction of alternative materials deposited on a substrate [37, 38, 39]. However, to the best of the authors' knowledge, the lateral conduction in fully processed operative devices at the nanoscale has not yet been addressed.

Though reliability of emerging devices is crucial for their commercialization, its study is still limited. As for Si-based devices, aging mechanisms [40], as Bias Temperature Instabilities (BTI) and Hot Carrier Injection (HCI) degradation have been observed in GFETs [41]. These mechanisms will introduce a time-dependent variability during the device operation in the circuit, so that drifts of key device parameters (as threshold voltage and carrier mobility) occur, which negatively impact the circuit performance. Aging has been related to the generation of defects in the materials and it is usually characterized at device level through Measurement-Stress-Measurement (MSM) tests, which customary involve wafer probe stations and SPAs [14, 42]. From these tests average information of the device aging can be obtained but nanoscale details cannot be revealed. With the aim of correlating nanoscale and device level aging effects, in [43], the authors combined CAFM measurements with SPA analysis to evaluate the impact of electrical stresses at different regions along the channel of a MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor), with a spatial resolution in the nanometer range. However, in that case, only the impact at the end of the test sequence could be evaluated: the test was destructive because the metal gate should be removed to expose the dielectric material before the CAFM measurement . Moreover, only vertical current measurements were allowed. In addition, the measurement process was very time consuming as the sample had to be physically moved from the wafer-probe station to the CAFM holder and thenthe stressed transistor localized on the piece of wafer and the tip located on the suitable scan area. From the above, it can be concluded that understanding the sources of time-zero and time-dependent variability (related to the fabrication process and/or the device operation) and their impact on the device behavior is essential for technology development. Since variability is mostly related to nanoscale materials properties (grain boundaries, defects…), a combination of nanoscale and device level measurements is required to get complementary information and build a complete picture of the overall phenomena. In this work, we developed a smart flexible experimental set-up (Fig. 1c), implemented at the UAB laboratories, that combines nanoscale AFM-related tests with standard electrical measurements at device level on fully processed electron devices. The devices have the active layer exposed to air, so that it is not required any destructive sample preparation. By integrating all the needed equipment into a unique measurement system, the proposed solution simplifies the testing procedure and also enlarges the capabilities of the system (Fig. 1c). To show its large capabilities, measurements on as-grown and stressed back-gate GFETs are shown.

II. Architecture of the Measurement System

Without loss of generality, in this work, it will be considered that a CAFM and a SPA are used for the nanoscale and device level tests, respectively; also, that DC voltages are needed for biasing and that currents have to be measured. So, with this aim, we integrated the CAFM and the SPA in the same measurement system, in which the sample is located on the CAFM holder. Note that a wafer probe station is not required, so that the cost of the system is reduced. Figure 2 presents the equipment diagram of the complete developed set-up. A PC is in charge of the configuration of the hardware, the execution of the user-defined test sequence and the data acquisition. The use of the SPA or the CAFM (or both simultaneously) for biasing/measuring can be selected, depending on the configuration of the *switch unit (*Fig. 2*, blue box).* A key point in the system is the connection of the instrumentation to the device terminals. With this purpose, we designed a custom-made inkjet-printed circuit board (I-PCB), whose layout defines the device-instrumentation connectivity, that is attached to the microscope holder.. All the needed connections are routed through a RJ45 connector (green line in Fig. 2) to ease the

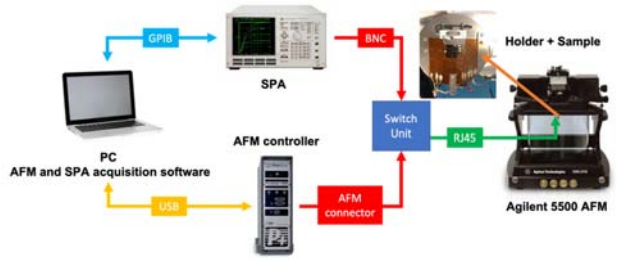

Fig. 2. General equipment diagram of the developed set-up. The sample is located on the AFM holder and a I-PCB defines the connectivity of the device electrodes. A RJ45 interface is used as a connection between the I-PCB and the switch unit. Measurements with the SPA and CAFM can be done, depending on the configuration of the switch unit.

operability of the proposed system. More details on the I-PCB and device connection will be given in the next section.

As an example of operation, the system can be configured to carry out device level MSM reliability tests, combined with nanoscale measurements (Fig. 1c). For these tests, first, the switch is configured to use the SPA (the CAFM tip is not in contact with the device), which, by correctly biasing the device, will be in charge of stressing and measuring the stress effects at device level as in Figure 1a. After that, the CAFM is connected to the device (by correctly configuring the switch unit) and the device is contacted by the CAFM tip (now, the drain of the device is not connected to the SPA). Then, the CAFM will measure the stress effects at the nanoscale (Fig. 1b). In addition, by providing the suitable biasing, lateral nanoscale conductivity measurements will be also feasible. To stress and measure again at device level, the CAFM tip is lifted (but not moved on the X-Y direction) and the switch unit configured to connect the SPA to the sample holder to stress/measure again the device. This sequence (stress-measure at device level and measure at the nanoscale) can be repeated as many times as defined by the user. Note that, since the tip position on the sample was not moved while doing the device level tests, if the drifts of the AFM are somehow controlled (for example with a closed-loop), the effect of sequential stresses on a particular area of the device can be analyzed. Moreover, in this example, SPA and CAFM are not stressing/measuring simultaneously, so that the measurements performed by one of them are not affected by the integration of the other in the system.

From the description above, it can be concluded that the key point in the system is how to easily change the connection of the device terminals from the CAFM electronics to the SPA and vice versa. This means that, first, the CAFM holder must be prepared for that, and second, the device must be connected to the holder. As for the first issue, on the one hand, holders provided by equipment manufacturers only allow the most common connections (Fig. 1b), and, on the other, the required connections are dependent on the particular contact pad configuration of the device under test (DUT). Therefore, standard CAFM holders are not practical for this purpose. Of course, equipment manufacturers could fabricate ad-hoc holders for each particular measurement need, but this would be expensive, little flexible and very time consuming, so this alternative can be ruled out. To overcome those limitations, we propose a low-cost very-flexible solution, which consists in the fabrication of a device-instruments connection interface, taking advantage of the versatility of ink-jet printing techniques [44, 45]. In particular, we propose the fabrication of a I-PCB, with a suitable layout that, when stuck on the CAFM holder, defines the connectivity of the holder to the CAFM and the SPA (Fig. 3a). Note that, once the I-PCB is printed, DUTs with the same contact pad distribution could be analyzed with the system. Since the connection layout can be easily changed, the solution provides large flexibility.

The second point refers to the connection between the device and the I-PCB paths. In this regard, a critical aspect is how the paths of the I-PCB are connected to the electrodes of the DUTs. Wire-bonding would be a traditional solution. However, since CAFM measurements must be performed, this option has the important disadvantage that the wires could obstruct the tip movement while scanning the surface. To overcome this problem, again, ink-jet printing offers a solution, since its resolution is sufficient to print paths inside the test chip to make the DUT connections without compromising the other devices, as it will be shown in section III when a particular case is studied. Using this technique, since the connections between the DUT and the I-PCB are printed, they are planar (just several nm high) allowing the free movement of the AFM tip over the surface of the sample.

III. Design of the I-PCB: A Case of Study

Until now, we have described the general concept behind our system, where the I-PCB design is crucial. Depending on the architecture of the DUTs, their location in the chip and the measurements of interest, a specific I-PCB layout will have to be designed and printed. In this section, as a particular example, an I-PCB to characterize back-gated graphene-based transistors (GFET, with its channel exposed to air) combining a CAFM and a SPA is presented (Fig. 3a and b). The back-gated GFETs

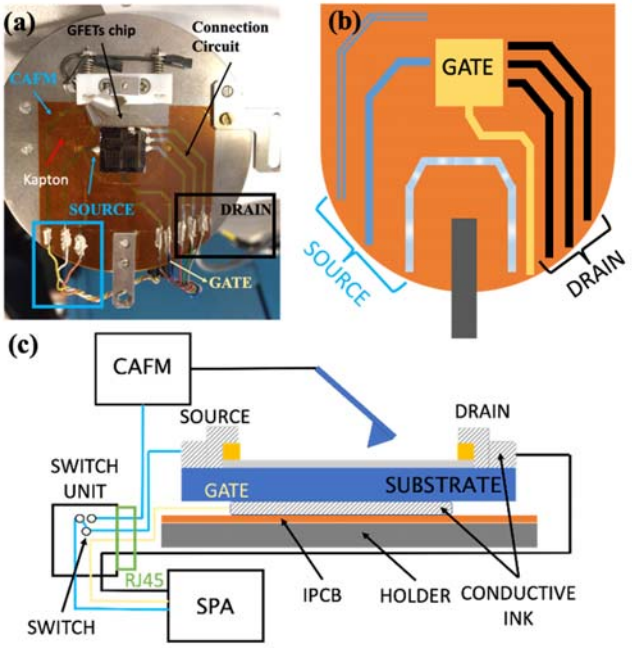

Fig. 3. (a) Photograph of the ink-jet printed connection circuit mounted over the AFM holder. It can be seen the auto adhesive I-PCB (orange-colored tape), the graphene transistor chip at the center and the connections corresponding to the drain electrodes (black box) and to the measurement systems (blue box). (b) Scheme of the printed paths over the auto adhesive Kapton. Each color corresponds to the different electrodes of the GFET. Black, gold and blue correspond to the paths connected to the Drain, Gate and Source of the devices, respectively. In the case of the source, the solid blue corresponds to the path connected to the chip, the double-lined path is connected to the AFM electronics and the light blue path to the SPA. (c) Cross-section of the I-PCB developed in this work for the analysis with a SPA and a CAFM of back-gate GFETs. The interface circuit allows to perform in-situ electrical measurements at device (with the SPA) and at the nanoscale (with CAFM). The switch unit allows the change of measurement modes changing the connections at the source electrode.

were fabricated on a SiO_2/Si substrate with an oxide thickness of 80 nm [46]. In our case, since the oxide thickness of the GFETs is very large and no tunneling current through the oxide could be measured by CAFM, the I-PCB has been designed in order to measure lateral currents only at the nanoscale. Therefore, the designed I-PCB allows the connections of the GFETs to either a CAFM (in order to measure topography and current through the channel) or the SPA, in order to stress or measure the electrical properties of the device.

Fig 3a and 3b show, respectively, a picture and a scheme of the I-PCB. In our case, the I-PCB has been designed to characterize three of the GFETs in the chip. The I-PCB will connect the GFETs with the different external instrumentation (SPA and CAFM). The interconnection lines have been ink-jet printed over an auto adhesive insulator polymide strip (Kapton, 50 µm thick, orange color material in Fig. 3a) using the conductive ink Siverjet DGP HR (ANP, South Korea, grey paths in Fig. 3a). The printing process was implemented at the UB laboratories and was done using a Dimatix printer with a 1 pl cartridge, which corresponds to roughly 20 µm track width (depending on the substrate surface energy) [47]. After the silver path printing, a sintering process, i.e, an annealing in vacuum, was performed to eliminate the organic components of the ink and make the printed path conductive [48]. It is important to emphasize that during the sintering process, the device properties could also change. In the case of the graphene based devices (as the samples analyzed in this work), such kind of process is usually used to clean the surface and improve the electrical properties of graphene [49]. Therefore, it is neither destructive nor detrimental for the material but, on the contrary, helps to improve its electrical properties. Then, the I-PCB is adhered on the existing AFM holder (Figs. 3a/c). In Fig. 3b a scheme that clearly shows the 7 ink-jet printed connection paths of the I-PCB is presented. On the right side, there are three paths (black) that will contact the drain electrodes of three different GFETs. These electrodes are connected to a Source-Measurement Unit (SMU) by means of a selector in the switch unit. The gold-colored path in Fig. 3b corresponds to the gate connection, which contacts the bottom part of the chip and will act as the Gate electrode. In our case, the gate is common to the three selected devices. The gate path ends in a square shaped region in which the chip will be adhered using an isotopically conductive (ICA) silver epoxy (CircuitWorks Conductive Epoxy CW2400, Chemtronix). The gate path is also connected to a SMU. The source path (solid blue color, connected to the source electrodes of the GFETs) will be connected via an external switch (in the switch unit, Fig. 3c) with one of the two adjacent paths, depending on the measurement mode (CAFM or SMU). The blue double-line path corresponds to the CAFM connection meanwhile the light blue colored path corresponds to the SMU connection.

Once the I-PCB has been designed and printed and the chip glued over the gate path, contacts between the printed lines therein and the GFETs electrodes in the chip must be done. As previously introduced in Section II, ink-jet printing techniques were also used with this purpose, instead of wire bonding due to the advantages explained before. In our case, taking into account the size of the electrodes of the GFETs and the separation between GFETs, the 1pl cartridge was selected to reduce the drop size, in order to be able to print the connections without harming the GFETs. Also, the ink wettability (Siverjet DGP HR) and drop spacing were studied in order to obtain the correct deposition of the ink over the SiO_2 substrate and thus obtaining continuous conductive strips (Fig. 4c). We found that three prints are required in order to get a thicker and more conductive paths, making them less resistive than the graphene channels. However, depending on the thickness of the chip, an important aspect must first be solved. Since the chip is attached on the I-PCB, and abrupt step may appear at the edge of the chip, which could impede a good contact of the printed paths from the GFET to the I-PCB. If this was the case, as with the chip used in this work, to soften the abrupt step and have a better contact, we have proceeded as follows. The ICA material used to attach the chip to the I-PCB is also deposited over the edges of the chip, forming slope-shaped terminations (red circle in Fig. 4a, detail of the termination in Fig. 4b, yellow contour) over which the GFET paths (Fig. 4b, green contour) are printed towards the I-PCB paths (Fig. 4b, grey areas) allowing a better contact. Also, it will act as an additional mechanical fixation of the chip to the I-PCB.

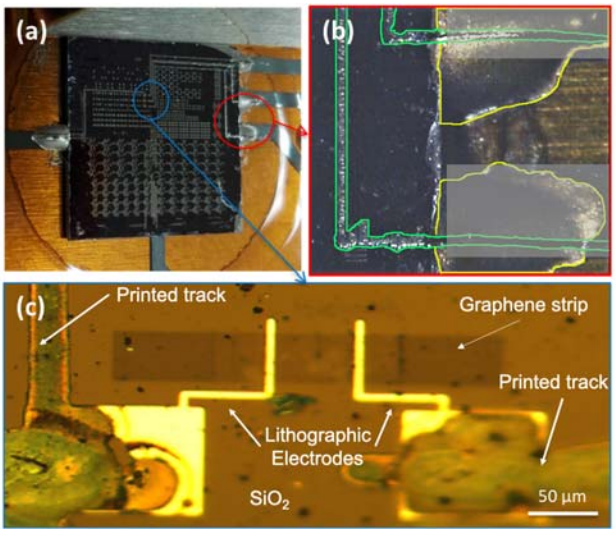

Fig. 4. (a) Chip with the GFETs positioned over the I-PCB using the ICA material (b) Detail of the slope-terminated interconnection between the chip and the connection circuit using the ICA. The green contour shows the printed paths from the DUT, the yellow contour the ICA slope termination and the grey areas correspond to the end of the printed tracks on the I-PCB over the Kapton that are covered by the slope termination. (c) Detail of a GFET contacted using the inkjet printing technique. The gold colored structures correspond to the metallic electrodes fabricated by standard lithographic techniques.

IV. Stress And Characterization of GFETs

To show the potentiality of the proposed system, as an example, the electrical properties of one of the GFETs in the chip, at device level and at the nanoscale, before and after device-level electrical stress, have been measured (Fig. 5). First, the electrical characteristics (V_G=0V) were measured before any electrical stress, using both the SPA and the CAFM

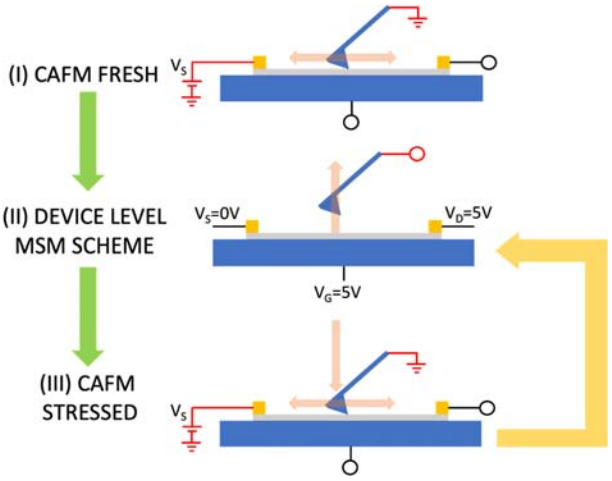

Fig. 5. Workflow of the measurement process. First, in (I) the fresh device channel is characterized at the nanoscale. Then, in (II), the tip is lifted, and an electrical stress is applied. Finally, in (III), the tip is lowered to the same position and the channel is again characterized at the nanoscale. (II) and (III) can be repeated as many times as needed. Red connections represent the connections to the CAFM, meanwhile the black ones represent connections to the SPA. A connection ended in a circle means that it is disconnected.

(Fig. 5.I and II). To stress the device, a two cycle MSM scheme has been followed, applying 5V DC at the Drain and Gate terminals, while the Source electrode was grounded, during 2h (first stress cycle) and 6h (second stress cycle), being 8h the total accumulated stress time (Fig. 5.II). After each stress cycle, morphology and local conductivity measurements were carried out (Fig. 5.III). An Agilent 5500 AFM was used, which was connected to a Resiscope Module (CSI Instruments), to measure currents in a higher dynamic range (from pA to mA) compared to standard CAFMs. The used tip was a bulk Pt tip from Rocky Mountain Nanotechnology. To obtain a clear image of the graphene layer morphological properties, the friction image was registered instead of the topography, as the contrast in the latter is very low due to the inherent low thickness of the graphene layer. Current maps were measured in contact mode, while the tip scans the surface. While scanning, using the I-PCB described in Section III, a voltage of 1V was applied at the Source terminal by the CAFM and the grounded Pt tip was acting as a Drain electrode, obtaining the nanoscale measurement of the lateral current flowing between the source terminal and the tip. This voltage was selected sufficiently low to obtain a measurable current but without provoking any electrical stress on the graphene layer.

Note that, in our set-up, the sample must not be moved from the AFM holder to the chuck of a wafer probe station, as needed if two separate set-ups were used. This offers several advantages. First, after a nanoscale measurement, the tip was lifted (but not moved in the x-y direction), so that, in the subsequent nanoscale test, the same area could be evaluated (this is not possible when two separate setups are used). Second, the time needed to change from "CAFM mode" to "SPA mode" (and vice versa) is mostly determined by the switching time of the used switch. When compared to the traditional method (i.e. when separated setups are used), this time is strongly reduced, since, in the latter case, the sample has to be physically moved from the CAFM holder to the wafer probe station, which certainly takes much longer. Finally, lateral conductivity measurements on fully developed devices are allowed. To the best of the authors knowledge, such kind of compact system with enhanced performance has not been yet reported.

A. Device properties before the stress.

The friction and current images of a region close to the source of the GFET, taken on the fresh device (i.e., before electrical stress), are shown in Figs. 6a/b. The friction image (Fig. 6a) shows grain boundaries and holes, which could have been created during the Chemical Vapor Deposition (CVD) growth [50] and/or graphene transfer process [51]. Similar features are mirrored in the current image, which show the lateral current between the tip and the Source (Fig. 6b). The holes, observed as areas with darker color in the friction image, are also measured in the current image with currents corresponding to the noise level of the setup. These areas might be related to regions without graphene and, therefore, to areas where the CAFM tip is contacting directly the SiO_2 substrate. Grain boundaries are detected in the friction image as lines that surround closed cells (the graphene single crystals) formed during the CVD synthesis process [52]. Again, in the current image, we can observe these Grain Boundaries. Their current is lower than that measured on graphene grains, but higher than that measured on holes (SiO_2). Figure 7 (blue curve) shows the I_D-V_D curve measured with the SPA, which presents a linear behavior. The inset shows a typical transfer characteristic of the

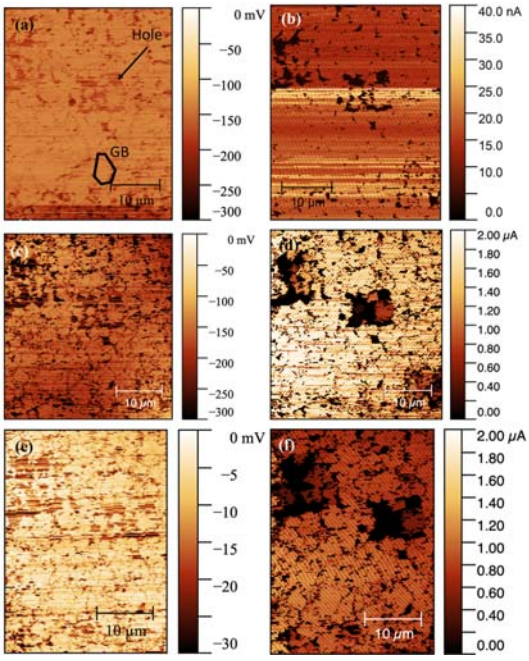

Fig. 6. Friction (a, c and e) and corresponding current images (b, d and f) of a zone near de source electrode of a GFET. (a) and (b) correspond to the fresh GFET, meanwhile (c) and (d) is the same zone after an 2h electrical stress. (e) and (f) show the same area after an 8h electrical stress. In (a) a hole and a grain boundary of the graphene layer have been highlighted.

fresh GFET. Its Dirac Point is shifted to around 37V, indicating a p-type doping due to the exposure of the channel to air [53]. The friction/current images in Figs. 6 a/b and the blue curve in Fig. 7 will be considered as the references, to whom those measured after the stress will be compared in the next section.

B. Device properties after the stress

Figure 7 also shows the I_D-V_D curves obtained on the GFET for the different stress times, together with the corresponding calculated resistances (from Ohm's law). As it can be seen, the changes in the device resistance are small, at least in this device. However, surprisingly, the highest resistance corresponds to the fresh device. This observation could be related to an additional sintering of the Ag ink or ICA epoxy during the stress due to Joule heating [54], which could be incomplete. This effect would hidden the real impact of the first-cycle stress on the absolute values of the current. Therefore, in this case, a comparison of the current absolute values before and after the first stress cycle is not meaningful at this moment. Then, sintering of the conductive ink and epoxy of the I-PCB must be studied in more detail before any measurement, to avoid this effect on the electrical data. However, after this additional sintering, smaller currents are observed when the stress time is increased from 2 to 8h (orange and green curves in Fig. 7), as expected.

Regarding the nanoscale graphene properties, Figure 6c and 6d show the friction and current images, respectively, after 2h of accumulated stress time, of the same region next to the Source. In the same way, Figures 6e and 6f show the friction and currents images after 8 hours of accumulated stress time of the same region. In the friction images one can see that, as the accumulated stress time increases, the inhomogeneities of the graphene channel also increase, which can be related to defects induced on the graphene layer during the electrical stress. The current images taken after the electrical stress, which correspond to the lateral current through the channel between the CAFM tip and the source, show that the stress has also affected the graphene electrical conduction. Those regions with lower conduction (grain boundaries and holes) have become larger. Therefore, the degradation leads to a less conductive graphene. Note, however, that the background current after the stress (Fig. 6d and 6f) is larger than in the fresh device (Fig. 6b), in agreement with device-level data, which, as previously mentioned, is an effect of the extra-curing of the silver ink and/or the ICA epoxy. However, when we compare the background current between images Fig. 6d and 6f (that is, after curing has been completed and changes can only be attributed to the electrical stress), after the 8h stress (Fig. 6f), current is lower than after the 2h stress cycle (Fig. 6d). This result is also in agreement with Fig. 7.

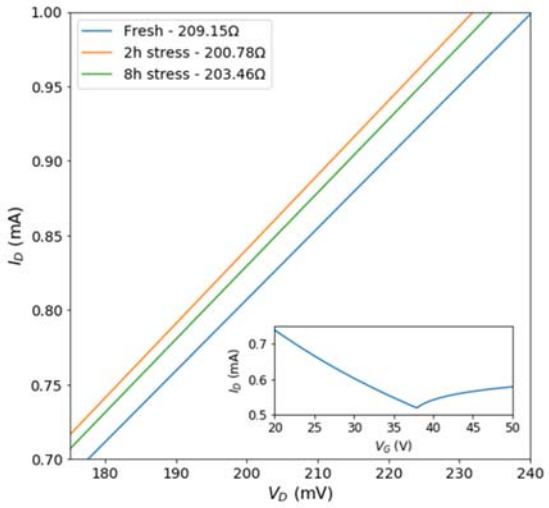

Fig. 7. I_D-V_D curves (V_G=0V) obtained in the GFET before and after HCI stress, for two different stress times. The measured resistivities are indicated in the label. The inset corresponds to a typical I_D-V_G curve of the fresh GFET.

These results, therefore, demonstrate that the stress induces a clear damage of the graphene layer at the nanoscale, which is observed in the GFET conduction at device level, leading to a less conductive device.

The case study described above demonstrates the potentiality of the proposed smart measurement system. However, other AFM-based techniques could be easily included in the system, instead of the CAFM, to evaluate other properties of fully processed devices at the nanoscale and their impact at device level. For example, a Kelvin Probe Force Microscope (KPFM) could measure the contact potential of the analyzed surface (which is related to the charged trapped in the device); or an Electrostatic Force Microscope (EFM), Magnetic Force Microscope (MFM), Scanning Capacitance Microscope (SCM) or Scanning Spreading Resistance Microscope (SSRM) could be used to determine the electrostatic, magnetic or doping profile, respectively. As for the instruments for the device level characterization, besides the SPA, other instruments as a C-V meter or a pulse generator could also be used instead. Then, the capabilities of the system can be easily extended.

VI. Conclusion

In this work, a smart flexible experimental set-up has been presented to combine nanoscale tests with standard electrical measurements at device level, on fully processed devices. The integration of the required equipment (SPA and CAFM in the described example) into a single system has been facilitated by the design of a custom-made inkjet-printed circuit board (I-PCB), that, when attached to the sample holder, allows the alternate or simultaneous connection of the device terminals to the required measurement instrumentation. The proposed system has demonstrated a large flexibility, making possible different test configurations, a fast switching between them and featuring an enlarged testing capability (i.e. nanoscale lateral conductivity measurements and characterization of the same area after a device-level test), at a lower cost. The capabilities of the proposed strategy have been demonstrated through smart reliability tests on back gated GFETs, which combine standard

MSM tests at device level with nanoscale lateral conductivity measurements on the same area. The results support the usefulness of proposed strategy and paves the way to new type of tests that, by unmasking hidden effects at device level, can provide a global view of the mechanisms acting in the device.

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