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SPICE simulation of the time-dependent clustering model for dielectric breakdown

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ABSTRACT

In this letter, a method for dealing with the time-dependent dielectric breakdown (TDDB) of oxide layers in MOS and MIM structures in the framework of SPICE simulations is reported. In particular, we focus the attention on the clustering model (Burr's XII distribution) for dielectric breakdown which can be considered an extension of the well known Weibull model. The oxide time-to-breakdown for both models is calculated using the inversion method for the cumulative distribution function. For the sake of completeness, the proposed approach includes uncorrelated variability both in the initial and final resistance states. For illustrative purposes, it is also shown how voltage acceleration, progressive breakdown or any other correlation factor can be introduced in the simulation parameters. As an application example, the proposed method is used to simulate the simplest case of a gate-to-drain dielectric breakdown of a NMOS-based inverter circuit.

1. Introduction

Because of the stochastic nature of the dielectric breakdown (BD) phenomenon in metal–oxide–semiconductor (MOS) and metal–insulator-metal (MIM) devices, its statistical features need to be addressed in terms of probability distributions. The most widely used distribution representing the time-to-BD statistics for constant or ramped voltage/current stress is the Weibull distribution [1]. This is a very flexible distribution able to capture different failure rate regimes, the most relevant one in the context of oxide reliability being the wearout phase (increasing failure rate). In previous studies, Monte Carlo simulations were used to investigate compound Weibull distributions [2] as well as the deviations caused by the oxide thickness variation and series resistance effect [3]. However, in recent years, oxide failure data have been shown to follow in many cases the so-called time-dependent clustering (TDC) model, from which the Weibull distribution can be derived as one of its limits [4]. Weibull and TDC coincide at the lowest percentiles but they notoriously differ at the highest ones. Importantly, TDC not only applies to failure data but also to the set and reset voltages of memristive devices based on the resistive switching (RS) mechanism [5,6]. TDC is a member of the Burr's family of distributions (Burr XII) and it can be regarded as a superposition of Weibull distributions with different scale factors [7]. This distribution of scale factors can arise for instance from a nonuniform gate oxide thickness from device to device which reflects in a wider spread of the BD times. In the case of RS devices, the distribution of scale factors can be attributed to the different current capacities of the generated filamentary structures. In any case, TDC involves some kind of additional variability in the analyzed data (detectable or undetectable) other than the weakest link character of dielectric BD. Monte Carlo simulations were also used to investigate TDC in the context of Bayesian inference [8] and non-uniform BD [7,9,10]. In this work, TDC is implemented in the LTspice XVII circuit simulator from Analog Devices [11] with the aim of simulating the oxide failure event occurring during a constant voltage stress. This is the typical experiment considered for qualifying a given MOS or MIM technology and is often referred to as Time-Dependent Dielectric Breakdown (TDDB). The proposed methodology can be adapted to more complex situations in which device area, stress voltage and temperature acceleration or correlation effects across model parameters and/or in between the initial and final resistance states of the device need to be considered. In the general case, to accomplish these objectives one can make use of feedback signals (current or voltage) acting on the behavioral electric components provided by the simulator or by adding new elements to the basic circuit. Here, we will concentrate on the simplest case, *i.e.* when the applied voltage directly drops across the device under test but series resistance effects can be easily included in the simulations. Once the simulation ends, measurement directives allow extracting the target information for further analysis or just for the generation of

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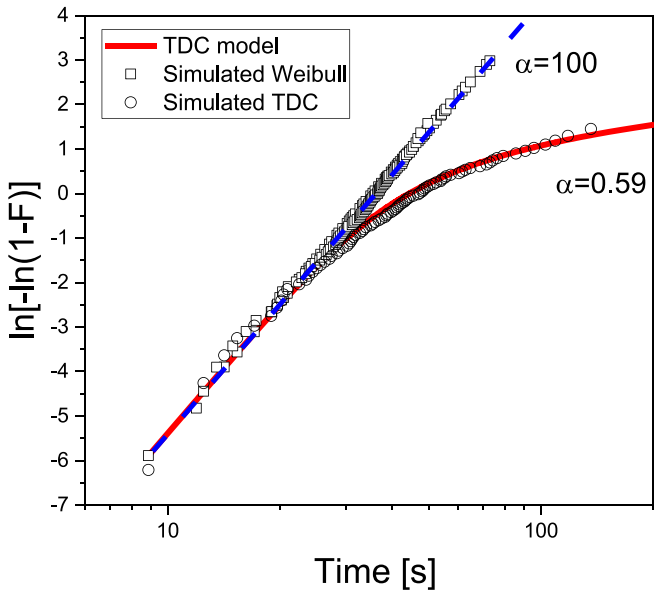


Fig. 1. Simulated data using the LTspice model (symbols) and calculated curves (lines) using Eqs. (1) and (4). The blue dashed line corresponds to the Weibull model. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

statistical reports. The method is extended to the case of progressive breakdown of the oxide layer. A simple example consisting in a biased MOS transistor with a gate-to-drain dielectric BD working as an inverter is used to illustrate how the proposed approach operates in a circuit environment.

2. Theoretical considerations

According to the TDC model, the cumulative distribution function for the BD events reads:

$$F_C(t) = 1 - \left[1 + \frac{1}{\alpha}\left(\frac{t}{\tau}\right)^{\beta}\right]^{-\alpha} \tag{1}$$

where α is the clustering factor, β the shape factor, and τ the scale factor (characteristic time). τ corresponds to the 63rd percentile value of the failure time. Following [8], expression (1) can be rewritten as:

$$F(t) = 1 - exp\left\{-\alpha ln\left[1 + \frac{1}{\alpha}\left(\frac{t}{\tau}\right)^{\beta}\right]\right\} \tag{2}$$

so that considering a series expansion results:

$$F(t) = 1 - exp\left\{-\alpha\left[\frac{1}{\alpha}\left(\frac{t}{\tau}\right)^{\beta} - \frac{1}{2}\left(\frac{1}{\alpha}\left(\frac{t}{\tau}\right)^{\beta}\right)^{2} + \frac{1}{3}\left(\frac{1}{\alpha}\left(\frac{t}{\tau}\right)^{\beta}\right)^{3} - \cdots\right]\right\} \tag{3}$$

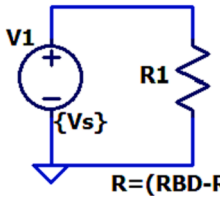
For $\alpha \to \infty$, the Weibull distribution is obtained:

$$F_W(t) = 1 - exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right] \tag{4}$$

It can be demonstrated that expression (4) coincides with expresion (1) at the lowest percentiles. In Fig. 1, the corresponding Weibit functions W calculated as $W = \ln[-\ln(1-F)]$ are plotted. In order to generate BD times consistent with Eq. (1) and therefore with Eq. (4) in the appropriate limit, Eq. (1) is inverted for a uniform random number $u \sim$ Unif[0,1] so that the BD time reads:

$$t = \tau\left\{\alpha\left[u^{-\frac{1}{\alpha}} - 1\right]\right\}^{\frac{1}{\beta}} \tag{5}$$

```
.tran 0 200 0 1e-3
.step param run 1 200 1
.param R0=10Meg+gauss(1Meg) RBD=10K+gauss(1K)
.param a=0.592 b=4.258 t0=4.2E2 gam=3.61E-1
.param seed=1000 t=t0*exp(-gam*Vs) Vs=7
.param tbd=t*((a*(rand(run+seed)**(-1/a)-1))**(1/b))
```




```
.meas time_to_BD param tbd
.meas BD_current find I(R1) at 200s
.meas fresh_current find I(R1) at 0s
R=(RBD-R0)*(time>tbd)+R0
```

Fig. 2. Complete schematic in LTspice for the time-dependent clustering and Weibull models for dielectric breakdown. The complete explanation about the expressions and commands used in this script is provided in Section 3.

Notice that since u is uniformly distributed, 1-u is also uniformly distributed. As reported in [12], for the model parameters considered in this work, τ is a voltage-dependent parameter which in the framework of the E-model (voltage acceleration) [7,13] is expressed as:

$$\tau = \tau_0 exp[-\gamma(V - I \bullet R_S)] \tag{6}$$

where τ_0 and γ are constants, V the applied voltage, I the current flowing through the device and R_S a series resistance. Eq. (6) illustrates how the potential drop in a series resistance can be introduced in the characteristic failure time as a feedback or correction term. This kind of effect has been reported in [3].

It is also worth mentioning that alternative expressions for the voltage acceleration factor in Eq. (6) such as the V^n-model [14], $1/E$-model [7] or $E^{1/2}$-model [2] can be considered as well.

3. SPICE model and simulation results

Simulations were carried out using the LTspice XVII simulator. This is a free downloadable circuit solver with a powerful simulation engine. For the sake of simplicity, the clustering parameters reported in [12] for the first BD event in Al_2O_3/HfO_2-based devices are considered. This is not relevant in the context of this work since we are not focusing neither on a particular device nor technology. We are presenting a computational method for its use in a circuit simulator which can be easily adapted to the user's particular needs. Since we will not analyze here the case of multiple failure events, the potential drop in Eq. (6) caused by the current flowing through the device can in principle be neglected. The proposed circuit schematic is illustrated in Fig. 2. After the definition of the total simulation time (200 s) and maximum timestep (1 ms), the parameter *run* (from 1 to 200 in unity steps) determines the number of independent simulations to be generated. Then, parameters α (a), β (b), τ_0 (t0), and γ (gam) are specified. *seed* (1000) is a parameter used to alter the random number generator output. *tbd* computes the BD time using Eqs. (5) and (6) with uniform random numbers generated by the stepped parameter *run*. V_s (7 V) is the stress voltage. R specifies the device resistance before (R_0) and after (R_{BD}) the BD event. *time* > *tbd* is a logic expression whose value is 1 for *time* > *tbd* and 0 for *time* < *tbd*. For simplicity, pre- and post-BD resistance values with Gaussian variability were assumed here but notice that these componenst can be easily edited so as to represent the current flowing through the fresh device (tunneling, Schottky, Poole-Frenkel, etc.) and the BD current (soft or hard BD, quantum point contact: $R = h/(2e^2N)$, etc.). R abruptly changes as the simulation proceeds according to *tbd*. Finally post-processing directives (*.meas*) provide the required outcomes as a function of the simulation run. In this particular case, the BD time is stored in the variable called *time_to_BD*. The current flowing through the device at the

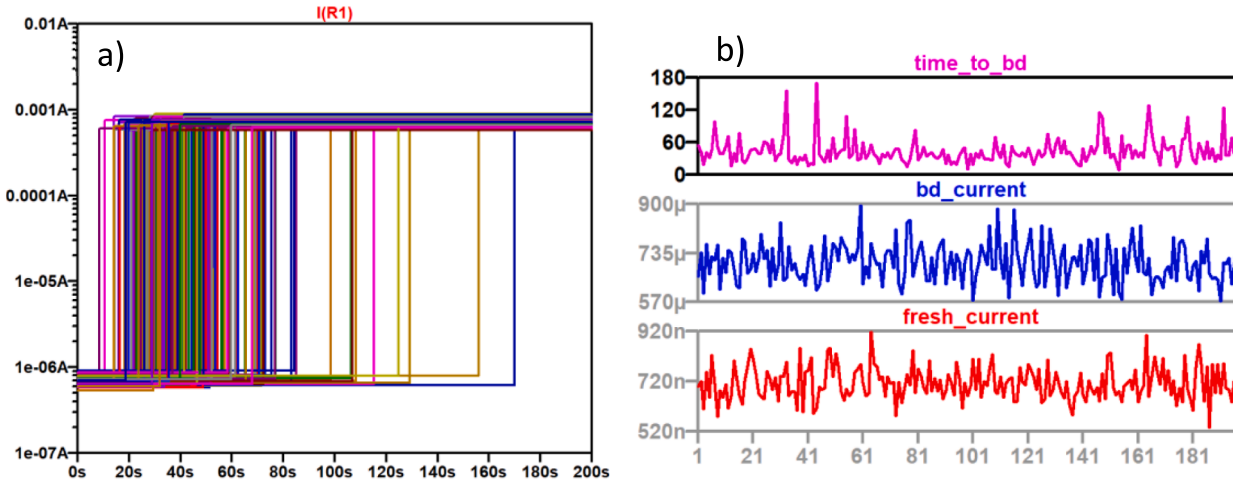


Fig. 3. A) ltspice simulations of the bd process using tdc. b) the time-to-bd, post-bd current and initial current as a function of the simulation number are also reported.

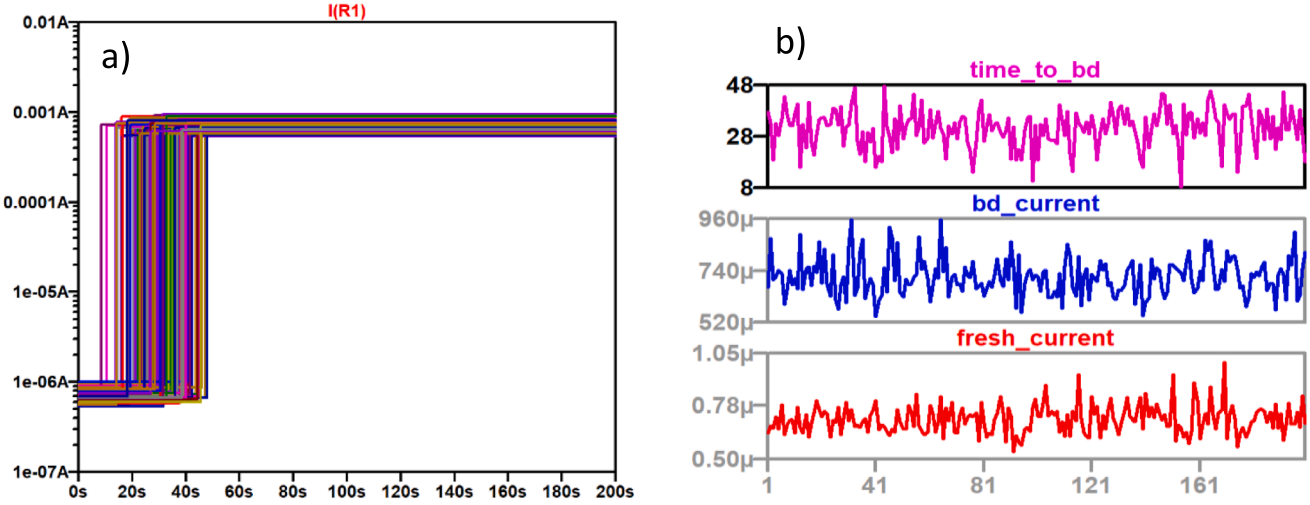


Fig. 4. A) ltspice simulations of the bd process using weibull. b) the time-to-bd, post-bd current and initial current as a function of the simulation number are also reported.

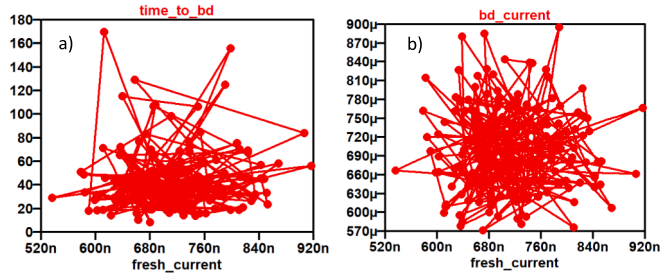


Fig. 5. Correlation plots among generated variables using TDC: a) time-to-BD as a function of the fresh current magnitude, b) post-BD current as a function of the fresh current magnitude. In this case, no specific correlations are expected.

onset (0 s) and end time (200 s) of the simulation are also recorded for further analysis. All these results can be viewed using the *Plot.step'ed. meas data* option (right click on the mouse) in the *VIEW → SPICE Error Log* tag. Notice that the BD times generated in this way can exceed the chosen simulation time window. In this case a redefinition of the total simulation time is required in order to avoid censoring. Average quantities or specific circuit values at a given time or condition can also be achieved using similar directives.

Fig. 1 shows the Weibit plot for the simulated BD times according to the TDC (see Fig. 3.a) and Weibull (see Fig. 4.b) approaches. Notice the close agreement between the simulated data and the theoretical curves calculated using Eqs. (1) and (4). As expected, both distributions coincide at the lowest percentiles and differ for the longest BD times. For completeness, Fig. 3.b and 4.b show the BD times and the initial and final current values as a function of the simulation run. Correlation plots are provided for the TDC model in Fig. 5. In the present case, currents are straightforwardly linked to the resistance values so that no correlations across calculated variables are expected. These plots are just for illustrating the kind of analysis that can be performed using the post-processing tools (*.meas* in Fig. 2) the simulator offers.

In addition, Fig. 6 illustrates how the proposed approach can deal with voltage acceleration (see Eq. (6)). As the applied voltage is reduced (V_s = 9, 7, and 3 V), longer BD times are statistically observed. This is equivalent to the addition of a series resistance in the circuit mesh. The acceleration law appears as a multiplicative factor in Eq. (6) and this affects both the average value and dispersion of the BD times.

The proposed approach also allows modeling progressive breakdown of the oxide layer. If a sigmoidal evolution [15] is assumed for the

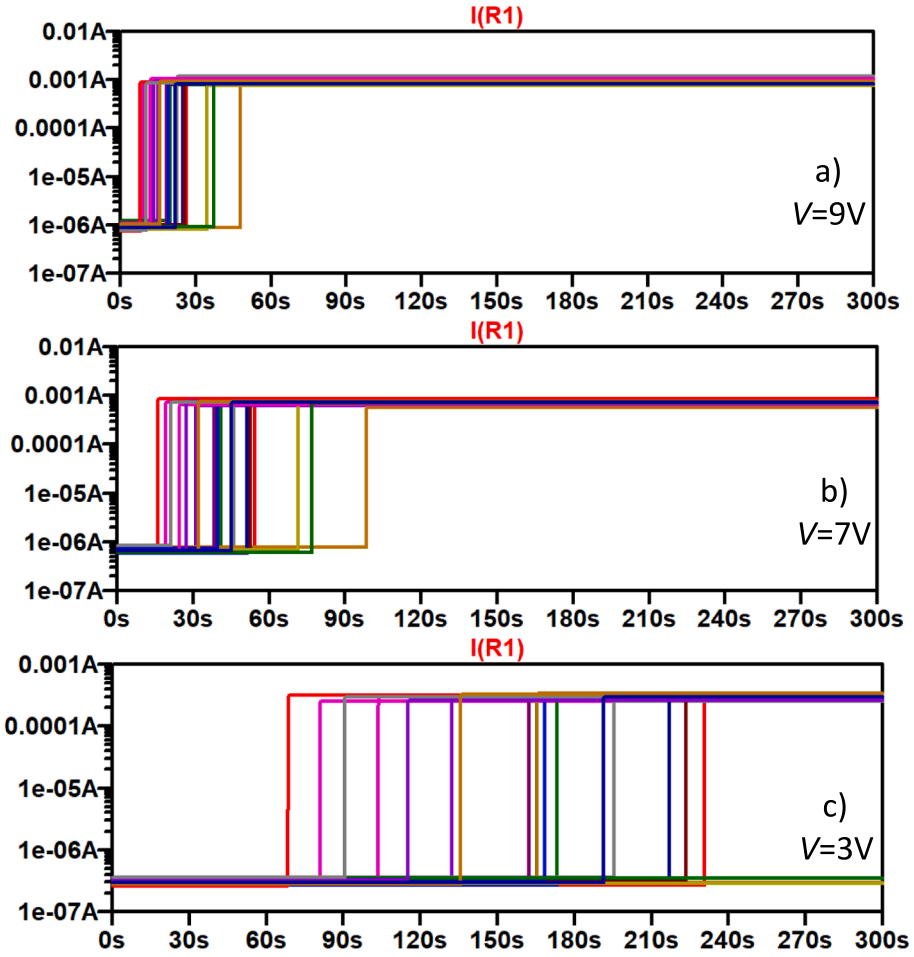


Fig. 6. Simulated curves using the TDC model with applied voltages: a) $V_s = 9$ V, b) 7 V, and c) 3 V.

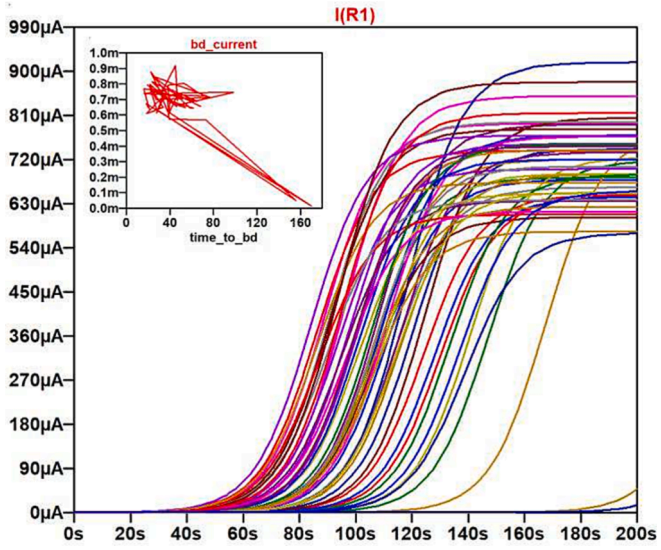


Fig. 7. Simulated curves using the TDC model and the progressive breakdown resistance (see Eq. (7)). The inset shows the final current magnitude as a function of the time to breakdown. Curves were obtained using the script shown in Fig. 2 with $k = 0.1$ s^{-1}.

breakdown resistance R in Fig. 2:

$$R = (RBD - R0)\{1 - exp[-k(time - tbd)]\}\cdot(time > tbd) + R0 \quad (7)$$

the results shown in Fig. 7 are obtained. k is a constant referred to as the degradation rate and depends on the applied voltage [16]. In this case, progressive breakdown and clustering/weibull models are combined in a single approach. As expected, the final state of the device depends on the total simulation time, the time-to-BD, and the initial and final distributions of resistances. As is clearly seen in Fig. 7's inset, the final breakdown current is no longer gaussian-distributed, *i.e.* degradation time matters.

4. Application to circuit simulations

The simulation of a failure event in SPICE or in any other simulator is important not only for the effects occurring in the device itself but also for the consequences this event can generate in the rest of a circuit [17,18,19,20,21]. As an application example, Fig. 8 shows the effects of a severe gate-to-drain dielectric BD occurring in transistors. Only the TDC case is investigated here for a simple NMOS inverter circuit. The same parameter values as in the previous sections were used just for illustrative purposes but they actually need to be tuned for the pulsed stress (dead times need to be considered). As shown in Fig. 8.a a pulsed signal (0–5 V) with duty cycle 0.5 is applied to the gate of the transistor (2 N7002). At ~ 35 s, according to the TDC distribution, the oxide breaks down establishing a direct path between gate and drain. A simple resistor (hard BD) was considered here but a power-law (soft BD) for the current–voltage characteristic can also be assumed [13,18,22]. From

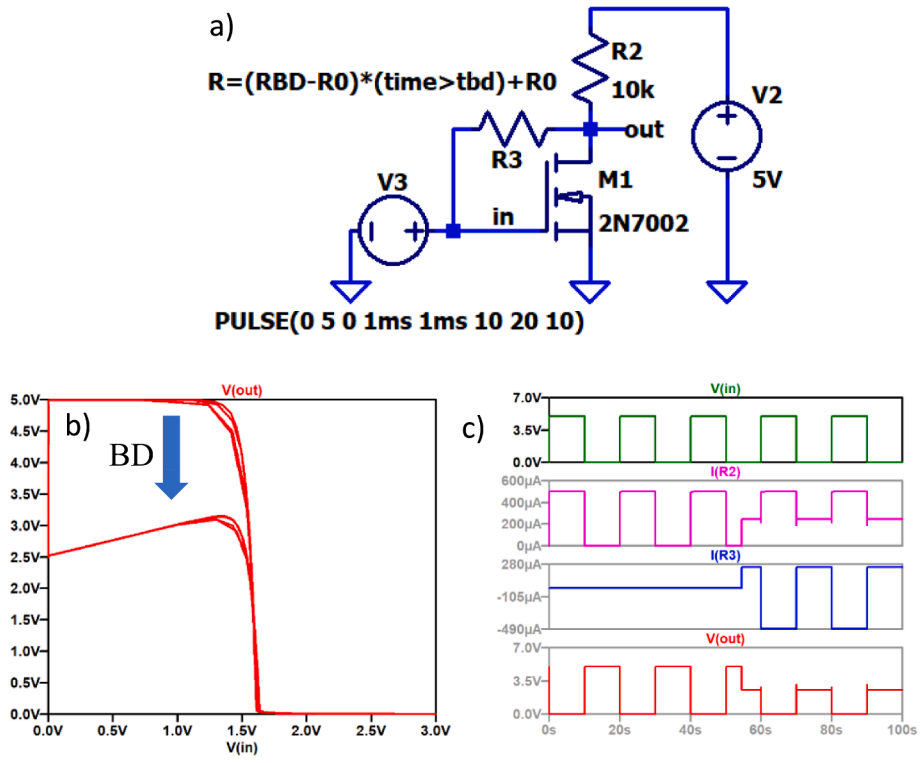


Fig. 8. A) application of the tdc model to a nmos inverter circuit. b) transfer curve for the circuit shown in a) before and after the bd event. c) input and output characteristics of the transistor as a function of time before and after the bd event ($tbd \sim 35$ s).

this point on, the circuit does no longer work as expected. Fig. 8.b shows the transfer function before and after the BD event. The channel current cannot be switched off and the gate current reaches positive and negative values as reported in [20]. The bottom panel in Fig. 8.c illustrates that, though the device still operates as an inverter, the output voltage excursion becomes limited. In [23], a similar problem was addressed in SPICE but considering the contribution of several independent voltage-controlled current sources in the gate-drain circuit. The authors analyzed the impact of a successive BD events on the performance of a ring oscillator. In this case, Monte Carlo simulations were carried out in combination with the Weibull distribution. Successive BDs in a CMOS inverter and their impact on the frequency drift of a ring oscillator were also investigated in [24] but again in the context of Weibull distribution. For the case of a gate-to-channel short, a model consisting in third order polynomial sources at the drain and source with a third current source in between drain and source with value proportional to the channel current was proposed in [25]. In none of the cases, the script used for generating the oxide BD data was provided.

5. Conclusions

A SPICE approach for simulating the breakdown time of the oxide layer in MOS and MIM structures was reported. We show how the clustering model for dielectric breakdown can be implemented using the inversion method for the cumulative distribution function. The Weibull distribution is included as a limiting case. Most of the paper is devoted to abrupt breakdown events, but it has also been shown how the equations can be adapted to the progressive breakdown case. A simple example (NMOS inverter with a gate-to-drain hard breakdown) showing how the proposed approach applies in a circuit environment was also presented.

CRediT authorship contribution statement

E. Salvador: Conceptualization, Formal analysis, Investigation, Supervision, Writing – original draft, Writing – review & editing. **R. Rodriguez:** Conceptualization, Funding acquisition, Investigation, Supervision, Writing – original draft, Writing – review & editing. **E. Miranda:** Conceptualization, Formal analysis, Investigation, Supervision, Writing – original draft, Writing – review & editing.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests: Enrique Miranda reports financial support was provided by EMPIR programme, project MEMQuD, code 20FUN06.

Data availability

Data will be made available on request.

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References

[1] Wu E. Facts and myths of dielectric breakdown processes—Part II: post-breakdown and variability. IEEE Trans Electron Devices 2019;66:4535.

[2] Chen F, Graas C, Shinosky M, Zhao K, Narasimha S, Liu X, et al. Breakdown data generation and in-die deconvolution methodology to address BEOL and MOL dielectric breakdown challenges. Mic Rel 2015;55:2727.
[3] Roy D, Bruyere S, Vincent E, Monsieur F. Series resistance and oxide thickness spread influence on weibull breakdown distribution: new experimental correction for reliability projection improvement. Mic Rel 2002;42:1497.
[4] Wu E, Li B, Stathis J. Modeling of time-dependent non-uniform dielectric breakdown using a clustering statistical approach. Appl Phys Lett 2013;103:152907.
[5] Raghavan N. Failure of weibull distribution to represent switching statistics in OxRAM. Mic Eng 2017;178:230.
[6] Sun H, Zhang M, Li Y, Long S, Liu Q, Lv H, et al. A cell-based clustering model for the reset statistics in RRAM. App Phys Lett 2017;110:123503.
[7] Shimizu T, Suzumura N, Ohgata K, Tsuchiya H, Aono H, Osagawara M. "A new aspect of time-dependent clustering model for non-uniform dielectric TDDB", 2016 IEEE International Reliability Physics Symposium (IRPS), Pasadena, CA, USA, 2016, pp. 3A-4-1-3A-4-10.
[8] Kunii K, Endo S, Yokogawa S. Bayesian infererence of a lifetime distribution parameter on the time-dependent dielectric breakdown with clustering defects. Jap J App Phys 2019;58. SHHG02.
[9] Wu E, Li B, Stathis J, Achanta R, Filippi R, McLaughlin P. "A time-dependent clustering model for non-uniform dielectric breakdown", 2013 IEEE International Electron Devices Meeting, Washington, DC, USA, 2013, pp. 15.3.1-15.3.4.
[10] Mei S, Raghavan N, Bosman M, Pey KL "Statistical basis and physical evidence for clustering model in FinFET degradation", 2017 IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 2017, pp. 3C-1.1-3C-1.6.
[11] https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html.
[12] Muñoz J, Gonzalez MB, Campabadal F, Suñé J, Miranda E. Application of the clustering model to time-correlated oxide breakdown events in multilevel antifuse memory cells. IEEE Elect Dev Lett 2020;41:1770.
[13] Li X, Qin J, Bernstein J. Compact modeling of MOSFET wearout mechanisms for circuit-reliability simulation. IEEE Trans Dev Mat Rel 2008;8:98.
[14] Wu EY, Nowak EJ, Vayshenker A, Lai WL, Harmon DL. CMOS scaling beyond the 100-nm node with silicon-dioxide-based gate dielectrics. IBM J Res Develop 2002;46:287.
[15] Miranda E, Jiménez D, Suñé J. Progressive breakdown dynamics and entropy production in ultrathin SiO2 gate oxides. Appl Phys Lett 2011;98:253504.
[16] Aguirre F, Rodriguez-Fernandez A, Pazos S, Suñé J, Miranda E, Palumbo F. Study on the connection between the set transient in RRAMs and the progressive breakdown of thin oxides. IEEE Trans Electron Dev 2019;66:3349.
[17] Rodriguez R, Stathis J, Linder B, Kowalczyk S, Chuang C, Joshi R, et al. The impact of gate-oxide breakdown on SRAM stability. IEEE Elect Dev Lett 2002;23:559.
[18] Rodriguez R, Stathis J, Linder B. A model for gate-oxide breakdown in CMOS inverters. IEEE Elect Dev Lett 2003;24:114.
[19] Kaczer B, Degraeve R, Roussel Ph, Groeseneken G. Gate oxide breakdown in FET devices and circuits: from nanoscale physics to system-level realiability. Mic Rel 2007;47:559.
[20] Nicollian P, Cakici R, Krishnan A, Reddy V, Seshadri A. Device characteristics and equivalent circuits for NMOS gate-to-drain soft and hard breakdown in polysilicon/SiON gate stacks. IEEE Trans Electron Dev 2011;58:1170–5.
[21] Miranda E, Kawanago T, Kakushima K, Suñé J, Iwai H. Analysis and simulation of the postbreakdown I-V characteristics of n-MOS transistors in the linear response regime. IEEE Elect Dev Lett 2013;34:798.
[22] Fang J, Sapatnekar S. Scalable methods for analyzing the circuit failure probability due to gate oxide breakdown. IEEE Trans Very Large Scale Int Sys 2012;20:1960.
[23] Panagopoulos G, Ho C, Kim S, Roy K. "Physics-based compact modeling of successive breakdown in ultrathin oxides. IEEE Trans Nano 2015;14:7.
[24] Saliva M, Cacho F, Huard V, Angot D, Federspiel X, Durand M, Parra M, Bravaix A, Anghel L. "New insights about oxide breakdown occurrence at circuit level," 2014 IEEE International Reliability Physics Symposium, Waikoloa, HI, USA, 2014, pp. 2D.5.1-2D.5.6.
[25] Chehade S, Chehab A, Kayssi A. "Modeling of gate oxide short defects in MOSFETS", 2009 4th International Design and Test Workshop (IDT), Riyadh, Saudi Arabia, 2009, pp. 1-4.