Noise-Induced Homeostasis in Memristor-Based Neuromorphic Systems

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***Abstract*— In this work, it is experimentally demonstrated that noise can be used to emulate the biological homeostatic neuron property in memristor-based neuromorphic systems. The addition of an external noise to the bias allows regulating the memristor performance when used as an artificial neuron, controlling the firing process through the modulation of the memristor threshold voltages. Experimental results have been correctly addressed using the Dynamic Memdiode Model (DMM) for memristors in the framework of SPICE simulation.**

***Index Terms*— Memristor, RRAM, resistive switching, stochastic resonance, homeostasis, spike neural networks, SPICE.**

I. Introduction

POST Von-Neuman computing architectures, such as neuromorphic systems, have attracted the attention of the scientific community in the last years because of their enormous possibilities in several application fields [1], [2]. Neuromorphic systems try to emulate the brain performance, forming the computation and memory units a single operational structure. The development of hardware implementations of these new architectures using emerging devices such as memristors offers beneficial features in terms of energy consumption and computational efficiency. In case of biological neurons, they receive, process and transfer information through the gap in between them called synapse. Since memristors are nonvolatile memory devices exhibiting nonlinearity, good scalability and programming capabilities, they are considered excellent candidates for the implementation of both artificial neurons and synapses in neuromorphic circuits [2], [3].

In Spike Neural Networks (SNN), excitatory and inhibitory neuron operations are fundamental processes of synaptic activities, and they mutually coordinate each other. However, neuron operation can lead to excessive excitatory or inhibitory processes [4], causing some neurons to continuously fire spikes (having a dominant role in the training process), while others cannot learn because of the low firing frequency [5]. However, biological neurons present a configurable performance capable of adapting to changing conditions maintaining the neural system homeostasis [6]. The homeostatic mechanism is necessary to balance neuron activities and reach more stable neural performances, resilient to different types of unstable neuron behavior [7], [8]. Then, the inclusion of homeostasis in artificial neural networks becomes mandatory for regulating the activity of neurons [9] and optimize learning [10].

Some previous works in the literature consider the homeostasis in memristor-based neuromorphic systems. In [5], the training of a SNN is enhanced through the flexible adjustment of the synaptic weight update frequency based on homeostasis. In [11], a memristive neural network circuit that can implement memory with emotional homeostasis is designed. In [12] and [13] homeostasis also plays a relevant role to avoid device variations in SNNs. Most of these proposals include homeostasis through software implementation. In a more realistic scenario, it would be convenient to include the homeostatic property in the memristor performance for self-adjusting the neuron activities and enhance the neuron ability of self-stabilizing.

Because of the non-linear properties of memristors, their performance can be improved through the exploitation of the so-called stochastic resonance (SR) phenomenon, which is the beneficial use of an external noise, in this case, to enhance memristor functionality (a detailed description of SR can be found in [14]). Some previous works have observed the increase of the memristor resistance ratio (R_{OFF}/R_{ON}) [15] and the improvement of the spike-time-dependent plasticity (STDP) learning protocol [16] through the addition of an external noise source.

In this work, we demonstrate that, by adding external noise to the device bias, the homeostasis property can be implemented in memristor-based SNNs. The impact of noise on the regulation of the spiking neuron operation, through the modulation of the memristor threshold voltages (set and reset

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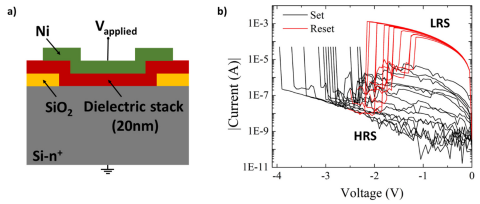

Fig. 1. a) Schematics of the unipolar memristors used in this work and b) typical $I-V$ characteristics after the electroforming of the conductive path.

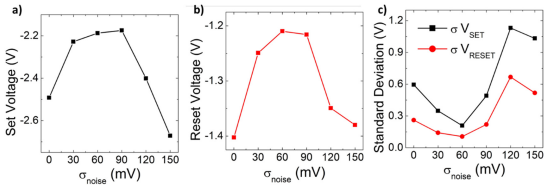

Fig. 2. a) Mean set and b) reset voltages and c) set (black) and reset (red) voltages standard deviation, versus noise σ.

voltages), is described. Experimental results were reproduced using the LTspice simulator and the dynamic memdiode model (DMM), which has demonstrated high versatility for different materials and input signals [17], [18], [19], [20].

II. Devices and Measurement Methodology

The devices used in this work were Ni/insulator/Si-n^+ metal-insulator-semiconductor (MIS) square structures with a 15×15 um^2 active area. These devices were fabricated on highly doped N-type (100) silicon wafers. The insulator layer was deposited via Atomic Layer Deposition (ALD) at 225 °C using as precursors trimethylaluminum and H_2O for Al_2O_3, and tetrakis (dimethylamido)-hafnium and H_2O for HfO_2. N_2 was used as carrier and purge gas. The Ni top electrode was deposited by magnetron sputtering and patterned by lift-off. The dielectric film of the characterized devices consisted of a stack of HfO_2 and Al_2O_3: 4 nm HfO_2 – 4 nm Al_2O_3 – 4 nm HfO_2 – 4 nm Al_2O_3 – 4 nm HfO_2, resulting in a 20 nm-thick dielectric layer. The device structure is presented in Fig. 1a. Further details regarding the fabrication process and device characterization can be found in [21]. Fig. 1b illustrates the unipolar non-volatile memristor behavior operating at negative voltages, showing the memristor high resistance state (HRS) and low resistance state (LRS).

The Semiconductor Parameter Analyzer (SPA) Agilent 4156C was used to carry out the electrical measurements. The experiments were programmed, launched and analyzed in MATLAB software. To trigger the electroforming process, a negative voltage sweep was applied, limiting the current to 1 μA to avoid the irreversible breakdown of the device. This electroforming occurs at around -11 V. In the experiments described in section III, after forming, 100 cycles of consecutive reset (switching from LRS to HRS) and set (from HRS to LRS) events are applied, through voltage ramps starting at 0V and ending when certain conditions are fulfilled. For the reset process, the ramp voltage is halted (reset voltage) when a current decrease of at least one order of magnitude is detected, with a 50mA compliance limit fixed. The set voltage was defined as the voltage at which the memristor current has increased until 50 μA. An external Gaussian noise was added point-by-point to the bias voltage; several noise standard deviations (σ) were considered, ranging from 0 mV to 150 mV. The set and reset voltages and their standard deviations have

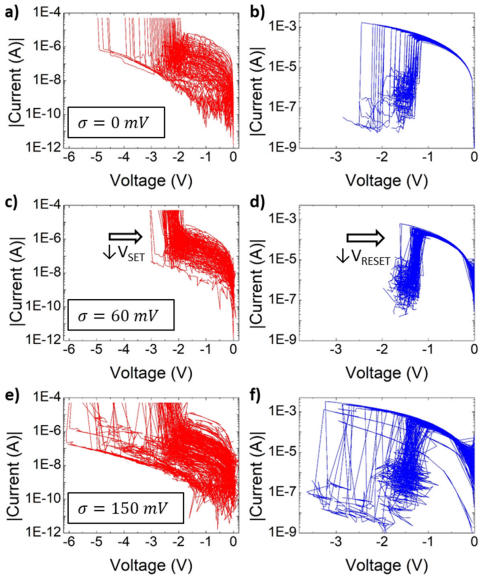

Fig. 3. $I-V$ curves from the 100 set-reset memristor cycles for set (in red, left column) and reset processes (in blue, right column) for three cases: no noise (a and b), noise addition with $\sigma = 60$mV (c and d) and $\sigma = 150$ mV (e and f).

been registered and analyzed. In section IV, after forming, staired constant voltages (i.e., a sequence of constant voltages of a certain duration, whose value was increased in steps in a given voltage range) were applied on different samples. The set transition modulation was studied by computing the time needed to switch the device. The experiments detailed in this work were repeated in other devices from the same wafer to ensure consistency and reproducibility of outcomes.

III. Noise Impact in the Set and Reset Transitions

In this section, the impact of an external noise in the set and reset voltages of a memristive device is evaluated. The mean set and reset voltages obtained for different noise amplitudes σ are shown in Figs. 2a and 2b, respectively; the standard deviation of these voltages is presented in Fig. 2c. The typical SR curve is observed, with a decrease (in absolute value) of the threshold voltages and a decrease of their σ, in a range of noise σ around 60 mV. The complete picture demonstrates that the threshold voltages of the memristor can be tuned through the action of an external noise source. Fig. 3 presents the set (in red, Figs. 3a, 3c and 3e) and reset processes (in blue, in Figs. 3b, 3d and 3f) for three distinct situations: Figs. 3a and 3b for the experiments without noise, Figs. 3c and 3d for experiments with $\sigma_{noise} = 60mV$, and Figs. 3e and 3f for experiments with $\sigma_{noise} = 150mV$. It is clear that for $\sigma_{noise} = 60mV$ both set and reset transitions occur at lower voltage values than those corresponding to the absence of noise and with $\sigma_{noise} = 150mV$. In addition, the transitions for $\sigma_{noise} = 60mV$ are less spread, meaning that the set and reset events are modulated to lower and less variable voltage values.

IV. Noise Impact on Memristor Spike Time

In this section, noise-induced homeostasis in memristors is studied by observing the effect of noise on the spike time of a single memristor operating as a neuron. We focus on the simplest memristor neuron, where the spike time is defined as the time to trigger a memristor set event. The results can be extrapolated to other memristor neuron implementations

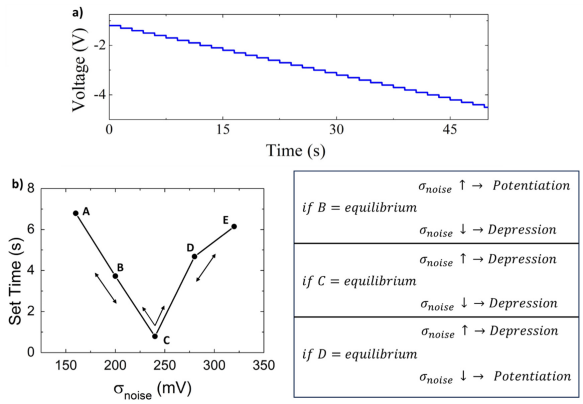

Fig. 4. a) Time evolution of the staired constant voltage. b) Stochastic resonance curve in the set event time against the noise σ. Schematic of homeostatic regulation possibilities for different equilibrium situations.

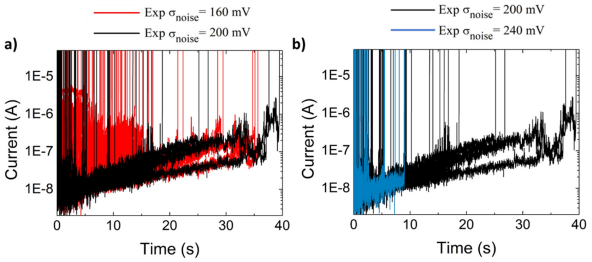

Fig. 5. a) Experimental current versus time evolution during a staired constant voltage for $\sigma_{noise} = 160mV$ (black curves) and $\sigma_{noise} = 200mV$ (red curves). b) for $\sigma_{noise} = 200mV$ (black curves) and $\sigma_{noise} = 240mV$ (blue curves).

as for example, the integer-and-fire memristor neuron [7]. On the one hand, if noise reduces the time required for a set event (spike), the system exhibits increased excitability, termed potentiation regime. On the other hand, when noise prolongs set event times, the system experiences decreased excitability, known as depression regime. Considering the memristor in HRS, the memristor spike time is defined in more detail as the cumulative time needed to produce a set event when a staired constant voltage is applied (Fig. 4a). The staired voltage started at -1.2 V adding -100 mV every 1.5 seconds; the sweep is stopped once the set event occurs (i.e., when the current abruptly increases and reaches 50 μA). To ensure the memristor was at the HRS, the reset process was induced with voltage ramps as those described in section III. The staired constant voltage is applied to accelerate the set transition and to ensure that the device switches to the LRS in an acceptable time window. The voltage increase is slower than when a voltage ramp (as those in section III) is applied, so that, as observed in other works [16], for this new biasing, the beneficial role of noise is observed for different noise σ. This procedure (reset with a voltage ramp and set with a staired constant voltage) was repeated 100 times (i.e., cycles) with different σ_{noise} values in the same device.

In Fig. 4b, we observe a stochastic resonance curve depicting the evolution of mean set time versus σ_{noise}. Different points are highlighted. Assuming brain as a noisy system, B point can be interpreted as an equilibrium point. When σ_{noise} is increased, shorter set times are obtained leading to a potentiation regime, meanwhile a decrease in σ_{noise} results in a depression regime. The dynamics are reversed if D is interpreted as the equilibrium point. The impact of noise on the memristor spike time has been analyzed in detail

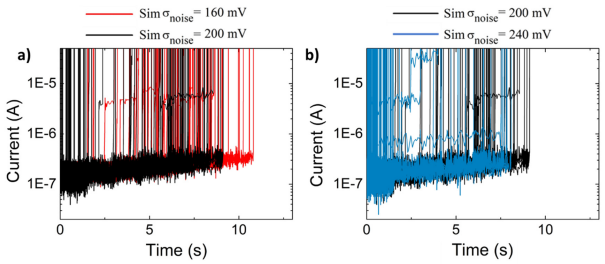

Fig. 6. a) Simulated current versus time evolution during a staired constant voltage for $\sigma_{noise} = 160mV$ (black curves) and $\sigma_{noise} = 200mV$ (red curves). b) for $\sigma_{noise} = 200mV$ (black curves) and $\sigma_{noise} = 240mV$ (blue curves).

for three different noise σ: 160mV, 200 mV and 240 mV (points A, B, and C respectively in Fig. 4b). Fig. 5a shows the experimental memristor current as a function of time for $\sigma_{noise} = 160mV$ (red curves) and $\sigma_{noise} = 200mV$ (black curves). The abrupt increase in current means the occurrence of the memristor spike. A depression regime is observed, being the spike time increased by reducing σ_{noise}. Oppositely, Fig 5.b shows the memristor current as a function of time for the experiments with $\sigma_{noise} = 200mV$ (black curves) and with $\sigma_{noise} = 240mV$ (blue curves). Now, a potentiation regime emerges, demonstrating reduced spike time with increased noise σ. Thus, modifying the σ_{noise}, memristor spike times are modulated, thereby regulating the neuron speed [7] to maintain homeostasis.

The previous experimental results were compared with LTspice simulations carried out with the DMM memristor model. The DMM relies on two key equations, one governing the current-voltage characteristic and the other dictating the memristor memory state. A comprehensive description of this model and its practical implementation can be found in [17] and [18]. Cycle-to-cycle variability was included in the model parameters related to the HRS current and set voltage, following the method presented in [20]. Calibration of the model parameters was performed by reproducing the experimental median I-V behavior using standard voltage sweeps. After calibration, the same input signal was reproduced including Gaussian noise in the applied signal. LTSPICE simulated results in Fig. 6 are qualitatively the same as the experimental results of Fig. 5 when, also observing the spike time modulation in both depression (Figs. 5a and 6a) and potentiation (Figs. 5b and 6b) regimes. This result demonstrates the suitability of the DMM for simulating the noise impact on the spike time.

V. Conclusion

This work presents a first experimental demonstration of noise-induced modulation of the spike time in memristor-based SNNs. Stochastic resonance has been observed in both memristor set and reset voltages and their respective standard deviations. Noise inclusion can modulate the memristor spike times, thereby facilitating both potentiation and depression of neural activity, crucial for maintaining system homeostasis. Experimental results have been correctly reproduced in LTspice using the DMM. The results highlight the pivotal role of noise in SNNs, thereby paving the way for further research of next-generation computing systems.

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