Statistical Reproducibility of Selective Area Grown InAs Nanowire Devices

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Abstract: New approaches such as selective area growth (SAG), where crystal growth is lithographically controlled, allow the integration of bottom-up grown semiconductor nanomaterials in large-scale classical and quantum nanoelectronics. This calls for assessment and optimization of the reproducibility between individual components. We quantify the structural and electronic statistical reproducibility within large arrays of nominally identical selective area growth InAs nanowires. The distribution of structural parameters is acquired through comprehensive atomic force microscopy studies and transmission electron microscopy. These are compared to the statistical distributions of the cryogenic electrical properties of 256 individual SAG nanowire field effect transistors addressed using cryogenic multiplexer circuits. Correlating measurements between successive thermal cycles allows distinguishing between the contributions of surface impurity scattering and fixed structural properties to device reproducibility. The results confirm the potential of SAG nanomaterials, and the methodologies for quantifying statistical metrics are essential for further optimization of reproducibility.

Keywords: nanowires, selective area growth, semiconductors, multiplexers, reproducibility

The characteristics of nanoscale electrical devices can be significantly influenced by rearrangements of only a few atoms in the vicinity of the active transport channel, especially at low temperatures.[1,2] Material purity and device reproducibility are thus key concerns in the development of increasingly complex and powerful electrical quantum circuits operating at ultra-low temperatures.[3] While bottom-up semiconductor nanowires have been an important platform for mesoscopic quantum electronics due to the high control of crystal properties,[4] intrinsic quantum confinement,[5] and flexible epitaxial integration of dissimilar materials,[6,7] the traditional out-of-plane geometry is incompatible with standard semiconductor processing and has prevented up-scaling of nanowire circuits. The method of SAG[8–11] potentially removes this roadblock by allowing large-scale lithographic control of planar nanowire growth. Already, key device concepts based on SAG nanowires have been realized, such as field effect transistors (FETs),[12,13] nanowire Hall bars,[14,15] quantum interferometers,[16,17] hybrid superconducting devices,[16,18,19] and quantum dots.[20] So far, however, the focus has been on proof-of-principle experiments based on a few devices. We here take the next step towards up-scaling by quantifying the statistical reproducibility of SAG devices operated at the deep cryogenic conditions relevant for quantum circuitry.

Statistical assessment of reproducibility requires repeated characterization of the electrical parameters for large ensembles of devices. To bypass the device-count limitation usually imposed on cryogenic nanowire experiments, we employ cryogenic multiplexers (MUX) for semi-automated characterization of large numbers of devices in a single cool-down.[21–23] The variability between nominally identical devices is influenced by both structural variations related to fabrication tolerances and local fluctuations in growth conditions and from the random electrostatic potential from charged impurities or adsorbates in the vicinity of the device. We study these relative contributions by statistically correlating measurements of successive temperature cycles between the cryogenic regime and room temperature, where impurity configurations are randomized.[24] These distributions are compared to the fixed structural variability that is quantified through systematic atomic force microscopy (AFM) analysis of 180 nominally identical nanowires.

The aim of this work is thus to quantify the statistical variations in the specific SAG InAs nanowires grown here, which serves as a reference for ongoing efforts to optimize SAG as a scalable platform for quantum electronics. Secondly, our work demonstrates the methods for acquiring the required statistical metrics in SAG circuits. We compare the results to alternative material candidates for cryogenic electronics, such as AlGaAs/GaAs 2D heterostructures and cryogenic CMOS.

SAG nanowires were grown by molecular beam epitaxy (MBE) on undoped (3 1 1)A GaAs substrates, which are electrically insulating at low temperatures. A growth mask (10 nm of SiO_2) was patterned using electron beam lithography and dry etching to expose the GaAs substrate in large arrays of nominally identical $0.15 \times 10\,\mu$m

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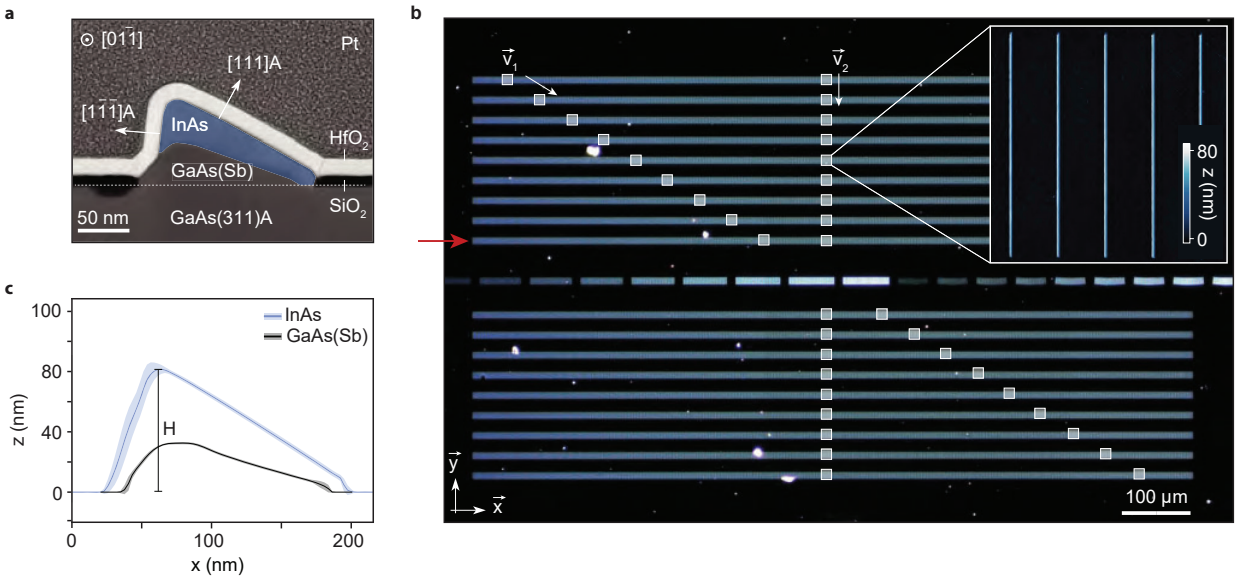

FIG. 1. **a** Cross-section transmission electron micrograph of a SAG InAs nanowire (blue). The asymmetric shape is a consequence of the (3 1 1) substrate symmetry. **b** Optical dark-field microscope image of a nanowire array consisting of two blocks of 9 rows, each holding 512 individual, nominally identical SAG nanowires with a length of 10 μm and cross-sections as in panel a. 180 nanowires were structurally characterized by AFM acquired at the positions of the white squares. An example of an AFM image is shown in the inset. The red arrow indicates the row of nanowires used in the transport measurements. **c** Example of cross-section AFM profile averaged over 1μm of an InAs nanowire and the GaAs(Sb) buffer. The shaded regions correspond to the standard deviation. The maximum height, H, is used to quantify the morphological variations in the nanowire array.

rectangular openings aligned along the [0$\bar{1}$1] direction. The arrays contain two blocks. Each block consists of 9 rows spaced 35 μm apart, and holds 512 nanowires with a pitch of 2 μm. The prepared substrates were introduced into the MBE chamber, and a GaAs(Sb) buffer layer was grown to improve the GaAs substrate surface for the subsequent growth of InAs which serves as the active conducting channel in the transport experiments.[12,23] Further details of substrate preparation and growth parameters are included in Supplementary Section I. Figure 1**a** shows a high-angle annular dark field scanning transmission electron microscope (HAADF STEM) micrograph of a SAG nanowire cross-section. The nanowire has an asymmetric profile imposed by the (3 1 1) symmetry of the substrate. Figure 1**b** shows a dark-field optical microscope image of an array consisting of 8192 nanowires. Three such arrays from the same growth were used in this study for the TEM, AFM, and transport characterization.

We first consider the contributions to structural variations between neighboring nanowires and across the array. Although all nanowires are defined to be nominally identical, different effects contribute to variations at different length scales. While variations that occur at length scales significantly below the typical device length ($L_D \sim 1\,\mu$m, see below) alter the average electrical parameters, the variations at longer scales reduce reproducibility between neighboring devices or lead to long-range modulations across the array. For example, on the few-nanometre scale, dislocations and stacking faults occur in the crystal due to the lattice mismatch at the GaAs/InAs interface. This is confirmed by cross-sectional TEM performed on four representative nanowires (see Supplementary Section III). Elastic relaxation is observed around the rounded top corner and the shorter (1 $\bar{1}$ $\bar{1}$)A nanowire facet, while misfit dislocations occur with an average distance of $\sim$ 9 nm along the longer (1 1 1)A InAs/GaAs(Sb) interface. In addition, based on a limited number of HR-TEM micrographs, a typical number of stacking faults between 1 and 4 are observed in each cross-section. As discussed previously,[12] the strain in the system and the elevated temperature during growth promote inhomogeneous diffusion of Ga from the GaAs(Sb) buffer layer during InAs growth as confirmed in cross-sectional HAADF STEM and electron energy loss spectroscopy (EELS) (Supplementary Sections III and IV). Such material intermixing will affect the electrical properties locally due to associated distortions of the band structure or defect states. As dislocations and stacking faults occur on a scale much shorter than L_D we expect that they mainly affect average electrical parameters such as the mobility, and contribute less to device-to-device variation. The impact of stacking faults on the mobility has been shown previously for out-

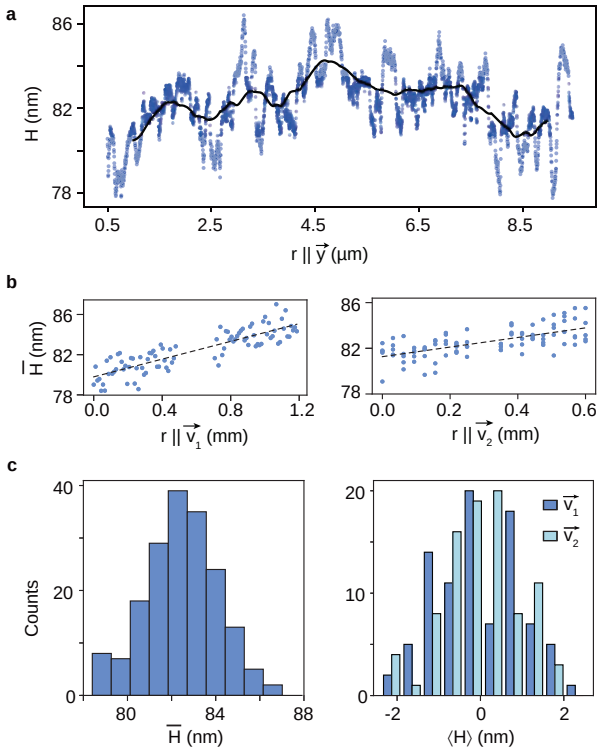

FIG. 2. **a** The height, H, defined in Fig. 1**c** along a typical SAG nanowire in the array of Fig. 1. The black curve shows the running average over 1 μm. **b** H averaged over a middle 1 μm segment for nanowires located along $\vec{v}_1$ ($\vec{v}_2$) as defined in Fig. 1**b**. The dashed lines are linear fits. **c** Histograms of the average $\overline{H}$ and the corresponding residuals $\langle H \rangle$ after subtracting linear fits to data in panels b, quantifying short-range variation between wires of the array.

of-plane InAs nanowires[25], and a significantly improved mobility was observed in Ref.[12] by suppressing the formation of crystal faults.

On an intermediate scale ($\sim$ 20 − 100 nm), etch roughness of the lithographically defined growth apertures and effects of random growth nucleation on the SiO_2 mask can lead to local structural variations along nanowires. Even larger scale modulations across the array (μm − mm) could arise from spatial variations in substrate temperature and adatom flux density across the substrate. To quantify these effects, detailed topographic AFM maps were acquired of 180 individual nanowires located at the positions of the white squares in Fig. 1**b**. An example of the average profiles of a 1 μm long segment from a complete nanowire structure, and from a GaAs(Sb) reference growth are shown in Fig. 1**c**, where the colored bands represent the standard deviation. As a characteristic parameter quantifying the morphological variations along nanowires and between nanowires of the array, an automatic procedure was developed to extract the maximum height, H, at each measured point along each nanowire (See Supplementary Section V). As the cross-sectional shape is defined by the [1 1 1] and [1 $\bar{1}$ $\bar{1}$] crystal planes, other dimensions scales with H..

As an example, Fig. 2**a** shows H along the length of a single nanowire having an average height of 82.3 nm and a standard deviation of $\pm$0.9 nm. The black curve shows the running average, $\overline{H}$, using a 1 μm averaging interval, relevant for comparison with L_D = 1 μm FET devices as discussed below. The relative standard deviation of $\overline{H}$ along the length of the nanowire is 1.5%. To further quantify this and to investigate systematic variations also across the array, Fig. 2**b** shows $\overline{H}$ from the center of each of 180 individual nanowires measured at positions along two directions across the array ($\vec{v_1}$ and $\vec{v_2}$ in Fig.1). $\overline{H}$ increases along both directions and linear fits yield slopes of 4.4 nm/mm and 4.2 nm/mm along $\vec{v_1}$ and $\vec{v_2}$, respectively. Assuming that the linearity extends across the entire array, a plane-fit of $\overline{H}(x, y)$ using these slopes yields an estimate of a maximum of 6% variation of $\overline{H}$ across a distance of 1 mm on the substrate. We attribute this variation to large-scale spatial modulation of the substrate temperature during growth[26]. Such considerable variations could be important for integrated nanowire circuits covering a significant area. In addition to the overall trend observed in $\overline{H}$, variations between neighboring nanowires are clearly significant. To quantify this, Fig. 2**c** shows histograms of $\overline{H}$ centered at 82.4 $\pm$ 1.6 nm and the residuals of $\overline{H}$ after subtracting the linear trend along $\vec{v_1}$ and $\vec{v_2}$. The standard deviation σ_H = 0.97 nm (1.1% of $\overline{H}$) corresponds to the average small-range height variations between the nominally identical nanowires.

Having discussed the structural variability across the array, we now consider the corresponding distribution and reproducibility of low-temperature electrical characteristics for nominally identical devices. A cryogenic, on-chip multiplexer/de-multiplexer circuit was used to enable the characterization of 256 individual, lithographically identical SAG nanowire FETs in a single cool-down (See Ref.[23] for details). Individual nanowires were electrically contacted by Ti/Au electrodes in an FET geometry keeping a constant channel length of L_D = 1 μm and top-gates separated from the InAs channel by 15 nm of HfO_2. Figure 3**a** shows an SEM micrograph of a part of the studied device array which is situated in the row indicated by the red arrow in Fig. 1**b**. The MUX circuit, which is shown schematically (an optical microscope image of the entire circuit is shown in Supplementary Section VIII.), addresses devices in pairs, and two gates (V_{G1}, V_{G2}) are used for the final selection; if one gate is active for a particular device, the other gate is inactive due to screening by the contact metal (insets to Fig. 3a). In the following, we denote the potential of the active gate of any device by V_G.

Figure 3**b** shows three representative examples of the conductance as a function of gate voltage, $G(V_G)$, measured at T = 20 mK. Typical n-type depletion mode FET behavior is observed as expected for InAs

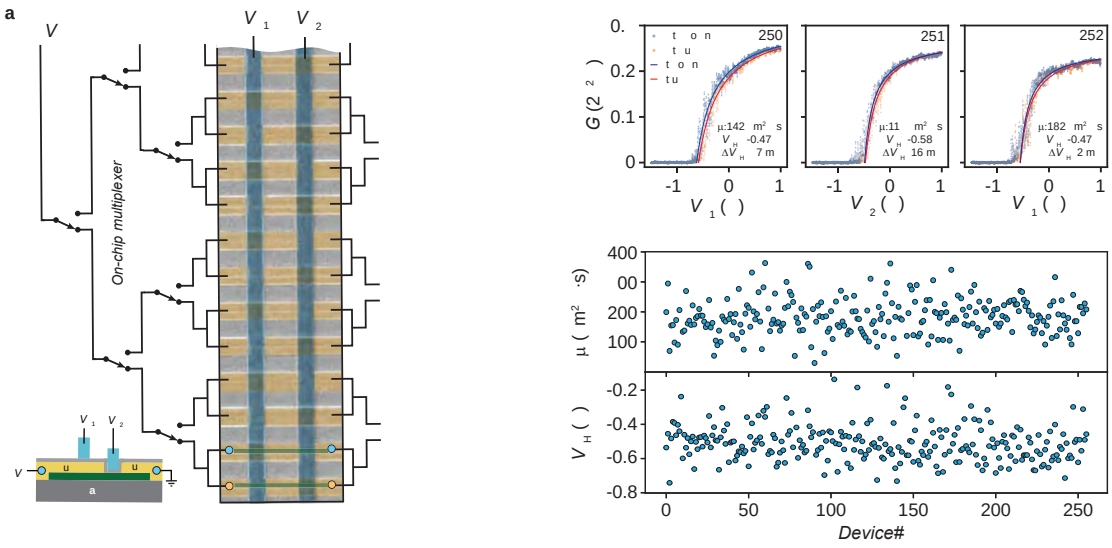

FIG. 3. **a** Schematic illustration of the multiplexer circuit used to address 256 individual SAG nanowire FET devices. The middle image shows a scanning electron micrograph of a part of the device array. Insets show schematic cross-sections of two neighboring devices. Note that the position of the exposed semiconductor segment alternates between devices, thus allowing the final selection to be carried out with the two top gates (V_{G1} and V_{G2}). **b** Example of the conductance as a function of gate voltage for three consecutive devices in the array. Data for the gate sweep towards negative voltage (down) is shown in blue, and towards positive voltage (up) - in orange. Blue and red lines are fits to the expression $G^{-1} = R_s + L^2/(\mu_{FE}C(V - V_{TH})$. Fit parameters for the threshold voltage,V_{TH} and mobility, μ, for the down traces are stated in each case, and panel **c** shows the extracted parameters for all 256 devices in the array.

nanowires. By fitting $G(V_G)$ to the standard expression[27] $G^{-1} = R_s + L_D^2/(\mu_{FE}C(V - V_{TH}))$ – shown as orange lines in Fig. 3**b** – we extract the field effect mobility, μ_{FE}, threshold voltage, V_{TH}, and series resistance, R_s. The series resistance R_s accounts for contact resistance and the resistance of the measurement circuit. Numerical simulation was used to estimate the gate capacitance $C = 5.3\text{fF}$[23], which was used for all fits. Also stated in the figure are values for the difference in threshold voltage between positive (*up*) and negative (*dwn*) V_G sweep directions $\Delta V_{TH} = V_{TH}^{dwn} - V_{TH}^{up}$, used here as a measure of hysteresis.

Since effects of quantum confinement and surface scattering decrease with increasing nanowire dimensions, lower V_{TH} and larger μ are expected[5,28–32] for larger $\overline{H}$. In Ref.[33] we investigated this relationship for InAs SAG nanowire and found approximately linear relationships with $\partial V_{TH}/\partial H = -14.1 \pm 1.0\text{mV/nm}$, and $\partial\mu/\partial H = 12.0\pm2.3\text{cm}^2/\text{Vs}\cdot\text{nm}$. This connects the structural properties and geometric variability discussed above with the variability of the electrical characteristics. If the geometric variability in Fig. 2 is dominating the statistics of the electrical properties, the standard deviations of the $\overline{H}$ distribution, $\sigma_H = 0.97\,\text{nm}$ would lead to a spread in V_{TH} of 13.7 mV and in μ of 11.6 cm^2/Vs.

Figure 3**c** shows μ and V_{TH} extracted for all 256 devices as a function of the position in the array (see Supplementary Sections VI and VII for the underlying data and fitting procedure). Device #1 and #256 are separated on the chip by ~ 0.5 mm and the absence of any clear trend shows that either large scale, systematic structural variations (cf. Fig. 2**b**) are not significant in this array or that other effects dominate the electrical properties. Figure 4**a** shows the distribution of V_{TH}, which provides important information about the gate ranges required for optimal operation large-scale SAG nanowire circuits. In the present case, all devices in the array are in pinch-off (accumulation) for $V_G < -0.8\,\text{V}$, ($V_G > -0.2\,\text{V}$), respectively. The FETs of the MUX circuit (cf. Fig. 3 and Ref.[23]) were operated at $V_G \pm 1\,\text{V}$ to ensure robust closed (open) states[23].

The threshold voltage has a mean value of $\overline{V_{TH}} \approx -530\,\text{mV}$ and a standard deviation $\sigma_{V_{TH}} = 90\,\text{mV}$ ($\sim 17\%$ of $\overline{V_{TH}}$). The larger relative standard deviation of V_{TH} compared to those of $\overline{H}$ suggests significant contributions to the variability from sources not directly detectable through H. One example could be microscopic crystal defects, as discussed above, or the effects of scattering and screening from random, charged impurities in the vicinity of the device. The latter depends on material quality, the quality of oxides, surface adsorbents, the parameters of processing, and experimental conditions. The charged impurity configuration remains stable if the impurity energy depth exceeds the thermal energy

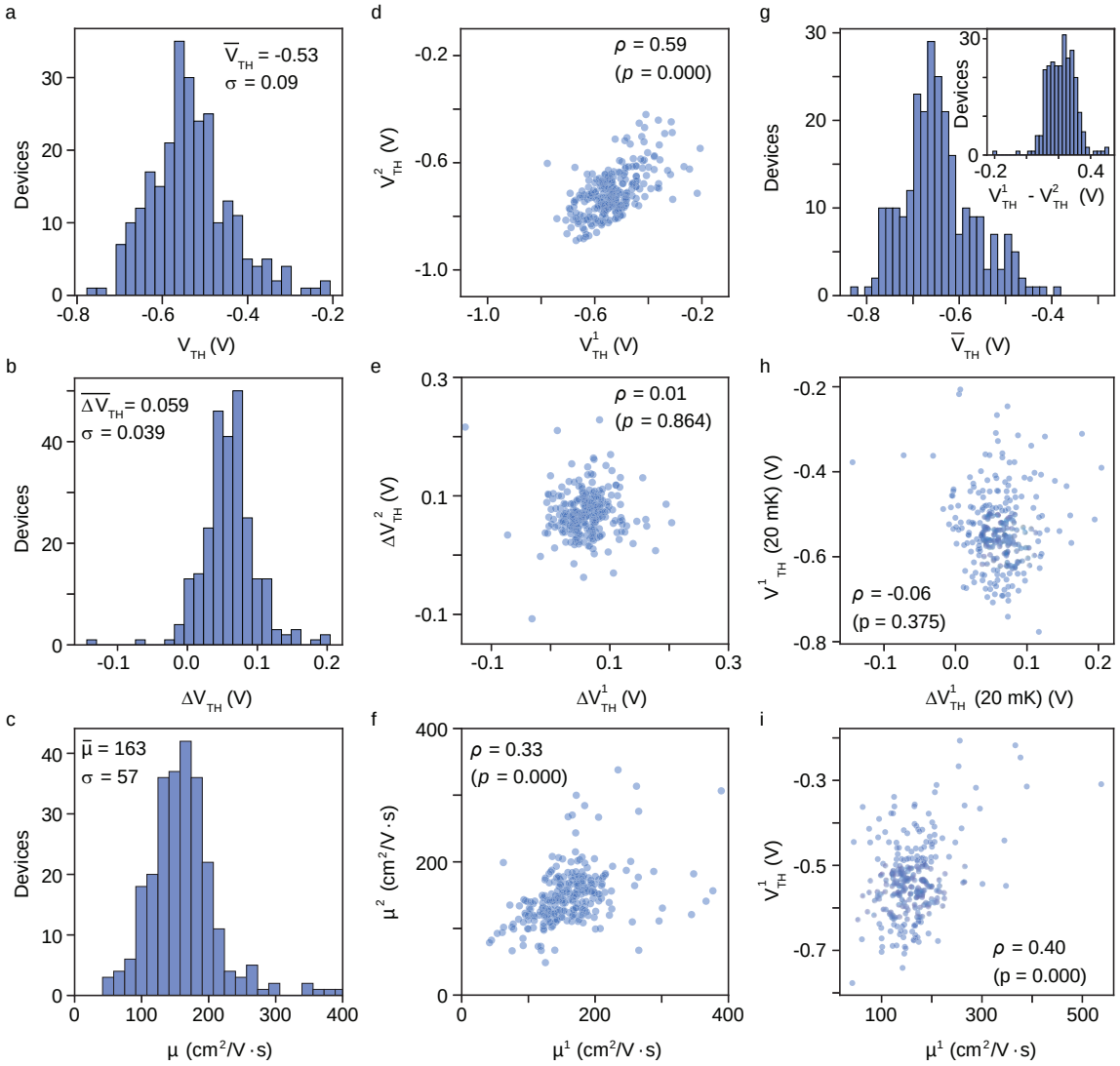

FIG. 4. **a,b,c** Histograms of threshold voltage V_{TH}, hysteresis ΔV_{TH}, and mobility μ, respectively, for 256 devices measured at 20 mK. **d,e,f** Correlations between two cool-downs to 20 mK for V_{TH}, ΔV_{TH}, and μ_{FE} respectively. Pearson's correlation coefficient ρ and the corresponding p-value shown in each panel. **g** Distribution of $\overline{V_{\mathrm{TH}}} = (V^1_{\mathrm{TH}} + V^2_{\mathrm{TH}})/2$ and the differences $(V^1_{\mathrm{TH}} - V^2_{\mathrm{TH}})$ of threshold values measured for the two cool-downs. **h** Correlation between V_{TH} and ΔV_{TH} **i** Correlation between V_{TH} and μ.

and the energy scale of external electrical fields, and we, therefore, expect a static background at the millikelvin temperatures and V_{G} ranges used here. However, thermally cycling the device 20 mK $\rightarrow$ 300 K $\rightarrow$ 20 mK causes a random re-configuration of the charged impurities,[24,34] allowing us to study their contribution to device reproducibility.

Figure 4**d** shows the correlation of the two V_{TH} values measured for each device at base temperature before and after thermal cycling having a correlation coefficient of $\rho = 0.59$. This shows that - although not detectable through H - fixed structural/intrinsic properties partly govern the transport parameters. At the same time, however, a significant scatter in Fig. 4**d** shows that charged impurities - randomized by thermal cycling - also contribute to the overall spread in the V_{TH}. The corresponding distribution in Fig. 4**g** of the mean for each device estimates the structural distribution with a standard deviation $\sigma_{\overline{V_{\mathrm{TH}}}} = 103$ mV which again exceeds the expectation from the variations of $\overline{H}$. We speculate that intrinsic defects such as atomic-scale crystal defects, stacking faults, and material intermixing could be responsible for these

thermal cycling independent variations between devices, which do not show up in the distribution of the geometric parameter $\overline{H}$.

The mobility is influenced by the same structural properties, and the distribution (Fig. 4**c**) and correlations (Fig. 4**f**) show qualitatively similar behavior, albeit with a larger dispersion caused by impurity charges. The hysteresis, ΔV_{TH}, on the other hand, is linked to gate-activated charge traps near the nanowire channel and is thus expected to be less dependent on the structure. This is consistent with the absence of correlations between the values obtained before and after thermal cycling, as seen in Fig. 4**e**.

Fig. 4**h** shows V_{TH} vs. ΔV_{TH} for all devices in the same cool-down. No correlations are observed, which is consistent with the hypothesis that the hysteresis is caused by rearranging surface charges - a process that is independent of the threshold voltage of the device. Similarly, Fig. 4**i** shows V_{TH} vs. μ. Here, both properties are dependent on the structure, and correlation is observed, which indicates that the intrinsic features governing the variation of threshold voltage are related to those determining the mobility.

Combined, the results show that the reproducibility in the values of μ and V_{TH} is influenced approximately equally by fixed structural/intrinsic properties and by the distribution of charged impurities, which vary between cool-downs. Thus, to improve the reproducibility of SAG nanowire transport properties at low temperatures, these results suggest that efforts should target both contributions. The intrinsic contribution cannot be accounted for by variation in the physical dimensions of the SAG nanowires, and thus, variations in composition or crystal defects may be the main source.

In summary, we have presented a comprehensive study of the reproducibility of structural and electrical parameters of nominally identical InAs nanowires realized by selective area growth. Large arrays of nanowires were grown, and statistics on the structural properties were acquired by high-resolution AFM analysis of 180 nanowires systematically spaced across the array. We quantify the nanowire-to-nanowire variability caused by local fluctuations in growth dynamics, lithographic accuracy, and large-scale systematic trends, presumably due to spatial temperature fluctuations across the growth wafer. To acquire statistically significant distributions of electron mobilities, threshold voltages, and hysteresis, we employed an on-chip cryogenic multiplexer design, allowing independent characterization of 256 individual devices. Comparing the spread of values to that expected from the distribution of structural parameters and by correlating values between successive cool-downs to millikelvin temperatures, we quantify the contributions to the variability from intrinsic fixed properties and from charged impurities in the vicinity of the devices.

The $\sigma_{\mathrm{V_{TH}}}$ in our system is comparable to values found in AlGaAs/GaAs 2DEGs[35,36] and foundry cryo-CMOS samples[37,38]. However, it must be noted that the width of the gates in our system is larger than those of Ref.[37,38], and variability is expected to decrease with increasing gate size[37] as the influence of impurities on the electrostatic environment averages over a larger scale[39]. Nevertheless, given that this is the first study of reproducibility of InAs SAG and no specific attempts were made to optimize reproducibility in the studied structures, the results clearly show the potential of the platform. In further experiments intrinsic defects can be reduced by including an intermediary buffer layer[12] and the amount of charged impurities can be reduced by employing in-situ or resist-free processing[40].

The statistical approach developed here will be an important tool for optimizing SAG nanowires and other bottom-up nanomaterials towards large-scale circuits and may motivate efforts towards developing high throughput TEM methodologies enabling statistical correlations between electrical quantum properties and the atomic scale structures. Finally, we emphasize that concerning the SAG nanowires, even with the current, low-mobility structures, reproducibility is sufficient for realizing large-scale functional circuits such as multiplexer/demultiplexer[23] and other logic circuitry. For circuits relying on high μ_{FE} or bandwidth, further optimization of μ_{FE} and the reproducibility of μ_{FE} is needed. The insights developed here will inform future optimization toward quantum devices with even stricter tolerances.

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Competing interests

The authors declare no competing interests.

Supplementary Information

Supplementary information contains extended information on structural characterisation and extended transport datasets.

REFERENCES

[1] Riel, H., Wernersson, L.-E., Hong, M. & del Alamo, J. A. III–V compound semiconductor transistors—from planar to nanowire structures. *MRS Bulletin* **39**, 668–677 (2014).

[2] Alamo, D. & A, J. Nanometre-scale electronics with III–V compound semiconductors. *Nature* **479**, 317–323 (2011).

[3] Gonzalez-Zalba, M. F. *et al.* Scaling silicon-based quantum computing using CMOS technology. *Nat Electron* **4**, 872–884 (2021).

[4] Dick, K. A., Thelander, C., Samuelson, L. & Caroff, P. Crystal Phase Engineering in Single InAs Nanowires. *Nano Lett.* **10**, 3494–3499 (2010).

[5] Ford, A. C. *et al.* Diameter-Dependent Electron Mobility of InAs Nanowires. *Nano Lett.* **9**, 360–365 (2009).

[6] Björk, M. T. *et al.* One-dimensional Steeplechase for Electrons Realized. *Nano Lett.* **2**, 87–89 (2002).

[7] Krogstrup, P. *et al.* Epitaxy of semiconductor–superconductor nanowires. *Nature Mater* **14**, 400–406 (2015).

[8] Wang, N. *et al.* Shape Engineering of InP Nanostructures by Selective Area Epitaxy. *ACS Nano* **13**, 7261–7269 (2019).

[9] Op het Veld, R. L. *et al.* In-plane selective area InSb–Al nanowire quantum networks. *Communications Physics* **3**, 1–7 (2020).

[10] Raya, A. M. *et al.* GaAs nanoscale membranes: prospects for seamless integration of III–Vs on silicon. *Nanoscale* **12**, 815–824 (2020).

[11] Bollani, M. *et al.* Selective Area Epitaxy of GaAs/Ge/Si Nanomembranes: A Morphological Study. *Crystals* **10**, 57 (2020).

[12] Beznasyuk, D. V. *et al.* Doubling the mobility of InAs/InGaAs selective area grown nanowires. *Phys. Rev. Materials* **6**, 034602 (2022).

[13] Friedl, M. *et al.* Template-Assisted Scalable Nanowire Networks. *Nano Lett.* **18**, 2666–2671 (2018).

[14] Lee, J. S. *et al.* Selective-area chemical beam epitaxy of in-plane InAs one-dimensional channels grown on InP(001), InP(111)B, and InP(011) surfaces. *Phys. Rev. Mater.* **3**, 084606 (2019).

[15] Seidl, J. *et al.* Postgrowth shaping and transport anisotropy in two-dimensional inas nanofins. *ACS nano* **15**, 7226–7236 (2021).

[16] Vaitiekėnas, S. *et al.* Selective-area-grown semiconductor-superconductor hybrids: A basis for topological networks. *Physical Review Letters* **121**, 147701 (2018).

[17] Krizek, F. *et al.* Field effect enhancement in buffered quantum nanowire networks. *Phys. Rev. Mater.* **2**, 093401 (2018).

[18] Hertel, A. *et al.* Gate-Tunable Transmon Using Selective-Area-Grown Superconductor-Semiconductor Hybrid Structures on Silicon. *Phys. Rev. Appl.* **18**, 034042 (2022).

[19] Goswami, A. *et al.* Sn/InAs Josephson Junctions on Selective Area Grown Nanowires with in Situ Shadowed Superconductor Evaporation. *Nano Lett.* **23**, 7311–7318 (2023).

[20] Ten Kate, S. C. *et al.* Small charging energies and g-factor anisotropy in pbte quantum dots. *Nano Letters* **22**, 7049–7056 (2022).

[21] Smith, L. W. *et al.* Statistical study of conductance properties in one-dimensional quantum wires focusing on the 0.7 anomaly. *Phys. Rev. B* **90**, 045426 (2014).

[22] Smith, L. W. *et al.* High-throughput electrical characterization of nanomaterials from room to cryogenic temperatures. *ACS nano* **14**, 15293–15305 (2020).

[23] Olšteins, D. *et al.* Cryogenic multiplexing using selective area grown nanowires. *Nature Communications* **14**, 7738 (2023).

[24] See, A. M. *et al.* Impact of Small-Angle Scattering on Ballistic Transport in Quantum Dots. *Phys. Rev. Lett.* **108**, 196807 (2012).

[25] Schroer, M. D. & Petta, J. R. Correlating the Nanostructure and Electronic Properties of InAs Nanowires. *Nano Lett.* **10**, 1618–1622 (2010).

[26] Madsen, M. H., Aagesen, M., Krogstrup, P., Sørensen, C. & Nygård, J. Influence of the oxide layer for growth of self-assisted inas nanowires on si (111). *Nanoscale research letters* **6**, 1–5 (2011).

[27] Gül, Ö. *et al.* Towards high mobility insb nanowire devices. *Nanotechnology* **26**, 215202 (2015).

[28] Choi, Y.-K., Ha, D., King, T.-J. & Hu, C. Threshold voltage shift by quantum confinement in ultra-thin body device. In *Device Research Conference. Conference Digest (Cat. No. 01TH8561)*, 85–86 (IEEE, 2001).

[29] Yuan, Y., Yu, B., Song, J. & Taur, Y. An analytic model for threshold voltage shift due to quantum confinement in surrounding gate mosfets with anisotropic effective mass. *Solid-State Electronics* **53**, 140–144 (2009).

[30] Granzner, R., Schwierz, F. & Polyakov, V. M. An analytical model for the threshold voltage shift caused by two-dimensional quantum confinement in undoped multiple-gate mosfets. *IEEE Transactions on Electron Devices* **54**, 2562–2565 (2007).

[31] Hou, J. J. *et al.* Diameter dependence of electron mobility in InGaAs nanowires. *Applied Physics Letters* **102**, 093112 (2013).

[32] Feng, W., Peng, C., Li, S. & Li, X.-Q. Low-field electron mobility of InSb nanowires: Numerical efforts to larger cross sections. *Scientific Reports* **7**, 1–8 (2017).

[33] Nagda, G. *et al.* Dimension dependent electrical transport in selective area grown inas nanowires. *To be submitted* (2024).

[34] Holloway, G. W., Song, Y., Haapamaki, C. M., LaPierre, R. R. & Baugh, J. Trapped charge dynamics in InAs nanowires. *Journal of Applied Physics* **113**, 024511 (2013).

[35] Al-Taie, H. *et al.* Cryogenic on-chip multiplexer for the study of quantum transport in 256 split-gate devices. *Applied Physics Letters* **102**, 243102 (2013).

[36] Yang, Q.-Z., Kelly, M., Farrer, I., Beere, H. & Jones, G. The potential of split-gate transistors as one-dimensional electron waveguides revealed through the testing and analysis of yield and reproducibility. *Applied Physics Let-*

ters **94**, 033502 (2009).

[37] Zwerver, A. *et al.* Qubits made by advanced semiconductor manufacturing. *Nature Electronics* **5**, 184–190 (2022).

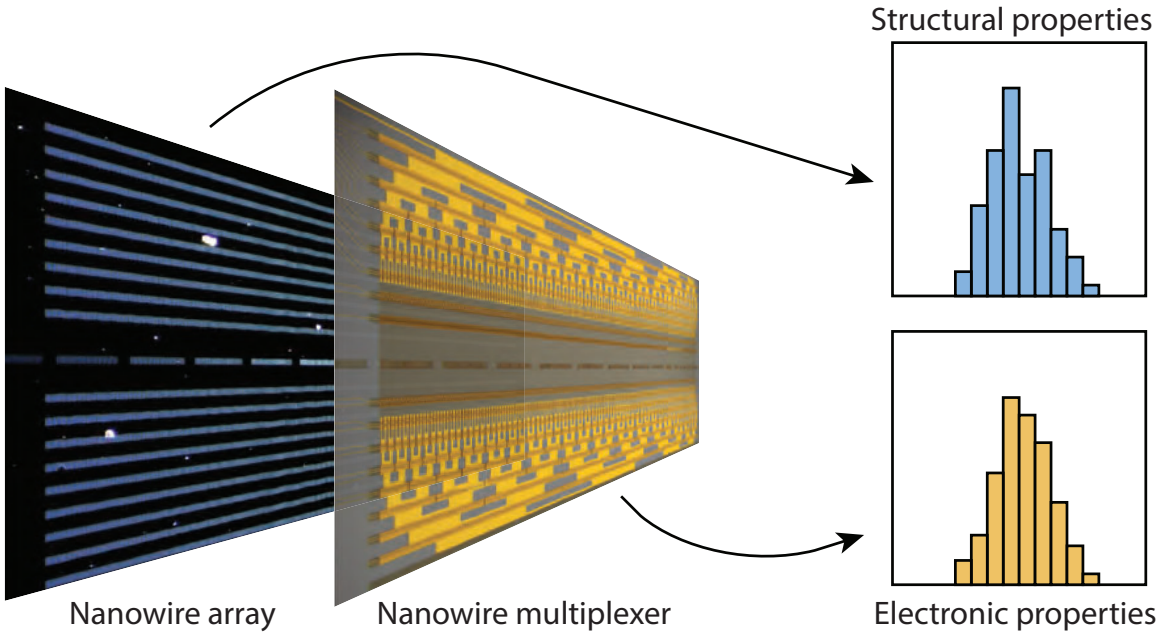
[38] Bavdaz, P. *et al.* A quantum dot crossbar with sublinear scaling of interconnects at cryogenic temperature. *npj Quantum Information* **8**, 86 (2022).

[39] Kuhn, K. J. *et al.* Process technology variation. *IEEE Transactions on Electron Devices* **58**, 2197–2208 (2011).

[40] Heedt, S. *et al.* Shadow-wall lithography of ballistic superconductor–semiconductor quantum devices. *Nat Commun* **12**, 4914 (2021).

Data Availability

The data supporting the findings is available at https://doi.org/10.11583/DTU.24967755


Structural properties
Nanowire array
Nanowire multiplexer
Electronic properties