Letters

Analysis of the Voltage Ramp Rate Effects on the Programming Characteristics of Bipolar-Type Memristive Devices

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***Abstract*—We investigate in this letter the role the voltage ramp rate plays in the conduction and programming characteristics of bipolar-type memristive devices. It is shown that speeding up the writing or erasing process of a memristor is beneficial in terms of energy consumption but has a side cost associated with power dissipation. This happens because of the dynamical aspects of the set and reset transitions which are ultimately dictated by the physics of metal ions and oxygen vacancies migration. It is shown that by adding a constant base voltage to the voltage sweep, shorter programming times can be achieved but no significant impact on the power dissipation-energy consumption relationship is observed. Modeling and simulations are carried out with the aid of the Dynamic Memdiode Model and its implementation in LTspice using the Method of Elementary Solvers. Since the device model parameters and simulation conditions can vary in a wide range, the complete schematics are provided so that the interested readers can test different casuistries by themselves.**

***Index Terms*—Memristor, resistive switching, energy consumption, power dissipation, SPICE, LTspice.**

I. Introduction

THE effect of the voltage ramp rate (*RR*) on the conduction characteristics of bipolar-type memristive devices has been the subject of numerous investigations [1], [2], [3], [4], [5], [6], [7], [8], [9], [10]. It has been clearly established that not only the maximum voltage but also how this voltage is applied determine the so-called set (V_{SET}) and reset (V_{RES}) voltages, i.e., the voltages at which the device switches on and off, respectively. However, to the best of our knowledge, the connection between *RR*, power dissipation, and energy requirements for setting a device to a specific conductance level as required for instance in analog neuromorphic computing (synaptic weight) has not been clarified so far. The main difficulty arises because the memristor behavior involves a system of two coupled nonlinear equations, one for the current magnitude and one for the memory state of the device [11], which imperatively requires the use of a circuit solver. Simulation and analytic results allow us to unveil that the key issue behind the memristor programming and erasing features is the interplay between the internal transition dynamics, expressed in terms of the characteristic switching times $\tau_{\mathrm{S,R}}$, and the external stimulus determined by *RR*. Notice that a ramped signal is in practice nothing but a sequence of pulses with increasing height. With the aid of the Dynamic Memdiode Model (DMM) [12], [13], [14] and its novel implementation in the LTspice circuit simulator using the Method of Elementary Solvers (MES) [15] we are able to clarify some crucial points about this challenging problem. For the sake of completeness, the circuit schematics for assessing the energy and power requirements are provided.

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II. Model Equations and Elementary Solver Method

According to the DMM, the current-voltage (*I-V*) characteristic of a bipolar-type memristive device is governed by the following system of coupled equations [13]:

$$I\ (V_A) = \left[(I_{on} - I_{off})\, g + I_{off}\right]\ \sinh\left(\alpha V_C\right) \tag{1}$$

$$\frac{dg}{dt} = \frac{1-g}{\tau_S\left(V_B\right)}\ - \frac{g}{\tau_R\left(V_B\right)} \tag{2}$$

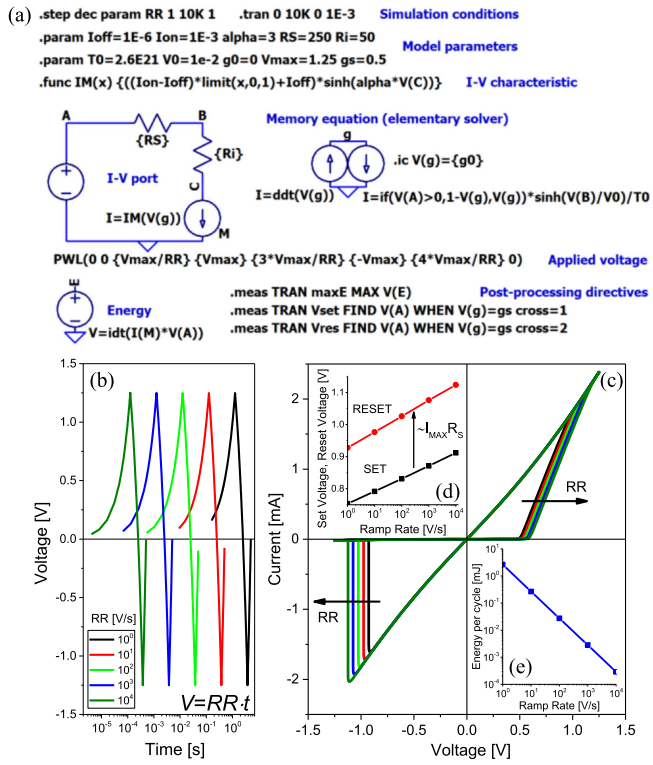

Fig. 1. (a) DMM model schematics: one mesh for the *I-V* characteristic (includes the snapback resistance R_S and internal resistance R_i) and one mesh for the memory state of the device (elementary solver). Three post-processing directives are used to calculate the energy as well as V_{SET} and V_{RES}. (b) Positive and negative linear voltage sweeps (log-axis) varying *RR* in decades. (c) *I-V* loops illustrating the shift of V_{SET} and V_{RES} with *RR* (d) and the energy required to perform the loop as a function of *RR* (e).

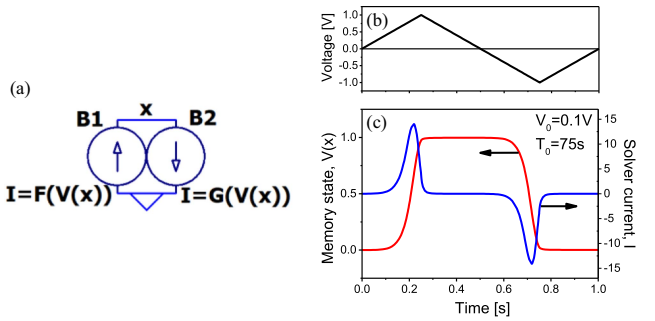

Fig. 2. (a) General form of an elementary solver. F and G are two arbitrary functions for the behavioral current sources B1 and B2, respectively. *x* is a circuit label and V(x) the voltage at the central node. (b) Applied signal. (c) Evolution of the solver current *I* and memory state V(x) as a function of time for the model equations shown in Fig. 1(a).

where α is a constant, and I_{on} and I_{off} are the maximum and minimum currents, respectively. The difference between the voltages V_A, V_B and V_C has to do with the series resistances R_S and R_I (see the node labels in Fig. 1(a)). From (1), and considering $V_C << 1$, $0 \leq g \leq 1$ is the low-voltage normalized conductance of the device (memory state@reading voltage):

$$\frac{G - G_{\min}}{G_{\max} - G_{\min}} = \frac{[(I_{on} - I_{off})\, g + I_{off}]\, \alpha - I_{off}\alpha}{I_{on}\alpha - I_{off}\alpha} = g \tag{3}$$

For the sake of simplicity, we assume in this work symmetric set ($V>0$) and reset ($V<0$) characteristic switching times:

$$\tau_{S,R}(V) = T_0\, csch\left(\frac{|V|}{V_0}\right) \tag{4}$$

with T_0 and V_0 constants. The generalization to asymmetric times is straightforward. (4) corresponds to the exponential drift times for vacancies and metal ions [16] with the correction for null applied voltage, $\tau(V \to 0) \to \infty$ [17]. For a ramped voltage sweep $V = RR \cdot t$ in the low-bias positive region (all resistances are neglected), from (2):

$$\frac{dg}{dt} = \frac{dg}{dV}\frac{dV}{dt} = \frac{dg}{dV}\, RR \approx \frac{1 - g}{2T_0 exp\left(-\frac{V}{V_0}\right)} \tag{5}$$

which yields

$$\frac{dg}{dV} = \frac{1 - g}{exp\left\{-\frac{1}{V_0}\left[V - V_0 ln\left(2T_0 RR\right)\right]\right\}} \tag{6}$$

so that we obtain as a first approximation:

$$V_{SET} \approx V_0\left[ln\left(RR\right) + ln\left(2T_0\right)\right] \tag{7}$$

in agreement with experimental results [5], [9], [10]. This logarithmic dependence of V_{SET} (similarly for V_{RES}) with *RR* is central to our discussion concerning the energy consumption ($E = \int P(t)dt$) and maximum dissipated power ($P_{Max} = I_{Max}\, V_{Max}$) occurring in the device during a switching loop [18], [19], [20], [21].

Next, we focus the attention on the LTspice implementation of the differential (2). To this end, we use the recently proposed MES [15]. This method consists in considering two opposite biased behavioral current sources with values F[V(x)] and G[V(x)] forming a single mesh as illustrated in Fig. 2(a). F and G are two arbitrary functions and V(x) is the voltage at the central node. V(x) is the voltage that matches the two currents as follows from Kirchhoff's laws, i.e., V(x) is the solution of the equation F(x) = G(x). Notably, the method eliminates the use of the storage capacitor in the memory circuit of a memristor [13] and benefits from the direct use of the behavioral components offered by LTspice. As an example, Fig. 2 shows the memory state and the solver current as a function of time (Fig. 2(c)) for a ramped signal of 1 Hz (Fig. 2(b)). As shown in Fig. 1(a), the elementary solver is coupled with the *I-V* port to solve the memristor behavior. In that figure, g_0 is the initial value of g and g_S the value of g at which the model output features are evaluated. *PWL* (piecewise linear) represents the applied signal as a function of *RR* and V_{MAX}. The function *limit* is used to ensure that the memory state values remain within the allowed limits. *ddt* is the time derivative and *idt* the time integral used to compute the energy *E*. Fig. 1(b) shows the applied signal for different *RR* values (log-scale in time) and Fig. 1(c) the corresponding *I-V* loops including V_{SET}, V_{RES} and *E* as a function of *RR*. Notice the V_{SET} and V_{RES} shifts as predicted by (7). As a result of the model equations, the energy per cycle *E* decreases as the sweep rate *RR* increases. Relaxation effects occurring after reaching

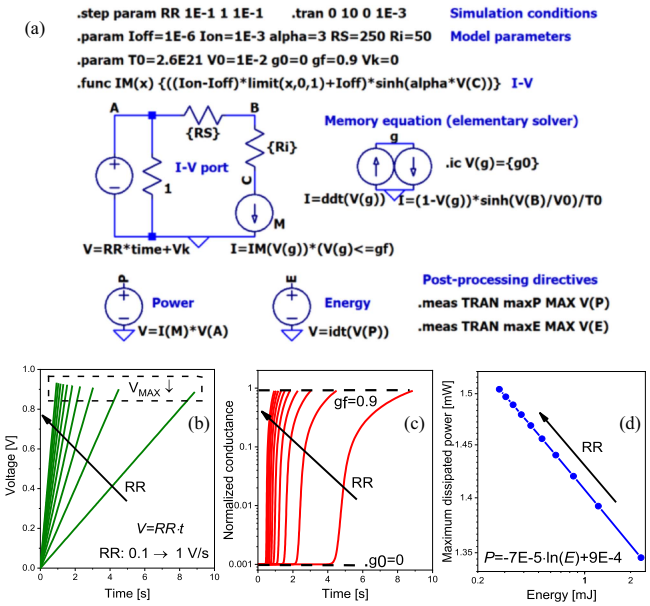

Fig. 3. (a) DMM model schematics for a set transition. Two post-processing directives are used to calculate the energy E and the maximum power P_{Max}. (b) Voltage sweeps with varying RR. Notice that the maximum voltage increases with RR. (c) Evolution of the low-voltage conductance towards a final value g_f. (d) Relationship between energy and power as a function of RR.

the target state g_f are completely disregarded since they do not contribute to either P_{Max} or E.

III. Memristor Programming With a Voltage Ramp

In the previous Section, the model equations and outcomes for complete loops were analyzed. In this Section, we applied the same framework to the programming case of a memristor using a ramped voltage [22], [23], [24]. The problem consists in finding the time required to program a device to a certain final conductance state g_f and evaluating E and P_{Max}. When the target condition is fulfilled, the programming current is derived through a shunt resistor (1 Ω). This allows performing stepped measurements in LTspice without changing the total simulation time. Fig. 3(a) illustrates the circuit schematics for a set transition. As RR increases, the maximum applied voltage required to reach the final state $g_f = 0.9$ (arbitrary value) increases as well (Fig. 3(b)). As expected, the target conductance is reached earlier (Fig. 3(c)) but as E decreases, P_{Max} increases (Fig. 3(d)). A clear tradeoff between energy and power is found. Notice the logarithmic power dissipated-energy consumption relationship. This is consistent with previous results obtained for nonlinear voltage sweeps with programming time constraints [22].

Now, let's analyze the case in which we add a base voltage V_k to the original ramp, i.e., $V = RR \cdot t + V_k$. This is equivalent to an initial ramp value. Integrating (2), the normalized conductance state as a function of time reads:

$$g\ (t) = (g_0 - 1)\ \ exp\left\{\frac{V_0}{RRT_0}\left[\cosh\left(\frac{V_k}{V_0}\right) - \cosh\left(\frac{RRt + V_k}{V_0}\right)\right]\right\} + 1 \tag{8}$$

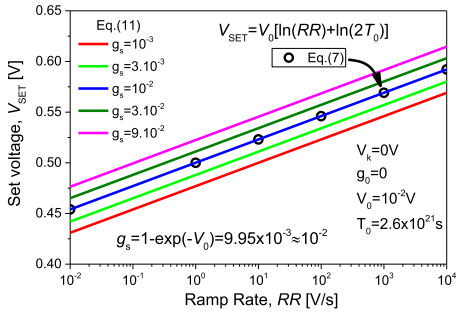

Fig. 4. Set voltages corresponding to different memory states as a function of the voltage ramp rate. (7), which is frequently used to assess experimental data is associated with a particular memory state gs (given by (14)).

which reduces to:

$$g_{RR=0}\ (t) = (g_0 - 1)\ \ exp\left\{-\sinh\left(\frac{V_k}{V_0}\right)\frac{t}{T_0}\right\} + 1 \tag{9}$$

when no ramp is applied (constant voltage programming). This case corresponds to the application of a sequence of pulses of equal height V_k disregarding relaxation effects. When no base voltage is considered (ramped voltage programming) (8) yields:

$$g_{Vk=0}\ (t) = (g_0 - 1)\ \ exp\left\{\frac{V_0}{RRT_0}\left[1 - \cosh\left(\frac{RRt}{V_0}\right)\right]\right\} + 1 \tag{10}$$

Importantly, from (8), it is also possible to find the exact expressions for the set voltage V_{SET} (defined as $V@g_s$):

$$V_{SET} = V_0\ arcosh\left[\cosh\left(\frac{V_k}{V_0}\right) - \frac{RRT_0}{V_0} ln\left(\frac{1-g_s}{1-g_0}\right)\right] \tag{11}$$

and for the set time t_{SET} (defined as $t@V_{SET}$):

$$t_{SET} = \frac{V_{SET} - V_k}{RR} \tag{12}$$

Equations (11) and (12) clearly show that the set process is both a function of the switching material properties (T_0, V_0) and the kind of electrical stimulus applied (RR, V_k). (11) also reveals that (7) is just an approximate expression. More in detail, the connection between (7) and (11) can be found assuming $V_k = 0$, $g_0 = 0$:

$$\begin{aligned} V_{SET} &= V_0\ arcosh\left[1 - \frac{RRT_0}{V_0}\ln(1-g_s)\right] \\ &\approx V_0 ln\left[-\frac{2RRT_0}{V_0}\ln(1-g_s)\right] \end{aligned} \tag{13}$$

so that from (7) and (13):

$$g_S = 1 - exp(-V_0) \tag{14}$$

Equation (14) reveals that the linear relationship V_{SET}-$ln(RR)$ with slope V_0 given by (7), often used to analize experimental results [3], [9], corresponds to a particular memory state value (g_s). The connection between (7), (11), and (14) is illustrated in Fig. 4.

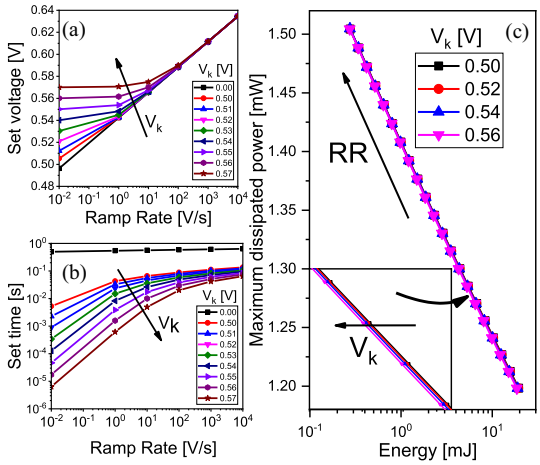

Fig. 5. (a) Set voltage (11) as a function of the ramp rate *RR* and base voltage V_k. (b) Set time (12) as a function of the ramp rate *RR* and base voltage V_k. (c) Relation between the maximum dissipated power and the energy required to reach a final target conductance. Model parameters in Fig. 3(a).

Fig. 5 illustrates the roles played by V_k and *RR*. As shown in Fig. 5(a), V_{SET} increases with *RR* and converges to V_k for low ramp rates. In this analysis, V_{SET} can never be lower than V_k. On the contrary, for high *RR*, V_{SET} becomes independent of V_k. Accordingly, Fig. 5(b) shows that t_{SET} strongly depends on V_k for low *RR* values and reduces its spread as *RR* increases because of the leading role of V_{SET} over V_k. Fig. 5(c) shows that the power dissipation-energy consumption plot is not significantly affected by V_k although a small shift towards lower energy values is observed (see the inset). Notice that the relevance of V_k can largely depends on the model parameters and test conditions.

IV. Conclusion

Power dissipation and energy consumption are key elements in any electrical system. Power dissipation (P_{Max}) is related to Joule heating and power supply requirements while energy consumption (E) concerns efficiency and sustainability. In this letter, the connection between P_{Max} and E was investigated in detail for the case of a bipolar-type memristor subjected to linear programming conditions. The observed tradeoff between power and energy is a consequence of the interplay between the applied signal and the internal response of the device. LTspice schematics were provided to let researchers investigate their own structures as well as the variety of experimental conditions.

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