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Resistive Switching phenomenon in FD-SOI Ω-Gate FETs: Transistor performance recovery and back gate bias influence☆

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ABSTRACT

Resistive Switching (RS) phenomenon, usually observed in two-terminal memristor devices, refers to the reversible change in resistance of a material under an external electric field. In this work, RS has been observed in N-type Fully Depleted Silicon-On-Insulator (FDSOI) Ω-gate nanowire field-effect transistors (NW-FETs). For the first time, partial recovery of the transistor's I_D-V_D characteristics during the RS cycling is experimentally demonstrated, indicating the potential of the device to be used both as a transistor and a memristor. The effect of increasing the back gate voltage on the RS characteristics was also experimentally investigated. It was found that higher back gate voltages enhance the RS parameters, thereby establishing a direct relationship between back bias and device performance.

1. Introduction

Resistive Switching (RS) phenomenon, as the basis of memristor devices, has acquired significant interest in the scientific community because of its potential in memory, logic, security, neuromorphic applications, etc. [1]. RS is typically observed in two terminal structures that incorporate a dielectric material between their terminals, such as Metal-Insulator-Metal (MIM) or Metal-Insulator-Semiconductor (MIS) devices. RS involves the reversible change of the conductivity of the dielectric material: the larger conductivity corresponds to a Low Resistance State (LRS), while the smaller correspond to a High Resistance State (HRS) [2]. These changes in the dielectric resistance are achieved by applying an appropriate voltage to the device terminals. The resistance states associated to the RS phenomenon are linked to the formation of a conductive path (CP) through the dielectric, which in some devices is generated through an initial electroforming process, referred to as 'forming' (see Fig. 2A). The transition from HRS to LRS is named as 'set' process, while the transition from LRS to HRS is named as 'reset' process (see Fig. 2B).

Though RS is usually exploited in two terminal devices, RS was observed in bulk MOSFETs [4] and more recently also in FD-SOI quasi-planar transistors [3], which opens the possibility of using the device as either a transistor or a memristor, as necessary [4]. In [3], the electrical conditions used to observe the RS caused significant damage to the transistor's functionality. In contrast to that study, this work analyzes the RS voltage and current conditions required to partially recover the I_D-V_D curves. On the other hand, in these devices the back gate voltage (V_B) influences transistor's performance [5–7]. In this work, for the first time, the effect of V_B on RS is evaluated.

2. Device description

The N-type Ω-gate NW-FETs used in this work were fabricated at CEA-LETI with SOI (Silicon on Insulator) technology and have L = 10 μm gate length and W = 10 μm width [7]. Their planar and cross-section representations are shown in Fig. 1A and Fig. 1B, respectively. The device is a single finger structure with a nanowire height (H_{NW}) of 11 nm. The buried oxide layer (BOX) has a thickness of 145 nm (see Fig. 1B). Because the large difference between the gate length and width (L = 10 μm x W = 10 μm) compared to the nanowire height (H_{NW} = 11 nm), the device can be considered as a quasi-planar SOI MOSFET [7] (Fig. 1C).

Electrical measurements were carried out using an Agilent 4156C Precision Semiconductor Parameter Analyzer, to obtain the I_G-V_G and I_D-V_D curves of the devices.

3. Results and discussion

This section experimentally analyses the possibility of recovering the

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transistor's characteristics during a complete RS cycle. Additionally, the impact of the back gate voltage on RS is experimentally evaluated.

3.1. Partial recovery of transistors characteristics during RS

Fig. 2 shows the I_G-V_G curves measured during the forming process (Fig. 2A) and a complete RS cycle, i.e. a reset followed by a set. (Fig. 2B). The electrical conditions applied in the electroforming process (Fig. 2A) are a continuous voltage sweep ranging from $V_G = 0$ V to 4 V, with a current compliance limit of 4 mA for the gate current (I_G).The reset process was measured by applying a negative voltage ramp to the gate terminal, ranging from $V_G = 0$ V to −2V, with gate current compliance of $I_G = 8$ mA (Fig. 2B Left). The set process was measured by applying positive voltages to the gate terminal, ranging from $V_G = 0$ V to 4 V with a gate current limit of $I_G = 4.5$ mA (Fig. 2B Right). The device shows bipolar switching. A reversible dielectric breakdown is a potential mechanism underlying resistive switching (RS). It occurs within a localized area of the insulator, where a CP forms through the dielectric, facilitating the RS phenomenon [8–10].

The I_D-V_D characteristics were obtained by applying voltage ramps to the drain terminal, with voltages ranging from $V_D = 0$ V to 1.2 V, while setting the gate voltage at $V_G = 0.3$ V, 0.6 V, 0.9 V and 1.2 V and the back gate voltage at $V_B = 0$ V. The I_D-V_D curve of the fresh sample (i.e., before forming) is depicted in Fig. 2C. The I_D-V_D characteristics of the transistor measured after the forming process are illustrated in Fig. 2D. Note that in a reduced drain voltage range (from 0 to 0.1 V), larger currents than for the fresh case and a negative dependence with voltage is observed, reaching $I_D = 0$ at $V_B = 0.1$ V. However, for larger voltages, a similar shape is observed, though with smaller currents, when compared to the fresh case (Fig. 2C), indicating that the device can be still operated as a FET.

The transistor's I_D-V_D curves following reset and set processes are shown in Fig. 2E and Fig. 2F, respectively. Similar trends than those described for the post-forming curves are observed, i.e. an initial voltage range that shows negative resistance followed by typical MOSFET behaviour. However, focusing the attention in the last case, the current levels depend on the dielectric state: when compared to the values measured in the fresh device, smaller currents are observed after set but currents are similar after reset. Then, the transistor current driving capability is partially recovered after undergoing the reset process (Fig. 2E). As an example, I_D after reset process measured at $V_G = 1.2$ V and $V_D = 1.2$ V decreases approximately 9 % with respect to the corresponding current of the fresh sample (see I_D-V_D characteristic in Fig. 2C and Fig. 2E), preserving the transistor functionality. This result was validated through several experiments, which revealed that by reducing the current compliance ($I_G = 8$ mA) and limiting the gate voltage ($V_G = -2$V) during the reset process, the transistor is still operative, though the operating voltage region has slightly changed, as shown in Fig. 2E and 2F.

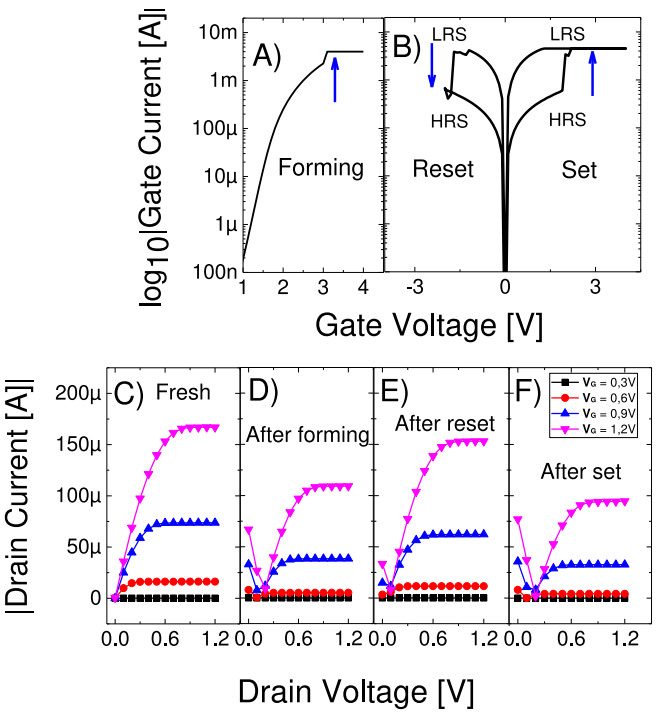

Fig. 2. Experimental I_G -V_G curves for A) forming, B) reset and set processes. I_D -V_D transistor characteristics at different gate voltages for C) a fresh device. D) after forming. E) after reset and F) after set processes. In all cases, $V_B = 0$ V.

3.2. Impact of the back gate bias on RS

In this section, it will be preliminary analyzed the impact of the back gate bias on the RS phenomenon in these devices. Fig. 3 illustrates the measurement procedure for three distinct cases used to compare the influence of the back gate bias voltage in the set and reset processes. In the first case (Fig. 3A), a positive voltage sweep from 0 to 4 V is applied to the gate terminal (V_G) while a constant negative voltage is simultaneously applied to the back gate terminal. Voltages of $V_B = 0$, −0,1V, −0.2 V, −0,3V and −0,4V are considered. This voltage configuration will be used to analyze the V_B impact on the RS cycle applying these conditions only on set process ($V_B = 0$ V during the reset process). In the second case (Fig. 3B), a negative voltage sweep from 0 to −2V is applied to the gate terminal (V_G), with a constant negative voltage of $V_B = -0.2$ V applied simultaneously to the back gate terminal. This voltage configuration will be used to analyze the V_B impact on the RS cycle applying these conditions only on the reset process ($V_B = 0$ V during the set process). In the third case (Fig. 3C), a positive voltage sweep (from 0 to 4 V) is applied to the gate terminal (V_G) Immediately following this, a negative voltage sweep (from 0 to −2V) is applied to the gate terminal. The back gate terminal is biased with a constant negative voltage of $V_B =$

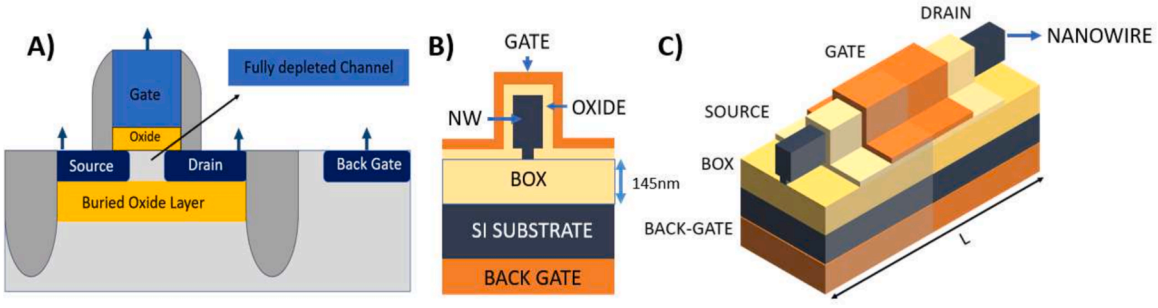

Fig. 1. Planar representation of the FD-SOI FET (A) cross section of the Ω-gate Nanowire (B) 3D sketch (not in scale) of the FD-SOI quasi-planar transistors used in this work (C).

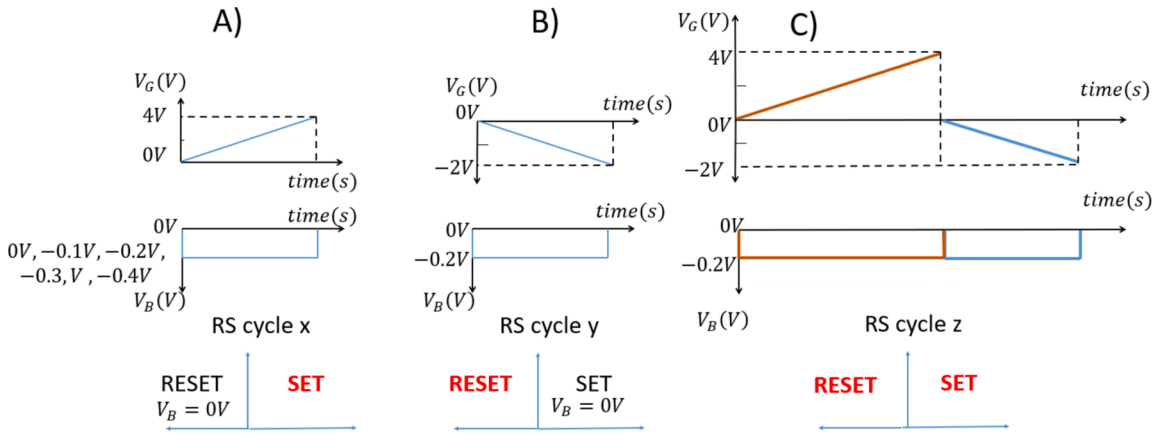

Fig. 3. Measurement procedure of three different approaches used to compare back gate voltage influence in RS set and reset events A) V_B = 0 V, −0.1 V, −0.2 V, −0.3 V, −0.4 V during set process B) V_B = − 0.2 V during reset process C) V_B = − 0.2 V during reset and set processes.

−0.2 V, during both the set and reset processes. This voltage configuration will be used to analyze V_B impact on the complete RS cycle applying $V_B \neq 0$ V.

Fig. 4 shows the average of three RS cycles, when V_B is only applied during the set process (voltage configuration shown in Fig. 3A.), for the cases of V_B = 0 V (Fig. 4A), − 0.1 V (Fig. 4B), − 0.2 V (Fig. 4C), − 0.3 V (Fig. 4D) and − 0.4 V (Fig. 4E). To evaluate the impact of V_B on the device performance, the I_{ON}/I_{OFF} ratio has been used as parameter to describe the device performance. I_{ON} is measured when the sample is in the LRS, and I_{OFF} is measured when the sample is in the HRS, at V_G = −1V and V_G = +1V (see Fig. 4A and D). This mean ratio is calculated over three cycles for each voltage configuration using a single sample. Fig. 5 shows the I_{ON}/I_{OFF} mean ratio measured at V_G = −1V and V_G = +1V as a function of V_B. The increasing I_{ON}/I_{OFF} ratio (averaging all the cycles) measured at V_G = -1V shows an increase with V_B (see Fig. 5 blue solid line) and it facilitates the distinction between the memristor

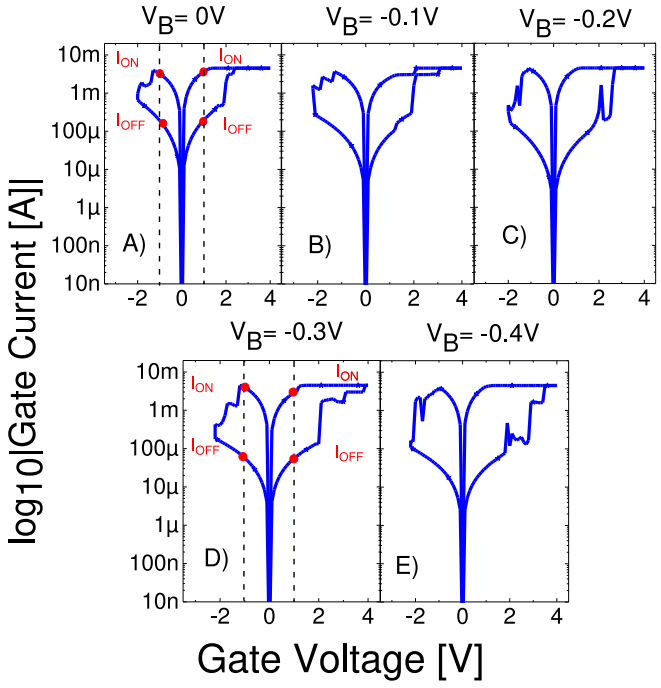

Fig. 4. RS I-V average curves of several cycles measured on the same sample when A) V_B = 0 V, B) V_B = -0.1 V, C) V_B = -0.2 V, D) V_B = -0.3 V, E) V_B = -0.4 V during set process. In (A) and (D) the I_{ON} and I_{OFF} currents measured at V_G = −1V and V_G = +1V to obtain the I_{ON} /I_{OFF} ratio are illustrated.

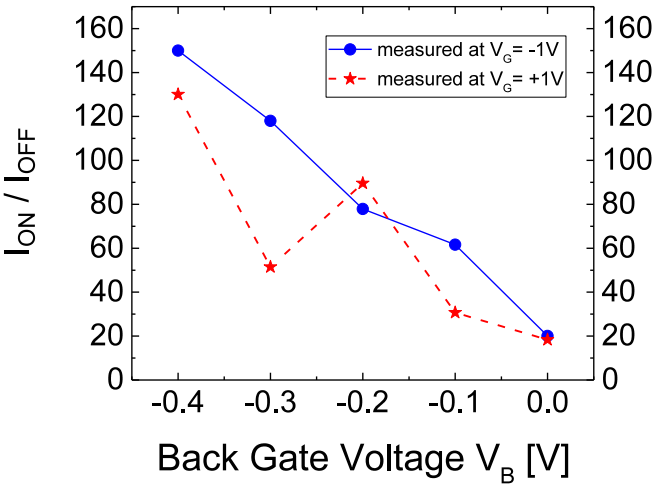

Fig. 5. I_{ON}. I_{OFF} mean ratio measured at V_G = -1V (blue) and at V_G = +1V (red) as a function of back gate voltage (V_B) for the measurements represented in Fig. 4.

conduction states, which is beneficial for memory applications. However, this I_{ON}/I_{OFF} ratio shows no stable increment with V_G when it is measured at V_G = +1V (see Fig. 5 red dash line). This can be attributed to the transversal electric field effect at negative back gate voltages in these wide-channel devices (W = 10 μm) [7], due to the total voltage applied to the structure. This electric field can affect the conductive filament structure during RS, especially during the reset process, decreasing the dielectric conduction (see Fig. 4), and consequently, increasing the I_{ON}/I_{OFF} ratio.

Fig. 6A shows the average of three RS cycles obtained when V_B= − 0.2 V during the reset process and V_B = 0 V during the set process (configuration in Fig. 3B). Fig. 6B shows the average of three RS cycles when V_B= − 0.2 V during both reset and set processes (configuration in Fig. 3C). The I_{ON}/I_{OFF} mean ratio (averaging all the cycles) for the curves in Fig. 6A and 6B, respectively are qualitative equal. Note that, when compared to the case of V_B = 0 V during the reset (Fig. 4C), in both cases, no significant impact of V_B on the I_{ON}/I_{OFF} mean ratio is observed, as far as can be expected in two different samples. These preliminary results suggest, in contrast to the experiment in Fig. 4, seems to indicate that there is no significant impact of V_B on RS characteristics when the reset and both set and reset processes are studied. In the first case, (Fig. 6A), the electric field (during the application of $V_B \neq 0$ V during the reset process) contributes to larger conduction through the conductive filament. In second case, (Fig. 6B) although $V_B \neq 0$ V is applied during both

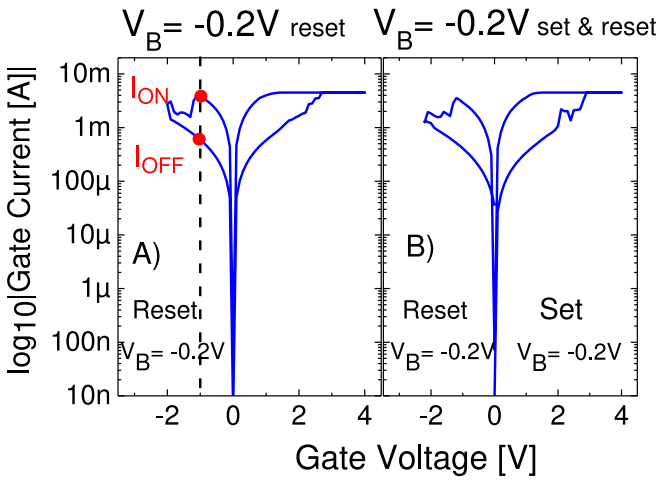

Fig. 6. RS I_G -V_G average curves measured on the same sample when A) V_B = -0.2 V for the reset process only (V_B = 0 during the set), B) V_B = -0.2 V during set and reset process.

set and reset processes consecutively, the electric field generated by the negative voltage (during the reset process) remains insufficient to decrease the conduction through the conductive filament formed during the set process.

4. Conclusions

In summary, this work experimentally studies, on the one hand, the I_D-V_D transistor curves, when the gate dielectric is at the high and low resistance states. The results point out that the transistor performance can be partially recovered after the reset process, by applying appropriate RS voltages and current limit conditions. This demonstrates the feasibility of integrating a memristor and a transistor within a single device also with these FDSOI devices. On the other hand, the back gate voltage influence on the device has been preliminary studied. When a negative back gate voltage is applied during set process the I_{ON}/I_{OFF} ratio increases, which could be related to the impact of the strong transversal electrical field. However, preliminary results indicate no significant effects of this bias on the I_{ON}/I_{OFF} ratio when it is applied during the reset process with $V_B \neq 0$ V or a complete RS cycle with $V_B \neq 0$ V in both set and reset processes. These differences need to be further addressed in future research.

CRediT authorship contribution statement

C. Valdivieso: . **R. Rodriguez:** Writing – original draft, Supervision. **A. Crespo-Yepes:** Resources. **J. Martin-Martinez:** Supervision. **M. Nafria:** Writing – original draft, Supervision.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

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