Solid-State Electronics 230 (2025) 109228

Contents lists available at ScienceDirect

Solid State Electronics

journal homepage: www.elsevier.com/locate/sse

On the role of power dissipation in the Post-BD behavior of FDSOI NanoWire FETs☆

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ARTICLE INFO

Handling Editor: Francisco F. Gamiz

Keywords:
Aging
FDSOI
Nanowire
High-k
Reliability
Dielectric breakdown

ABSTRACT

Dielectric Breakdown, which has been associated with the progressive wear-out of the gate dielectric, has been one of the most detrimental failure mechanisms in CMOS devices. With downscaling, new device architectures and/or materials have been introduced, so, it is necessary to evaluate the BD impact at device (and circuit) level in these new structures. In this work, the dielectric BD and the post-BD behavior in largely scaled FDSOI nanowire transistors with high-k gate dielectric have been characterized, using the energy and the power dissipated by the device under test as key parameters. The experimental results evidence the presence of new detrimental effects for the device's integrity beyond the traditional dielectric BD.

1. Introduction

In CMOS technologies, dielectric breakdown (BD) of the gate oxide has been one of the most important reliability concerns because of its impact on the gate stack conduction, which can lead to the final device failure [1–7] and damage the circuit functionality. [8–10]. During the last decades, BD (i.e., Soft, Progressive and Hard BD [11–13]) has been widely studied in planar bulk MOSFETs with SiO_2 and Hf-based high-k gate dielectrics [4–6,13], also the post BD conduction and the observation of the BD reversibility under specific stress conditions [14–16]. Additionally, Ultimate Nanowire (NW) transistors on Fully Depleted Silicon-On-Insulator (FDSOI) also experience the dielectric BD, with negative consequences on the circuit functionality. However, the impact of the device architecture (i.e., Buried Oxide (BOX) under the active area, channel confinement…), if any, on the BD and post-BD performance of the device have not been comprehensively analysed yet. In this work, the BD and post-BD behaviour of NW FDSOI MOSFETs with high-k gate dielectric have been characterised, using as key parameters the energy and the power dissipated by the device.

2. Device and experimental procedure

The studied devices were nMOS and pMOS FDSOI MOSFET transistors fabricated at CEA-LETI, with high-k Ω-gate (HfSiON/TiN with EOT = 1.3 nm and H_{NW} = 11 nm) and nanowire architecture (NW-FET) [17]. The buried oxide (BOX) thickness is 145 nm. Fig. 1 (left) shows the 3D sketch and the cross-section of a single device. Devices with two different widths were studied: (1) W = 30 nm (1-channel) with lengths ranging from 20 nm to 1000 nm, and (2) W_{eff} = 300 nm (split in 10-channels of W = 30 nm) with two lengths, 20 and 40 nm. Ramped voltage stresses (RVS) were applied to the gate terminal (from 0 V to |10 V|, with the rest of the terminals grounded) to induce the oxide wear out and to provoke the dielectric BD. Approximately, 300 transistors have been measured which allow the statistical analysis of the BD and CD events. But only those devices in which the BD and CD are triggered are used in this study. The applied voltage and the current through the gate were registered during the experiments, together with the sampling time used during the RVS, to calculate the dissipated power and energy before/after the BD.

3. Results and discussion

Fig. 1(right) shows different examples of I_G-V_G curves measured during the RVS. In these devices, after the typical BD-related current increase, a new event can be triggered, observed as a large and sudden current drop (which from now on will be named as CD), always measured at larger voltages than BD. In many cases, the BD and CD events are clearly distinguishable. However, in some cases, CD is

☆ This article is part of a special issue entitled: 'EuroSOI-ULIS 2025' published in Solid State Electronics.

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https://doi.org/10.1016/j.sse.2025.109228

Available online 29 August 2025

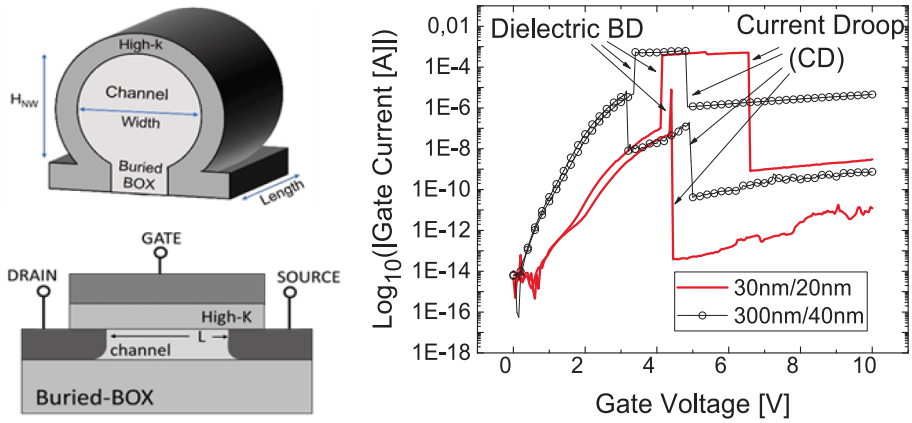

Fig. 1. (left-top) 3D sketch of the Ω-Gate NW FD-SOI transistors (left-bottom) Transistor cross-section [17]. (right) Examples of typical I_G-V_G curves measured during the RVS applied to the gate terminal to provoke the BD in nMOS FDSOI transistors with W/L = 30 nm/20 nm (lines) and W/L = 300 nm/40 nm (circles).

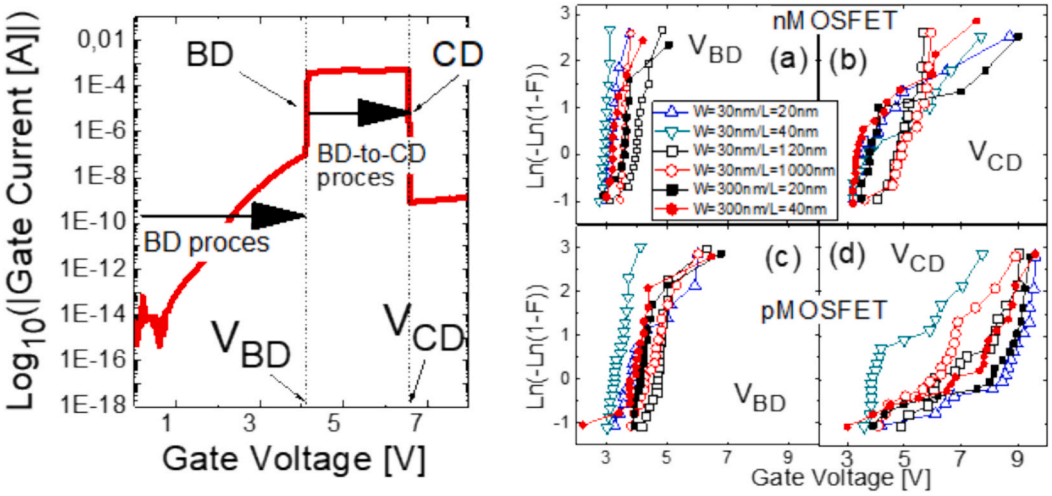

Fig. 2. (left) Definition of the parameters used in this work. (right) Weibull distributions of V_{BD} (a and c), and V_{CD} (b and d), for nMOS (top) and pMOS transistors (bottom) of different lengths and 1-channel (W = 30 nm, open symbols) and10-channel (W = 300 nm, solid symbols) architectures.

immediately triggered after the BD, so that the equipment (Keithley 4200) is not able to register the BD, and only the CD is measured. Such behaviour was observed in all the studied devices, nMOS or pMOS, and single or 10-channel devices, though with a large dispersion in the associated voltages and currents. BD of the gate oxide has been extensively studied in bulk devices, and no relevant differences could be expected in these FDSOI transistors. However, CD events, since unique of these technologies, must be further investigated.

Fig. 2(left) shows the definition of the BD and CD related parameters, such as V_{BD}/V_{CD}, the BD process voltage region (i.e. from 0 V to V_{BD}) and the BD-to-CD process region (from V_{BD} to V_{CD}). Fig. 2(right) shows the V_{BD} and V_{CD} statistical distributions, for nMOS and pMOS with different areas. As expected, the V_{BD} distributions depend on the device area and device type (n-type or p-type transistor), while those of V_{CD} do not, due to the local nature of the post-BD conduction, for all device types. In addition, V_{CD} distributions are broader than those of V_{BD} because of the random nature of the conductive filament after the BD that is controlling the device conductivity. Since energy dissipation plays a key role in the gate BD and self-heating is a critical issue in channel-confined technologies [18], the energy-to-BD (i.e., from 0 V-to-V_{BD}), E_{BD}, and the energy-to-CD (from V_{BD}-to-V_{CD}), E_{CD}, together with the power dissipated at the moment that BD and CD are triggered (i.e., at V_{BD} and V_{CD}), have been computed and statistically analyzed to get more insights on the origin of the CD and on the conditions that trigger this failure mode. Note that only devices on which both BD and CD are clearly measured (around 140 out of the 300) are included in the analysis (Figs. 3, 4 and 5). Fig. 3 shows the energy- to-BD (Fig. 3 a and b) and this energy normalized to the device area (Fig. 3 c and d). Note that, since the number of devices (20) per type and dimensions is the same, the number of points plotted in the distributions indicates the probability of the occurrence of the BD and CD events. As observed in Fig. 3, E_{BD} is area dependent for both device types (Fig. 3 a and b) but larger for the nMOS. Interestingly, the normalized distributions have large slopes (i.e. low dispersion) and, independently of the device type or architecture, the energy values are concentrated in an energy decade (Fig. 3 c and d). Therefore, as for bulk devices, the dissipated energy also plays a key role in the BD of these FDSOI technologies.

In contrast to the BD, the E_{CD} distributions of the BD-to-CD process (Fig. 4) are not area dependent, as reasonably expected, because of the extremely local nature of the BD phenomenon. The E_{CD} values are larger for the nMOS transistors as compared to the pMOS transistors because the energy values exhibit larger dispersion. The smaller slopes of E_{CD} suggest that this parameter is not as well-suited to characterize the CD event as it is for the BD. Therefore, power consumption at the CD event, P_{CD}, (Fig. 5) has been evaluated, for both nMOS and pMOS transistors (Fig. 5 a and b, respectively). As can be observed, for both device types, the distributions of P_{CD} are also independent of the device area. However, some differences have been observed in nMOS and pMOS devices.

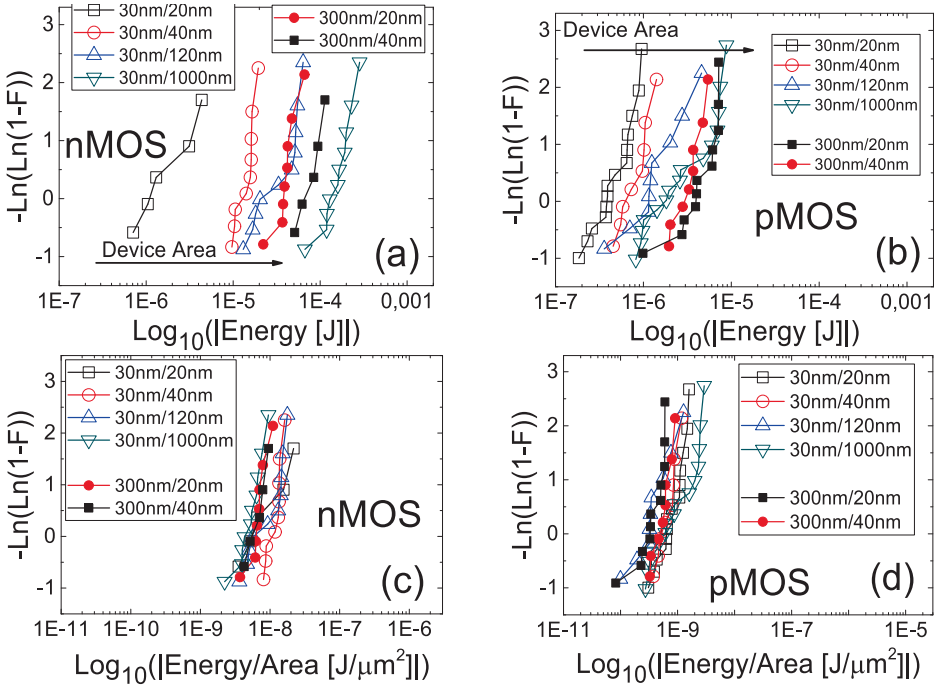

Fig. 3. E_{BD} (top) and E_{BD} normalized to device area (bottom) in nMOS (a and c) and pMOS (b and d) transistors.

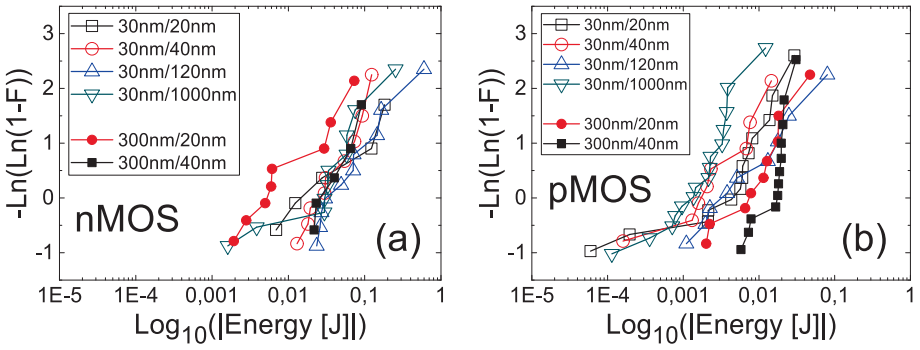

Fig. 4. Energy-to-CD (i.e. from V_{BD} to V_{CD}) in nMOS (a) and pMOS (b) FDSOI transistors.

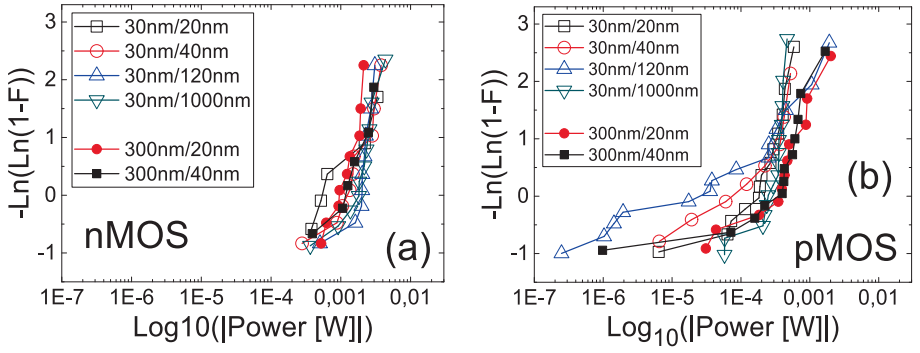

Fig. 5. Power dissipated at the CD event (i.e.,at V_{CD}) for nMOS (a) and pMOS (b) transistors.

For the nMOS transistors, the values of P_{CD} are larger (with a maximum of ~ 3mW, compared to ~ 1mW for the pMOS) and exhibit low dispersion with almost monomodal distributions (as observed for E_{BD} in Fig. 3). However, for the pMOS, bimodal distributions seem to be observed, suggesting that two mechanisms can lead to the CD event. Note, however, that the mode observed at larger P_{CD} appears to be like that observed in the nMOS, suggesting the presence of an intrinsic CD mode (in nMOS and pMOS) and an extrinsic mode (mostly observed in pMOS). Therefore, opposite to the mechanism that controls the BD (i.e. wear out), which is an area dependent and cumulative process related to the dissipated energy in the device (Fig. 3), the CD is driven by a local and instantaneous process, probably linked to the power dissipation in

the device after the BD.

4. Conclusions

The BD and CD phenomenology in high-K Ω-shape NW FD-SOI transistors have been statistically analyzed, using the power consumption at BD and CD and the dissipated energy to BD and to CD as parameters. The results show that, as for bulk technologies, BD is a cumulative process that depends on the device area, associated with the oxide wear out consequence of the energy dissipation. However, the CD, solely observed in these FDSOI technologies, is driven by the local conduction of the BD path and triggered when a certain amount of power has been dissipated, probably related to the power dissipation capability of the Buried Oxide (BOX).

CRediT authorship contribution statement

R. Goyal: Writing – review & editing, Writing – original draft, Validation, Supervision, Methodology. **A. Crespo-Yepes:** Writing – review & editing, Writing – original draft, Validation, Supervision, Methodology. **M. Porti:** Writing – original draft. **R. Rodriguez:** Writing – review & editing, Writing – original draft, Validation, Supervision, Methodology. **M. Nafria:** Writing – original draft.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgments

This work was supported by Grant PID2022-136949OB-C22 funded by MCIN/AEI/10.13039/501100011033/ FEDER, UE, and 2021-SGR-00199. EU ASCENT project is acknowledged for sample provision.

Data availability

No data was used for the research described in the article.

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