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Field-Induced Phase Transitions in Cuprate Superconductors for Cryogenic in-Memory Computing

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Energy-efficient cryogenic memory systems play a critical role in a wide spectrum of applications focused on ultra-energy-efficient information and communication technologies, such as quantum computing or superconducting electronics. Neuromorphic systems, known for their superior energy efficiency, have emerged as a promising approach for in-memory computing. Specifically, strongly correlated oxides that exhibit Mott metal-insulator transitions through field-induced oxygen movement are of great interest for analog memory and neuromorphic computing. Yet, optimizing their performance at low temperatures may prove challenging due to their reliance on ionic motion. In this study, superconducting structures composed of strongly correlated $YBa_2Cu_3O_{7-x}$ (YBCO) combined with ferromagnetic $La_{0.7}Sr_{0.3}MnO_3$ (LSMO) are investigated to obtain non-volatile multilevel memristive switching effects with high performance at cryogenic temperatures. This research reveals the presence of two competing switching mechanisms, which are attributed to the movement of oxygen vacancies and electric carriers within these structures. It is determined that a phase transition induced by the movement of holes is the primary factor influencing the switching dynamics at low temperatures. Additionally, a physics-based compact model is proposed that accurately replicates the experimental findings and provides a tool for circuit-level design.

1. Introduction

The constantly growing demand for data processing and transfer leads today's society into the Age of Big Data.[1] Until now, improvements in storage and computing performance have relied on advances in semiconductor technology. However, the scalability and power consumption of current devices based on complementary metal oxide semiconductors (CMOS) are reaching their physical limits. Moore's law is slowing down, primarily due to the power dissipation related to standby leakage currents in complex chips.[2] Moreover, current computing systems are inherently limited in energy efficiency and data bandwidth by the physical separation between memory and processing units. This is known as von Neumann's bottleneck.[3] Therefore, new unconventional computing architectures, able to boost data management while reducing power, are required to accelerate computational performance in terms of time and energy.[4] Cryogenic Electronics, including cryogenic CMOS, superconductor electronics, and quantum information processing, has been recognized as one of the International Focus Teams in the IRDS roadmap.[5] These innovative technologies present compelling alternatives to traditional CMOS, showcasing a range of novel functionalities and applications. They promise high performance, large system energy efficiency, or low power dissipation at cryogenic temperatures. This makes them a critical area of research for achieving breakthroughs in high-performance computing and cutting-edge technology applications. Cryogenic semiconductor electronics may offer a viable approach to sustain Moore's Law, meeting high-performance computing demands by reducing operating voltage with no impact on operating speed.[6] Rapid Single-Flux Quantum (RSFQ) superconducting electronics can achieve performance enhancements, with efficiency levels up to 100 times greater than traditional semiconductor-based technologies.[7] Additionally, integrating these technologies with lossless interconnections could be highly effective. However, the lack of fast, low-power, high-density cryogenic memory compatible with RSFQ circuits limits the progress of practical and reliable systems.[8] Cryogenic memories are also essential for advancing quantum computers, potentially addressing critical societal challenges that

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classical computers cannot solve within a reasonable timeframe. While various technologies can be used to implement the fundamental units of a quantum computer, superconducting qubits are particularly noteworthy due to their fast gate times and maturity in design.[9] To create the necessary conditions for quantum computing, it is crucial to keep all qubits—regardless of whether they are superconducting or not—at cryogenic temperatures. This environment is vital for minimising thermal noise and preserving quantum coherence.[10,11] To effectively utilize the advanced capabilities of cryogenic electronics, it is essential that compatible memory systems, logic circuits, and interconnects operate optimally at the extremely low temperatures found in a dilution refrigerator. Alternatively, these components can also be designed to function efficiently at higher temperatures, such as 77K. While cryogenic versions of non-superconducting memories provide large storage capacities, they face challenges in terms of speed and compatibility with RSFQ and qubit superconducting circuits. Conversely, superconducting memories that use Josephson junctions work well with superconducting electronics, but they lack scalability.[11] Thus, the advancement of high-performance, multi-level, and scalable memory devices based on superconducting materials—capable of seamless integration with superconducting interconnections—plays a pivotal role in the advancement of superconducting electronics and quantum computing, thereby having a significant potential impact on society. Strongly correlated oxides present an extremely rich phase diagram with various forms of ordered phases and collective fluctuations originating from the interplay of charge, spin, orbital, and lattice degrees of freedom.[12] Particularly interesting is the phase diagram of strongly correlated High-Temperature superconducting (HTS) cuprates with multiple quantum phases with different forms of charge, spin order, and quasiparticle states that compete with superconductivity.[13] Transitions between different quantum phases, with dramatically different physical properties, may be induced through external parameters such as composition, strain, disorder, temperature, pressure, light, magnetic or electric fields.[14–16] The ability of Mott memristors to continuously adjust electrical resistance, modulate time-dependent resistance, and exhibit high nonlinearity with the electric field makes them an effective way to create synapses at a device level.[17,18] Furthermore, depending on the balance between the driving force that injects or removes carriers to the system and the kinetic barrier needed to drive the system to the initial state, both non-volatile and volatile behaviors can be induced, enabling the implementation of synaptic and neuron functionalities in a single material.[17,19] It is important to highlight that the Metal-Insulator Transition (MIT) can happen on ultrafast timescales.[17] For instance, it has been reported that MIT can be induced in vanadium dioxide on the subpicosecond scale.[20] Given that the mechanisms of Mott MIT are expected to be "ultrafast," many studies have attempted to integrate Mott materials into ultrafast switches, Mott transistors, optical detectors, solid-state sensors, and neuromorphic elements.[21,22] Neuromorphic computing, inspired by the brain and based on analog compute-in-memory approaches, presents a promising alternative for energy-efficient computation. This method reduces the energy-intensive data transfer between memory and processors.[23] A key device in this context is the memristor, which was developed as a solid-state device in ref. [24]. Memristors are distinguished by their hysteretic, pinched current–voltage characteristics and possess at least two non-volatile resistance states. Transitions between the Low Resistance State (LRS) and the High-Resistance State (HRS) and vice versa are referred to as the RESET and SET processes. For neuromorphic applications, at least one of these transitions must be gradual to enable the programming of intermediate resistance states. Emerging memristive technologies for in-memory computing are based on memristive memory elements with storage and computing principles relying on the physics of the active materials, such as ion migration, phase change transitions, spin-dependent tunnel magnetoresistance, or ferroelectricity.[25–27] However, current neuromorphic systems still fall short in terms of power efficiency, computational strength, and compactness compared to the impressive capabilities of the human brain.[28] Therefore, there is a critical need for innovative platforms to deliver superior energy efficiency, paving the way for the next generation of computing technologies. The primary source of power consumption in neuromorphic systems is the extensive interconnectivity between neurons and synaptic networks. Superconducting cryogenic neuromorphic computing shows potential in addressing the interconnect loss issues faced by conventional device platforms, which could lead to the development of ultra-compact, brain-like neuromorphic devices. Additionally, a cryogenic environment may significantly reduce noise, which can positively impact the overall performance of the neuromorphic system.[29] In this context, Field-induced MIT in HTS cuprates offers an opportunity to leverage the advantages of Mott memory and neuromorphic devices, along with the exceptional properties of loss-less superconducting materials.

Strategies for modulating carrier concentration in cuprate superconductors via electrical field gating include pure electrostatic charge doping or electrochemical oxygen doping.[15,16] Field-induced oxygen modulation of $YBa_2Cu_3O_{7-x}$ (YBCO) HTS can yield multiple non-volatile states through oxygen vacancy migration induced by applying gate voltages using direct metallic gates,[30–32] via interfacial redox reactions facilitated by intermediate buffer layers,[33] or through electromigration effects.[28,34,35] However, mechanisms relying on ionic motion may be complex to operate at low temperatures. An alternative approach involves electrostatic gating techniques to modulate carrier concentration without altering the crystal structure.[36,37] Several successful studies have demonstrated the efficacy of electrostatic doping in cuprate superconductors using liquid electrolytes or ferroelectric gates.[15,37–39] Ionic liquid gating enables precise carrier modulation, yet the challenge lies in achieving non-volatile states and integrating this process into devices. With ferroelectric gates, controlling non-volatile carrier density modulation is done through ferroelectric polarization, but it is difficult to achieve precise tuning for multilevel states.

Here, we demonstrate the coexistence of two processes, namely electrochemical oxygen doping and electrostatic carrier modulation in a microsized functional device. The structure consists of a bilayer made of a strongly correlated high-temperature superconductor, YBCO, which serves as the active layer, and a half-metallic ferromagnetic material, $La_{0.7}Sr_{0.3}MnO_3$ (LSMO), which acts as a passive bottom electrode. These two mechanisms can be clearly distinguished as they exhibit opposite switching po-

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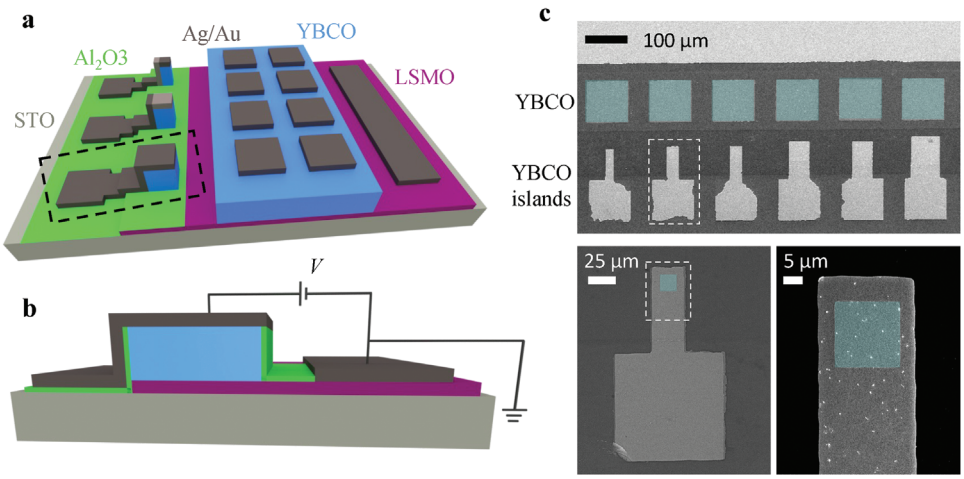

Figure 1. a) Schematic layout of the devices, illustrating several YBCO islands (left) and unpatterned devices (right). An enlarged cross-section view of the devices based on YBCO islands (indicated with black dashed rectangle in a)) is provided in b). The top contact of the YBCO is biased, while the bottom contact is grounded. c) False-color Scanning Electron Microscopy image of several YBCO islands, unpatterned devices and an enlarged image of one of the YBCO island devices. The white dashed lines indicate the zoomed region.

larities. We reveal that the formation of an oxygen-depleted layer below the top electrode may be controlled through oxygen migration at room temperature. This non-superconducting layer initiates a gradient of holes within the material, offering the potential to fine-tune it through electrostatic effects at low temperatures, thereby achieving stability across various resistance states within the YBCO phase diagram. The combination of both mechanisms allows for optimizing the switching performance for cryogenic analog memory and neuromorphic computing applications. In addition, the memristor response to arbitrary input signals was simulated using a physics-based compact model to facilitate neuromorphic circuit evaluation and design.

2. Results and Discussion

The structures analyzed throughout the manuscript consist of a superconducting YBCO film, with thicknesses of 50 and 100 nm, grown on $SrTiO_3$ (STO) substrates, buffered with a 40 nm thick, ferromagnetic LSMO layer, serving as a bottom electrode and 100 nm thick Silver or Gold as top electrodes. Superconducting and ferromagnetic properties of YBCO and LSMO, respectively, were measured by SQUID magnetometry, shown and explained in more detail in the Supporting Information (Figure S1). Two different types of structures were fabricated: unpatterned YBCO films with top electrodes of 100 × 100 µm^2 and 150 × 150 µm^2, and patterned square-shaped YBCO islands of varying lateral sizes ranging from 10 × 10 to 100 × 100 µm^2. YBCO islands were coated with an insulating layer of Al_2O_3 of 30 nm to avoid short circuits between the top and the bottom electrodes. **Figure** 1a shows a schematic drawing of the device layout, while Figure 1b illustrates a more detailed cross-section view of the patterned devices. For further details regarding the fabrication, see Experimental Section. Figure 1c shows scanning electron microscope (SEM) images of a larger part of the sample and one of the devices based on a YBCO island.

2.1. Competing Switching Mechanisms at Room Temperature

The resistive switching performance of YBCO devices is evaluated by applying a series of writing voltage pulses, V_{write}, following a specific sequence: $V^+_{min} \rightarrow V^+_{max} \rightarrow V^+_{min}$, $V^-_{min} \rightarrow V^-_{max} \rightarrow V^-_{min}$. Each writing pulse was alternated with a low-voltage reading pulse of amplitude, V_{read}. The value of V_{read} is selected to be small enough to prevent any change in the internal state variable, ensuring no resistance variation. The pulse widths, which can be adjusted independently, are t_{write} for the writing pulse and t_{read} for the reading pulse, respectively. Each completed cycle comprises 200 writing voltages. To study the reproducibility of the resistance hysteresis, the cycle above can be repeated for a specific number of times, denoted as n_c. **Figure** 2a illustrates this method schematically. As the parameters used for the measurements vary throughout the manuscript, they are specified in the figure captions. The memristive characteristics of the device may be evaluated by plotting the resistance obtained by the reading voltage, R_{read}, as a function of the applied voltage, V_{write}.

Figure 2d shows the results obtained by applying this method to an unpatterned YBCO device with silver electrodes of size 150 × 150 µm^2 at room temperature. Starting from a low-resistance state (LRS), the device can switch to a high-resistance state (HRS-1) when negative voltages are applied (1). Resistance changes occur when the writing voltage exceeds approximately –5 V, and the HRS stabilizes around –8 V. During a subsequent positive sweep from 0 to 7 V (2), the sample returns to the LRS, defining a stable hysteresis loop, shown in grey, with a clockwise polarity. In addition to this major loop, a second stable loop with opposite polarity, shown in purple, can be obtained. In this case, starting from the HRS-1, by applying a sweep toward +2 V (3), below the threshold voltage required to switch the device back to the LRS ($V_{th} \approx +2.5$ V), the resistance increases by approximately 30 Ω (HRS-2). This increase can be reversibly modulated by sweeping the voltage to –5 V (4). The coexistence of a reproducible major (grey) and minor loop (purple) suggests that two distinct switching mechanisms are present in the device. This

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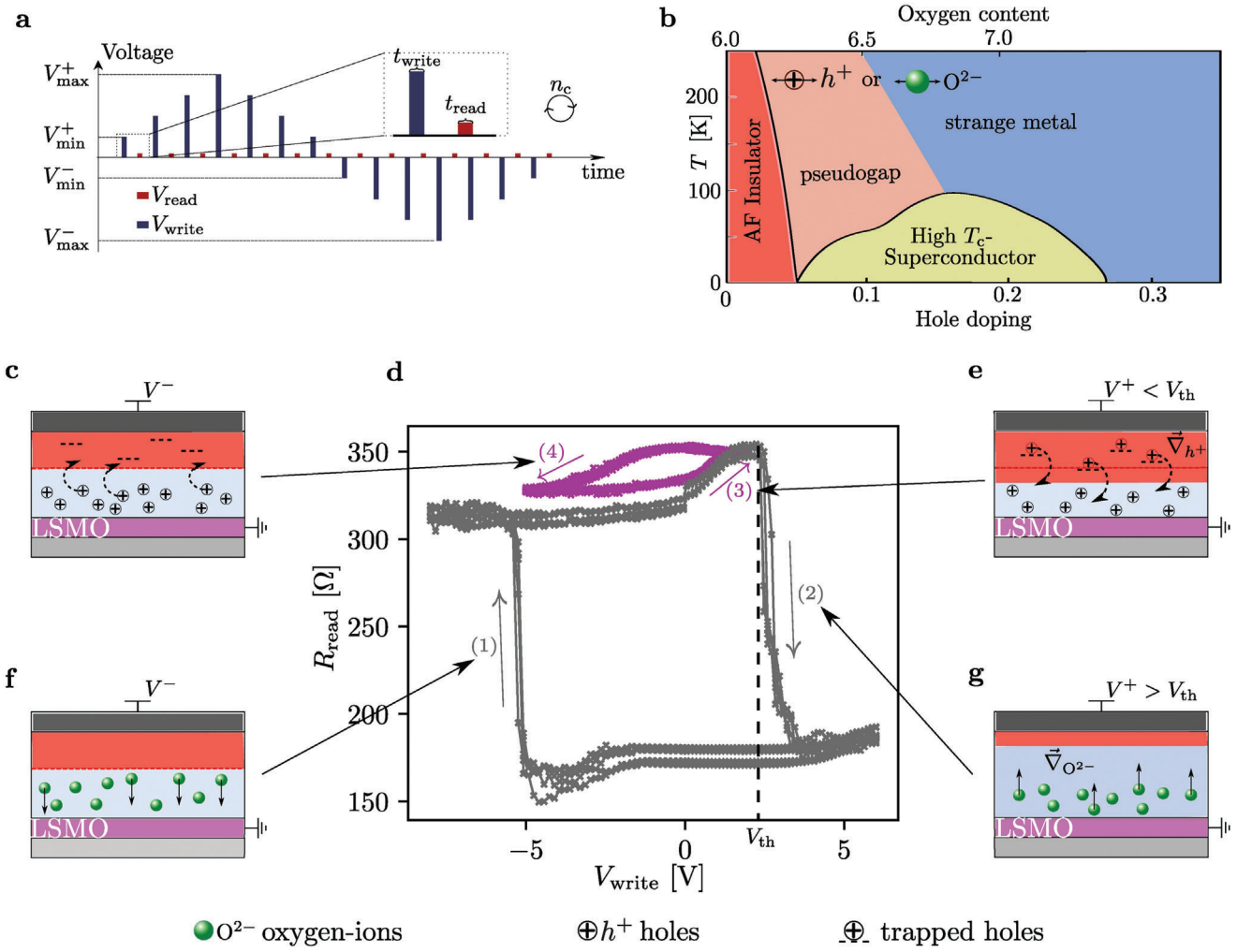

Figure 2. a) Schematic representation of the pulse train used to obtain the resistance hysteresis loops. b) Schematic temperature-doping phase diagram of YBCO with the transition through different phases due to hole, h^+, and oxygen O^{2-} motion indicated with arrows. d) Resistance hysteresis measured at 300 K for an unpatterned 50 nm thick device with a top silver electrode of 150 × 150 μm^2. The major loop, indicated in grey with the transitions (1) and (2) and the minor loop, illustrated in purple with the transitions (3) and (4), occur at opposite polarities as indicated by the direction of the arrows. Data was obtained setting t_{write} = 1 ms, t_{read} = 5 ms, V_{read} = 0.2 V, $V^+_{min} = -V^-_{min}$ = 0.05 V and n_c = 5 for both loops. The maximum voltages for the minor loop were V^-_{max} = −5 V and V^+_{max} = 2 V and V^+_{max} = 7 V and V^-_{max} = −8 V for the major loop. f,g and c,e) Simplified schematics of the switching mechanisms responsible for the transitions (1), (2) and (3), (4) for the major and minor loops depicted in (d), respectively. The proposed mechanism for transitions (1) and (2) involves oxygen movement and the manipulation of an oxygen gradient, $\vec{\nabla}_{O^{2-}}$, while (3) and (4) are driven by electrostatic hole motion and the manipulation of a hole gradient, $\vec{\nabla}_{h^+}$.

phenomenon of coexisting mechanisms in a switching device has been observed in Fe-doped $SrTiO_3$ thin films, where the two loops were attributed to the formation of a filament and a homogeneous change distributed over a large area of the electrode.[40] Another example of such behavior was demonstrated in devices made from ferroelectric $BaTiO_3$ with an LSMO bottom electrode, where the effect was explained through independent control of ferroelectric and oxygen vacancy switching.[41] Furthermore, resistive switching loops with inverse polarity may occur due to resistance changes at the top and bottom interfaces.[42] However, this effect was ruled out using a device with reference electrodes (see Supporting Information S2). With these reference devices, we determined that both switching loops are related to resistance changes taking place close to the top electrode. We also measured the current–voltage (I–V) characteristics in both the LRS and the HRS at low voltages to prevent any switching and at various temperatures (see Supporting Information S3). The symmetry observed in the I–V characteristics indicates that there is no modulation of a Schottky barrier, suggesting a bulk-limited conduction mechanism. Therefore, both the top and bottom electrodes may be considered as ideal contacts able to supply or remove holes as needed by the external circuit.

Based on the argument that the switching effect associated with both loops occurs below the top electrode, we propose a physical mechanism to explain our experimental findings.

Figure 2b illustrates the phase diagram of YBCO, showing various electronic phases that depend on temperature and oxygen or hole doping, which supports our physical explanation of the

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switching mechanisms. The crystal structure of YBCO comprises alternating CuO-chains and CuO_2-planes. The CuO-chains act as charge reservoirs, while the CuO_2-planes are responsible for the high-temperature superconductivity. The hole doping of the material can be adjusted by either removing electrons from the copper-oxygen planes, i.e., directly adding holes through an electrostatic doping process (bottom axis) or by altering the oxygen stoichiometry of the CuO-chains, from $YBa_2Cu_3O_6$ to $YBa_2Cu_3O_7$ (top axis), which creates holes in the CuO_2-planes using electrochemical doping. Either mechanism for hole doping results in a suppression of the antiferromagnetic order and leads to a Mott phase transition from an antiferromagnetic-insulating state toward a metallic or, below a critical temperature T_c, to a superconducting state.[13,43] Therefore, the forced movement of oxygen ions or holes under an external electric field may stabilize different phases across the phase diagram and, thus, change the resistive state of the devices. According to this, the major loop follows the expected polarity for ionic oxygen diffusion. At negative polarity, negatively charged oxygen ions, O^{2-}, move toward the bottom electrode, creating an oxygen-depleted layer at the top interface, which switches the device to the HRS-1 (Figure 2f). Thus, we establish a gradient of oxygen, $\vec{\nabla}_{O^{2-}}$, and associated holes, $\vec{\nabla}_{h^+}$, along the sample thickness. At positive voltages above a certain threshold, oxygen moves back to the electrode, switching the device to the LRS (Figure 2g). Similarly, to the established gradient of oxygen ions, a gradient of holes may be induced through a pure electrostatic effect. In this case, since holes are positively charged, they will move toward the bottom electrode at positive polarity, creating an enlarged region of hole-depleted YBCO at the top electrode and switching the system to HRS-2 (Figure 2e). At negative polarity, holes are injected back, returning the system to HRS-1 (Figure 2d). Based on the movement of positively charged holes and negatively charged oxygen ions, these two mechanisms provide a natural explanation for the opposite polarities of the major and the minor loops. It is worth pointing out that the major hysteresis loop, associated with oxygen doping, is better observed in the samples with silver electrodes, as silver may catalytically activate surface oxygen exchange.[44] Field-induced electrochemical oxygen doping has been widely studied in YBCO films,[30–33] holding significant promise for the development of flexible multiterminal transistor-like devices with neuromorphic functionalities. Additionally, it allows to locally modulate the thickness of the oxygen-depleted layer below the gate with the applied voltage.[31] However, although field-induced oxygen doping works well at high temperatures, the switching performance, reproducibility and extension of the oxygen-depleted region are reduced at low temperatures in agreement with low oxygen mobility.[31] Thus, our studies are focused on the minor loop to explore the device behavior and performance at cryogenic temperatures. In the following sections, we will refer to the initial low-resistance state of the minor loop (HRS-1) as LRS and the HRS-2 obtained after positive voltage pulses as HRS.

2.2. Switching Performance at Cryogenic Temperatures

To further understand the switching mechanism of the minor loop, temperature and area dependences of the resistance hysteresis loops are studied. **Figure 3a** shows the evolution of the hysteresis loops obtained at different temperatures during the cooldown of an unpatterned device from 300 to 50 K. It is observed that the resistive switching prevails far below the superconducting transition temperature of the YBCO thin film of $T_c \approx$ 90 K and that the hysteresis is strongly increased by decreasing the temperature. This trend can be better elucidated by plotting the dependence of the HRS and the LRS as a function of the temperature in Figure 3b, where a resistance change from a metallic (LRS) to an insulating (HRS) behavior is observed. Additionally, it is relevant to remark that low voltages are required to induce the switching event (~1 V) exhibiting minimal dependence on temperature. These characteristics argue against a thermally activated switching mechanism such as ion migration and further point toward field-induced hole motion. Interestingly, the temperature dependence of hysteresis loops varies among devices with different initial high resistance states (HRS), as shown in Figure S4 (Supporting Information).

This variation highlights the significance of the oxygen-depleted layer beneath the electrode, which determines the initial HRS, and plays a crucial role in facilitating the field-induced movement of holes and associated non-volatile MIT at low temperatures. These results align with findings reported for YBCO/Nb:STO,[45] where the authors attributed the non-volatile switching mechanism to charge trapping and de-trapping near the interface. They suggested that oxygen vacancies within the chains of underdoped films might promote switching by increasing the number of charge-trapping centres. Additionally, it is shown in ref. [46] that the switching mechanisms in Pt/Nb:STO junctions involve charge trapping within a defected layer at the interface. Stable self-trapping of holes in strongly correlated oxides, such as manganites and cuprates, was also observed in ref. [47], supported by the formation of polaron states. It aligns with the observation that polarons, lattice distortions, and electron correlations play a significant role in facilitating phase transition processes in strongly correlated systems.[48] In the context of polaron-mediated MIT, the introduction of excess carriers results in their redistribution within the lattice, leading to self-trapping due to the formation of a polaron state, a quantum quasiparticle arising from the interaction between excess charges and the crystal structure. Polaron correlations may play a crucial role in stabilizing charges within the system, which could contribute to the development of non-volatile electronic data storage in correlated electron devices.[49] Our results, which are supported by the previously discussed findings, can be explained by considering that the oxygen-deficient layer formed at the top YBCO interface allows for hole trapping and de-trapping, leading to a non-volatile electrostatic transition. This paves the way for engineering resistive switching based on intentional modifications of the oxygen concentration within the oxygen-depleted layer. Such modifications would enable complete control over the device's volatility and allow for further investigation of the role of polarons in the metal-insulator transition of cuprate superconductors. Extensive research has demonstrated that heterojunction topologies possess significant potential to enhance the performance of devices in resistive switching applications while simultaneously introducing novel functionalities. For instance, it has been suggested that conductive pathways can be localized in filamentary devices.[50] Additionally, precise control over oxygen dynamics at the contact interface provides

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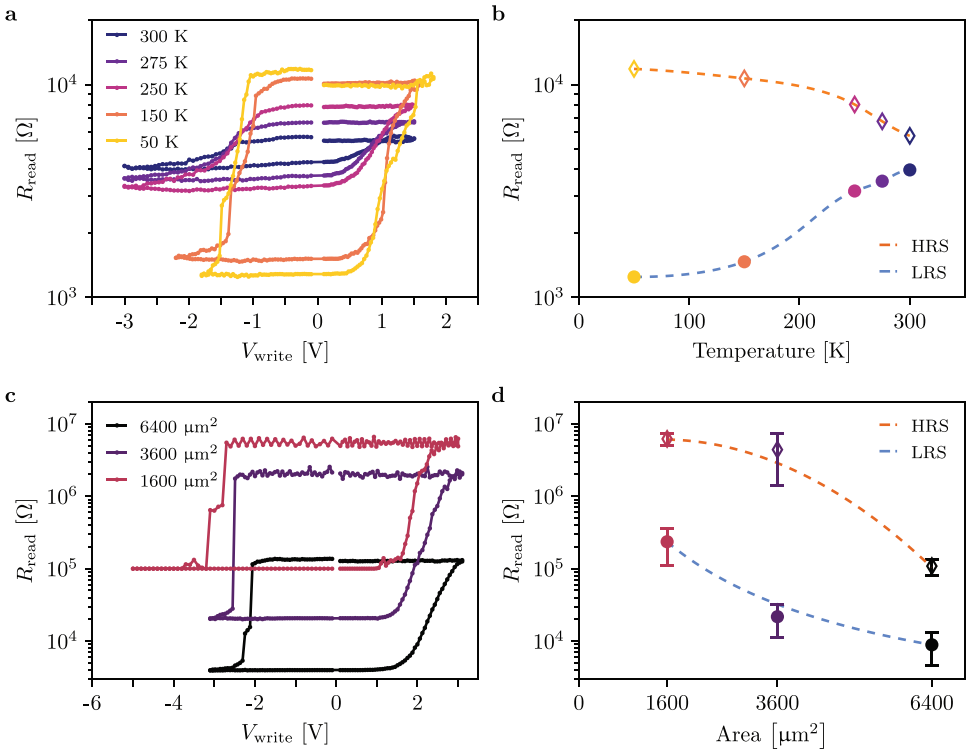

Figure 3. a) Resistance hysteresis loops obtained at different temperatures for a 50 nm thick unpatterned device with 100 × 100 μm² gold electrodes. Data were obtained setting $t_{write} = 1$ ms, $t_{read} = 1$ ms, $V_{read} = 0.2$ V, $V^{+}_{min} = -V^{-}_{min} = 0.1$ V and $n_c = 5$ for all loops. To assure saturation of the hysteresis, the voltages V^{+}_{max} and V^{-}_{max}, were varied throughout the measurements. b) Temperature dependence of the resistances in the HRS and LRS obtained with the loops shown in a). Dashed lines are guides to the eye. The color code a) is kept for the symbols. c) Area dependence on the resistance hysteresis loops obtained for different patterned devices with gold electrodes and a thickness of YBCO of 100 nm at 77 K. During the measurement the parameters were set to $t_{write} = 0.3$ ms, $t_{read} = 0.3$ ms, $V_{read} = -1$ V, $V^{+}_{min} = -V^{-}_{min} = 0.1$ V and $n_c > 5$ for all loops. The maximum and minimum voltage of the sweep are adjusted to obtain saturation of the resistance, and only one cycle is shown for clarity. d) Area dependence of the LRS and HRS. The error bars are given by the standard deviation obtained from the measurements of three different devices, while the markers show the average LRS (circles) and HRS (diamonds).

a solid foundation for integrating signals from multiple inputs, which aids in achieving realistic synaptic functions.[51] Specifically, the controlled migration of oxygen vacancies can not only alter the material's resistance but also improve its photoresponse, thereby enabling the development of photomemristors with synaptic functionalities,[50] or promote light-induced synaptic plasticity.[52]

Figure 3c shows the hysteresis loops measured at 77 K on YBCO islands of different sizes. As illustrated in Figure 3d, both LRS and HRS are inversely proportional to the cell area excluding effects of filamentary switching.[53] Large switching ratios are obtained for micrometric-size devices, demonstrating the possible device miniaturization and implementation in electronic circuits. To roughly quantify the electric field required to produce the minor and major hysteresis loops, we have used $E = V/t$, where V is the applied voltage and t is the thickness of the switching device. For the major loop, assuming a voltage of $V = 5$ V and a film thickness of $t = 50$ nm (Figure 2d) we obtain an average electric field of $E = 10^6$ V cm^{-1}, which is consistent with the expected electric field for memristive devices based on ionic motion.[54] In this case, the local environment, initial oxygen doping, crystal orientation, and defects significantly influence the activation energy for oxygen ions in YBCO. This activation energy can range from 0.5 to 1 eV, and may even be higher in the optimally doped state.[35] In the minor loop, the electric field required to induce switching is significantly lower. Using the values of $V = 1$ V and $t = 50$ nm (Figure 3a), or $V = 2$ V and $t = 100$ nm (Figure 3c), we can calculate an electric field of $E = 2 \times 10^5$ V cm^{-1}. This value is independent of temperature and may be associated with the energy needed to induce an electrostatic-driven metal-insulating transition. The stability of the resistance states was evaluated by conducting retention tests on one of the devices at two different temperatures: 150 and 77 K. The results are presented in the Supporting Information S5. Both the LRS and HRS exhibited good retention times at both temperatures, although, at 150 K, we observed a slight drift in the LRS toward higher resistance values. In contrast, the LRS remained stable throughout the entire measurement period at 77 K. Thus, we conclude that cryogenic temperatures are more favourable for the stable operation of our devices.

We demonstrated the ability to create reproducible reversible hysteresis loops with high HRS/LRS ratios at cryogenic temperatures, as depicted in Figure 3c. In the following, we explore the potential for generating stable, non-volatile, multi-level analog states, which are essential for the successful implementation of neuromorphic functionalities and high-capacity, non-volatile

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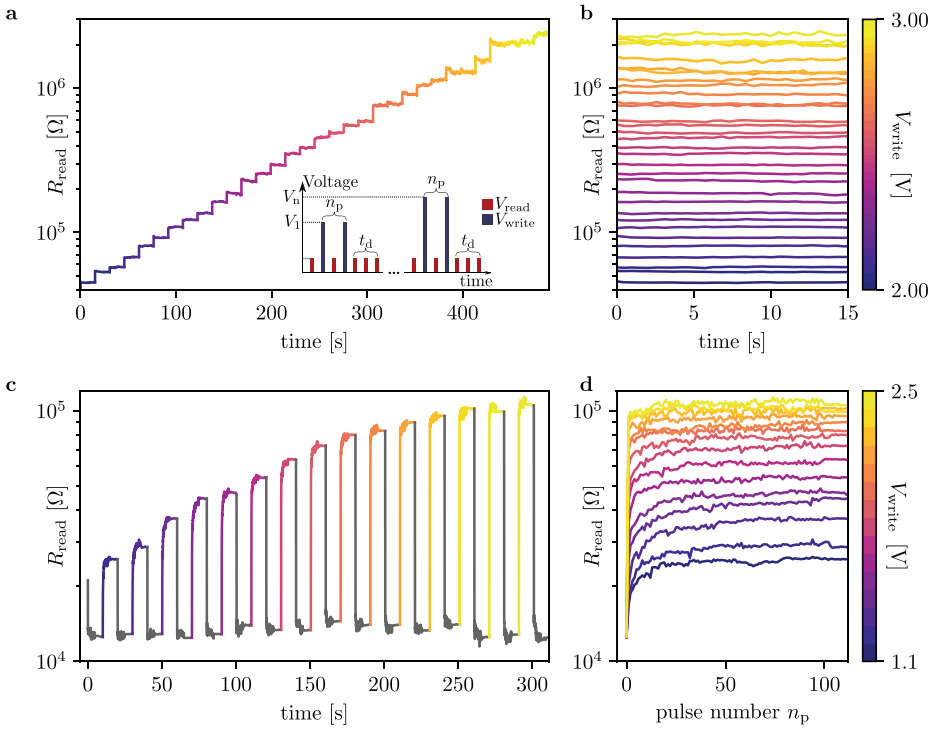

Figure 4. a) Multiple resistance states stabilized at 77K by applying voltage pulse trains of different intensities, as schematically shown in the inset using the parameters $t_{write} = t_{read} = 0.3$ ms, $t_d = 15$s and $n_p = 1$. The voltage amplitude V_{write} was steadily increased from 2 to 3 V in 32 steps, indicated by the color bar in b). b) Evolution of the reading resistance states with time. c) Alternating depression and potentiation cycles obtained with $t_{write} = t_{read} = 0.3$ ms, $t_d = 5$s and $n_p = 100$. To guarantee comparable initial conditions, the potentiation voltage is kept constant at −2.6 V, ensuring the device saturation at the LRS after each depression cycle. Potentiation cycles are illustrated in grey. The depression voltages are increased continuously from 1.1 to 2.5 V in 15 steps, represented by the color bar in d). d) Detail of the evolution of the reading voltage shown in c) as a function of the pulse number. The data shown in a,b) was measured on a YBCO-island with size 60 × 60 μm^2, while the data shown in c,d) was obtained from a device with size 80 × 80 μm^2.

memory devices.[25,55] Measurements were performed at 77K by applying several writing pulses n_p, with a given duration, t_{write}, variable amplitude, $V_{write} = V_1 ... V_n$ and polarity. In this way, different potentiation and depression cycles can be obtained. In between these potentiation and depression cycles, the resistance is measured at V_{read} during a given decay time, t_d, to assure stability of the induced resistive state. The inset in **Figure** 4a provides a general scheme of the pulse train.

Figure 4a, shows the evolution of the resistance obtained for a device initially in the LRS, after applying consecutive voltage pulses with positive t_{write}, $n_p = 1$ and $t_{write} = 0.3$ ms, followed by a reading period of 15 s. Up to 32 non-volatile stable states with exponentially increasing resistances from 10^4 Ω to 10^6 Ω are induced in a single device by linearly increasing the writing voltage from 2 to 3 V, and without the need for any special algorithm. To emphasize the stability of the resistive states, the measured R_{read} during the reading period of consecutive cycles is plotted with an initial time of 0 s in Figure 4b. Complementing the previous experiment depicted in Figure 4c, we present the response of the device to alternating potentiation-depression pulses, demonstrating the complete reversibility of the SET and RESET transitions. Due to the more abrupt nature of the SET transition in comparison to the RESET transition (see hysteresis loops in Figure 3c), depression pulses able to stabilize different HRS were acquired by continuously increasing the depression voltage from 1.1 to 2.5 V. Subsequent potentiation pulses applied at a constant voltage amplitude following each depression pulse trend successfully restore the initial LRS. The details of the depression transients are shown in Figure 4d. Departing from the initial LRS, distinct saturation resistances are observed, which are solely dependent on the amplitude of the writing pulse. Therefore, cryogenic neuromorphic neural networks based on YBCO could be trained by simply relying on the pulses of different voltage amplitudes, thus facilitating their operation.

2.3. Modeling of the Switching Performance

After experimentally characterizing the device, we propose a physics-based compact model to simulate resistive switching behavior and analog synaptic plasticity. This compact model aims not only to clarify the key elements underlying the memristive effects but also to enable the simulation of neuromorphic circuits based on these devices. First, we propose a simple description of the device physics consistent with our interpretation of the experimental results. This enables the definition of an internal state variable for our devices and describes their memristive behavior. The simple model also explains why the resistance saturates at different values for different voltage pulse amplitudes (see Figure 4d). Second, we propose a balance equation between potentiation and depression to describe the electrical behavior of the device under arbitrarily applied voltage signals.

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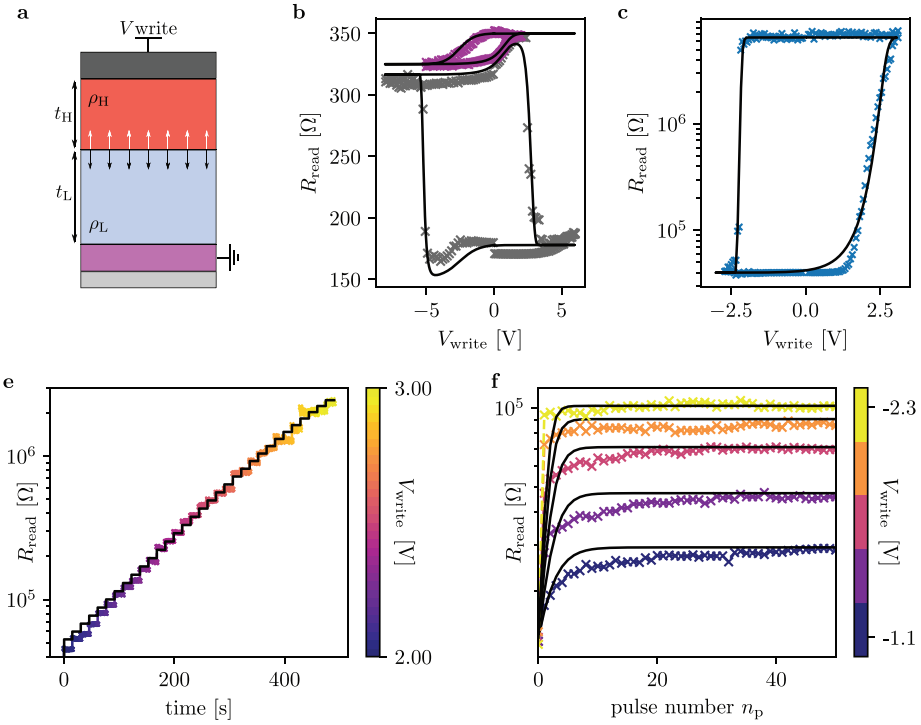

Figure 5. a) Schematic representation of the sample parameters used for the modeling. b) Fittings of the major and minor loops shown in Figure 2b). The fit of the major loop was obtained with the fitting parameters $\kappa_{P_0} = 2 \times 10^{-6}$, $\eta_p = 5$, $\kappa_{D_0} = 2 \times 10^{-12}$, $\eta_d = -6$, $R_{max} = 295$, and $R_{min} = 155$. To fit the minor loop, the parameters were set to $\kappa_{P_0} = 6 \times 10^{-3}$, $\eta_p = -1.7$, $\kappa_{D_0} = 9$, $\eta_d = 0.6$, $R_{max} = 26$, and $R_{min} = -1$. c) Fitting of the hysteresis loop measured for a typical patterned device (Figure 2c) using the parameters $\kappa_{P_0} = 10^{-30}$, $\eta_p = -32$, $\kappa_{D_0} = 0.5$, $\eta_d = 1.75$, $R_{max} = 4 \times 10^4$, and $R_{min} = 6.5 \times 10^6$. e,f) The fitting parameters in c) were used to reproduce the stable resistance states shown in Figure 4a,d. For clarity, only five depression cycles are shown in f). The color bars in e,f) correspond to the experimental voltages. All the simulation data is shown with black lines.

As schematically shown in **Figure 5a**, we consider that the YBCO film is divided into a high-resistance layer (HRL) with thickness t_H and a low-resistance layer (LRL) with thickness t_L. The total thickness of the layer being $t = t_H + t_L$. These layers are modulated during the SET and RESET processes, keeping the total thickness of the layer constant. The internal state variable is defined as $g = t_L/t$. This variable ranges from $g = 0$ (full depression) to $g = 1$ (full potentiation). For simplicity, we assume that the voltage drop in these layers is linear and that their respective resistances are $R_L = \rho_L t_L/A$ and $R_H = \rho_H t_H/A$, with $\rho_{L,H}$ and A being the resistivities and the device area, respectively. Since the resistances are in series, the structure is that of a voltage divider, and we can calculate the field in both layers. Since both hole trapping and oxygen transport are likely controlled by the electric field in the LRL and they are expected to exponentially depend on the voltage, we assume that there is a critical field, F_{crit}, below which these mechanisms are suppressed. Under these assumptions, simple calculations allow us to prove that there is a minimum value of g_{min}, which is reached under the depression bias, V_{crit}. There is no limitation for g under potentiation conditions, and it can always reach $g = 1$. The value of g_{min} depends on the depression voltage as

$$g_{min}(V) = \frac{1}{r-1}\left(r - \frac{V}{V_{crit}}\right) \quad (1)$$

where $V_{crit} = F_{crit}/t$ and $r = \rho_H/\rho_L = R_{max}/R_{min}$, these being the maximum and minimum resistances related to $g = 0$ and $g = 1$, respectively. The previous equation is only valid in the voltage interval $V_{crit} \leqslant V \leqslant rV_{crit}$. Above this interval $g_{min} = 0$ and below it $g_{min} = 1$. For the description of the memristor dynamics, we follow a previous approach proposed for filamentary switching.[56] Although the physics is completely different, the mathematical description is straightforwardly equivalent in terms of phenomenological parameters. The evolution of the memory state variable g is modeled as

$$\frac{dg}{dt} = \kappa_P(V)(1-g) - \kappa_D(V)(g - g_{min}) \quad (2)$$

where the potentiation and depression rate constants are considered to depend exponentially on the applied voltage by

$$\kappa_{P,D}(V) = \kappa_{P_0,D_0} e^{\eta_{P,D} V} \quad (3)$$

where κ_{P_0,D_0} are fitting constants and $\eta_{P,D} V$ are transition rates. This exponential dependence is consistent with the transition times to stable resistance states during the application of pulse trains, with increasing amplitude (Figure 4a,c). Depending on whether potentiation/depression occurs at positive/negative voltages, $\eta_{P,D}$ are positive/negative. For a constant applied voltage, the solution of the equation is analytical and, provided that we

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consider small enough time intervals Δt, this provides us with a recursive solution for arbitrary time-dependent voltage waveforms:

$$g(t) = \frac{\kappa_P + \kappa_D g_{min}}{\kappa_P + \kappa_D}\left[1 - \exp(-(\kappa_P + \kappa_D)\Delta t)\right] + g(t - \Delta t)\exp(-(\kappa_P + \kappa_D)\Delta t) \quad (4)$$

It is noted here that Δt must be small, e.g., in the scale of voltage variations, to obtain an accurate solution. After calculating $g(t)$, the device resistance is calculated as

$$R = \frac{R_{max} R_{min}}{R_{min}(1 - g) + R_{max} g} \quad (5)$$

Using this model, it is possible to reproduce the main experimental results presented in the previous sections. The major and minor loops are reproduced by considering two different equations for g_{minor} and g_{major} and adding their corresponding resistances, as illustrated in Figure 5b. Remarkably, the bumps of the major loops, i.e., the signature of the coupling between hole and oxygen-related phenomena, are nicely captured. In Figure 5c, the optimized resistance hysteresis of patterned devices, with high ratio R_{HRS}/R_{LRS}, is well fitted by the proposed model and the relevant parameters are extracted. With this set of parameters, we have successfully simulated the evolution of the resistive state under a depression pulse staircase in Figure 5d and the depression transients of the potentiation and depression cycles in Figure 5f.

The presented compact model is valid for any input signal since the recursive equation for $g(t)$ (Equation 4) does not impose any condition on the input $V(t)$. However, the integration time Δt used in the recursive approach must be appropriately matched to the frequency of the input signal, meaning it should be sufficiently small so that $V(t)$ does not significantly change during Δt. This is a very simple approach based on the underlying physics of the devices. It integrates two layers with distinct resistances to replicate the behavior of the LRS and HRS layers. This compact model allows us to fit the experimental results by extracting a specific set of parameters. While it is useful for circuit simulations, it is not intended to serve as a predictive tool. Gaining a deeper understanding of the physical phenomena behind the switching mechanisms and predicting device behavior under operational conditions requires a more comprehensive approach, which is beyond the scope of this work.

3. Conclusion

We have demonstrated that both electrochemical oxygen diffusion and electrostatic charge doping can trigger resistive switching in superconducting YBCO devices. These two types of switching coexist at high temperatures and exhibit opposite switching polarities. Notably, for cryogenic memory applications, we have observed a considerable enhancement in the resistance hysteresis loops associated with charge motion at low temperatures, even below the superconducting transition. Our findings highlight the critical role paved by the oxygen-depleted layer and the resultant hole-doping gradient formed beneath the switching electrode during sample preparation at room temperature, which governs the switching performance at cryogenic temperatures. Experimental results indicate that the bottom electrode has a minimum influence on switching performance and mainly serves as a passive component within the overall system. However, it may offer valuable insights into additional effects coming from the unique underlying order parameters of superconductivity and magnetism,[57] as well as facilitate the introduction of new functionalities. The devices exhibit completely reversible potentiation and depression effects at cryogenic temperatures, and a large number of non-volatile resistance states may be achieved through the linear increase of voltage. We have developed a physical-based compact model that accurately describes the switching performance in good agreement with experimental measurements.

YBCO-LSMO heterostructures represent a promising material for designing energy-efficient analog memory states and neuromorphic functionalities using the physics of metal-insulating transitions in superconducting cuprates. Low-power, non-volatile superconducting memories that operate at cryogenic temperatures can be seamlessly integrated into emerging energy-efficient technologies, including quantum computing and superconducting electronics. Moreover, the incorporation of superconducting switching elements offers significant advantages, including inherent energy efficiency and the ability to interconnect through lossless, low-dispersion superconducting lines. The antagonistic properties of superconducting and ferromagnetic materials may provide additional opportunities for leveraging the field-induced metal-insulating transition by manipulating the coupling between distinct order parameters across interfaces, such as through proximity effects. To explore this further, YBCO/LSMO bi-layers may be grown in-situ to ensure clean interfaces. While this investigation extends beyond the scope of this paper, it remains an intriguing area for future research.

4. Experimental Section

Thin Film Growth: Epitaxial films of $La_{0.7}Sr_{0.3}MnO_3$, with a thickness of 30 nm, were grown by off-axis radio frequency sputtering on (001)-oriented $SrTiO_3$ single-crystal substrates, in a sputtering system. The sample is oriented perpendicular to the LSMO target, while the temperature is kept at 850 °C and the pressure is adjusted to be ≈20 mbar under a constant flow of 2 sccm of Argon and 20 sccm of oxygen during the deposition. After the deposition, the thin films were annealed at 850 °C at 500 mbar in a pure oxygen atmosphere for 1 h. The Epitaxial 50 nm and 100 nm thick YBCO films were grown on top of LSMO, ex-situ, by pulsed laser deposition (PLD). Substrates were heated up to 810 °C, with an oxygen partial pressure of 0.3 mbar and a distance of 52.5 mm from the target. Ablation of the target material is induced by a high fluence laser (≈2 J cm^{-2}) working at a frequency of 5 Hz. During cool down to room temperature, the sample is kept in an oxygen atmosphere of 1 bar to ensure proper oxygenation of the deposited thin films.[32] 100 nm silver and gold electrodes were deposited in a *TSST* sputtering system. Insulating Al_2O_3 capping layers were grown by Atomic Layer Deposition in a *Atomic Layer Deposition System Savannah from Cambridge NanoTech* at a temperature of 150 °C. The films were patterned via photolithography, lift-off and wet etching with orthophosphoric acid H_3PO_4 for YBCO and Piranha solution for LSMO. The different steps of the fabrication process are schematically shown in Figure S4 of the Supporting Information.

Characterization: Basic thin film characterization was done by SQUID magnetometry.

Voltage Pulses: The pulsed experiments were conducted with *Keithley 2604B and 2601 Source Measure Units* (SMUs). For clarification and as a key part of the manuscript, the pulse trains are described in detail in the main section. A homemade software was written in Python to control the SMUs.

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The code is available upon request. The low-temperature measurements were conducted in a *Quantum Design PPMS System*.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

cryogenic memristor, compact model, high-temperature superconductor, metal-insulator transition, neuromorphic computing

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[1] C.-W. Tsai, C.-F. Lai, H.-C. Chao, A. V. Vasilakos, *J. Big Data* **2015**, *2*, 21.
[2] M. Mitchell Waldrop, *Nature* **2016**, *530*, 145.
[3] S. X. Zou, L. Y. Xiaoming Chen, Y. Han, *Science China Information Sciences* **2021**, *64*, 160404.
[4] J. Shalf, *Philos. Trans. R. Soc., A* **2020**, *378*, 20190061.
[5] *International Roadmap for Devices and Systems*, IEEE Advancing Technology for Humanity, **2023**, 1–77.
[6] R. Saligram, A. Raychowdhury, S. Datta, *Chip* **2024**, *3*, 100082.
[7] D. S. Holmes, S. Member, A. L. Ripple, M. A. Manheimer, *IEEE Trans. Appl. Supercond.* **2013**, *23*, 1701610.
[8] A. I. Braginski, *J. Supercond. Novel Magn.* **2019**, *32*, 23.
[9] P. Krantz, M. Kjaergaard, F. Yan, T. P. Orlando, S. Gustavsson, W. D. Oliver, *Appl. Phys. Rev.* **2019**, *6*, 2.
[10] Q. A. Memon, M. Al Ahmad, M. Pecht, *Quantum Reports* **2024**, *6*, 627.
[11] S. Alam, M. Hossain, S. R. Srinivasa, A. Aziz, *Nat. Electron.* **2023**, *6*, 185.
[12] E. Morosan, D. Natelson, A. H. Nevidomskyy, Q. Si, *Adv. Mater.* **2012**, *24*, 4896.
[13] S. Keimer, B.and Kivelson, M. Norman, S. Uchida, J. Zaanen, *Nature* **2015**, *518*, 179.
[14] E. Janod, J. Tranchant, B. Corraze, M. Querré, P. Stoliar, M. Rozenberg, T. Cren, D. Roditchev, V. T. Phuoc, M. P. Besland, L. Cario, *Adv. Funct. Mater.* **2015**, *25*, 6287.
[15] P. Liu, B. Lei, X. Chen, L. Wang, X. Wang, *Nature Technical Reviews* **2022**, *4*, 336.
[16] Y. Guo, D. Qiu, M. Shao, J. Song, Y. Wang, M. Xu, C. Yang, P. Li, H. Liu, J. Xiong, *Adv. Mater.* **2023**, *35*, 1.
[17] Y. Zhou, S. Ramanathan, *Proc. IEEE* **2015**, *103*, 1289.
[18] Y. Wang, K. M. Kang, M. Kim, H. S. Lee, R. Waser, D. Wouters, R. Dittmann, J. J. Yang, H. H. Park, *Mater. Today* **2019**, *28*, 63.
[19] P. Stoliar, J. Tranchant, B. Corraze, E. Janod, M. P. Besland, F. Tesler, M. Rozenberg, L. Cario, *Adv. Funct. Mater.* **2017**, *27*, 1604740.
[20] A. Cavalleri, C. Tóth, C. W. Siders, J. A. Squier, F. Ráksi, P. Forget, J. C. Kieffer, *Phys. Rev. Lett.* **2001**, *87*, 237401.
[21] Z. Yang, C. Ko, S. Ramanathan, *Annu. Rev. Mater. Res.* **2011**, *41*, 337.
[22] M. S. Laad, L. Craco, *Adv. Quantum Technol.* **2024**, *2200186*, 1.
[23] D. Marković, A. Mizrahi, D. Querlioz, J. Grollier, *Nat. Rev. Phys.* **2020**, *2*, 499.
[24] D. B. Strukov, G. S. Snider, D. R. Stewart, R. S. Williams, *Nature* **2008**, *453*, 80.
[25] Z. Wang, H. Wu, G. Burr, C. Hwang, K. Wang, Q. Xia, J. J. Yang, *Nat. Rev. Mater.* **2020**, *5*, 173.
[26] M. Xu, X. Chen, Y. Guo, Y. Wang, D. Qiu, X. Du, Y. Cui, X. Wang, J. Xiong, *Adv. Mater.* **2023**, *35*, 51.
[27] A. Mehonic, D. Ielmini, K. Roy, O. Mutlu, S. Kvatinsky, T. Serrano-Gotarredona, B. Linares-Barranco, S. Spiga, S. Savelev, A. G. Balanov, N. Chawla, G. Desoli, G. Malavena, C. M. Compagnoni, Z. Wang, J. J. Yang, G. S. Syed, A. Sebastian, T. Mikolajick, B. Noheda, S. Slesazeck, B. Dieny, T.-H. Hou, A. Varri, F. Bruckerhoff-Pluckelmann, W. Pernice, X. Zhang, S. Pazos, M. Lanza, S. Wiefels, et al., *APL Materials* **2024**, 109201.
[28] S. Marinkovic, A. Fernandez-Rodriguez, S. Collienne, S. B. Alvarez, S. Melinte, B. Maiorov, G. Rius, X. Granados, N. Mestres, A. Palau, A. V. Silhanek, *ACS Nano* **2020**, *14*, 11765.
[29] M. M. Islam, S. Alam, M. S. Hossain, K. Roy, A. Aziz, *J. Appl. Phys.* **2023**, *133*, 1.
[30] M. J. Rozenberg, M. J. Sánchez, R. Weht, C. Acha, F. Gomez-Marlasca, P. Levy, *Phys. Rev. B* **2010**, *81*, 115101.
[31] A. Palau, A. Fernandez-Rodriguez, J. C. Gonzalez-Rosillo, X. Granados, M. Coll, B. Bozzo, R. Ortega-Hernandez, J. Sune, N. Mestres, X. Obradors, T. Puig, *ACS Appl. Mater. Interfaces* **2018**, *10*, 30522.
[32] J. Alcalà, A. Fernández-Rodríguez, T. Günkel, A. Barrera, M. Cabero, J. Gazquez, L. Balcells, N. Mestres, A. Palau, *Sci. Rep.* **2024**, *14*, 1939.
[33] A. Lagarrigue, C. D. Dios, S. J. Carreira, V. Humbert, S. Mesoraca, J. Briatico, J. Trastoy, J. E. Villegas, *Supercond. Sci. Technol.* **2024**, *37*, 045007.
[34] S. Marinkovic, D. Stoffels, S. Collienne, A. Fernandez-Rodriguez, N. Mestres, A. Palau, A. Silhanek, *Phys. Rev. B* **2024**, *110*, 165157.
[35] S. Collienne, S. Marinković, A. Fernández-Rodríguez, N. Mestres, A. Palau, A. V. Silhanek, *Adv. Electron. Mater.* **2022**, *8*, 1.
[36] J. Mannhart, *Supercond. Sci. Technol.* **1996**, *9*, 49.
[37] C. H. Ahn, A. Bhattacharya, M. Di Ventra, J. N. Eckstein, C. D. Frisbie, M. E. Gershenson, A. M. Goldman, I. H. Inoue, J. Mannhart, A. J. Millis, A. F. Morpurgo, D. Natelson, J. M. Triscone, *Rev. Mod. Phys.* **2006**, *78*, 1185.
[38] X. Leng, J. Garcia-Barriocanal, S. Bose, Y. Lee, A. Goldman, *Phys. Rev. Lett.* **2011**, *107*, 027001.

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[39] Y. Zhou, S. Ramanathan, *Crit. Rev. Solid State Mater. Sci.* **2013**, *38*, 286.
[40] R. Muenstermann, T. Menke, R. Dittmann, R. Waser, *Adv. Mater* **2010**, *22*, 4819.
[41] V. Rouco, F. Gallego, D. Hernandez-Martin, D. Sanchez-Manzano, J. Tornos, J. Beltran, M. Cabero, F. Cuellar, D. Arias, G. Sanchez-Santolino, F. J. Mompean, M. Garcia-Hernandez, A. Rivera-Calzada, M. Varela, M. C. Muñoz, C. Leon, Z. Sefrioui, J. Santamaria, *APL Mater.* **2021**, *9*, 3.
[42] M. Scherff, B. Meyer, J. Hoffmann, C. Jooss, *J. Appl. Phys.* **2011**, *110*, 043718.
[43] R. Liang, D. A. Bonn, W. N. Hardy, *Phys. Rev. B* **2006**, *73*, 180505.
[44] A. Stangl, A. Palau, G. Deutscher, X. Obradors, T. Puig, *Sci. Rep.* **2021**, *11*, 1.
[45] H. J. Zhang, X. P. Zhang, J. P. Shi, H. F. Tian, Y. G. Zhao, *Appl. Phys. Lett.* **2009**, *94*, 092111.
[46] E. Mikheev, B. D. Hoskins, D. B. Strukov, S. Stemmer, *Nat. Commun.* **2014**, *5*, 1.
[47] Y. Chen, L. Chen, G. Lian, G. Xiong, *J. Appl. Phys.* **2009**, *106*, 2.
[48] X. Liu, T. Yang, S. Chen, J. Wu, C. S. Tang, Y. Ning, Z. Chen, L. Dai, M. Sun, M. Chen, K. Han, D. Zhou, S. Zeng, S. Sun, S. Li, M. Yang, M. B. Breese, C. Cai, T. Venkatesan, A. T. Wee, X. Yin, *Appl. Phys. Rev.* **2025**, *12*, 1.
[49] C. Jooss, L. Wu, T. Beetz, R. F. Klie, M. Beleggia, M. a. Schofield, S. Schramm, J. Hoffmann, Y. Zhu, *Proc. Natl. Acad. Sci. USA* **2007**, *104*, 13597.
[50] K. Leng, X. Yu, Z. Ma, W. Li, J. Xu, L. Xu, K. Chen, *Appl. Phys. Lett.* **2022**, *120*, 1.
[51] Y. Lin, F. Meng, T. Zeng, Q. Zhang, Z. Wang, Y. Cheng, X. Zhao, L. Gu, H. Xu, Y. Liu, *Adv. Funct. Mater.* **2023**, *33*, 1.
[52] T. Wu, S. Gao, Y. Li, *Small* **2024**, *20*, 1.
[53] A. Sawa, *Mater. Today* **2008**, *11*, 28.
[54] J. J. Yang, D. B. Strukov, D. R. Stewart, *Nat. Nanotechnol.* **2013**, *8*, 13.
[55] D. Ielmini, S. Ambrogio, *Nanotechnology* **2020**, *31*, 092001.
[56] E. Miranda, G. Milano, C. Ricciardi, *IEEE Trans. Nanotechnology* **2020**, *19*, 609.
[57] M. G. Blamire, in: *Superconductors at the Nanoscale*, (Eds.: R. Wordenweber, V. Moshchalkov, S. Bending, F. Tafuri), De Gruyter, Berlin,Boston **2017**, pp. 473–486.

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