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Split Capacitive Boosting Technique for High-Slew-Rate Single-Ended Amplifiers: Design and Optimization

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Abstract

Parallel-type slew-rate enhancers (PSREs) improve the driving capability of operational transconductance amplifiers (OTAs) for large capacitive loads. While capacitive-boosting (CB) techniques enhance PSRE efficiency in fully-differential designs, their application to single-ended configurations—common in off-chip load driving—remains unexplored. This work identifies a critical limitation of standard CB in single-ended unity-gain buffers: severe slew-rate degradation due to large common-mode input swings. To overcome this, we propose a novel split CB (SCB) technique for single-ended PSREs that strategically divides the boosting capacitance. Simulated in a 0.18- μm CMOS process, the proposed method achieves a $\times 5.53$ reduction in settling time compared to standard CB when driving a 1-nF load. With only 4 μA quiescent current under a 3.3-V supply, it attains a 1% settling time of 2.56 μs for 2.64-V steps, demonstrating robust performance across process-voltage-temperature variations. This technique enables low-power, high-speed interfaces for drivers of off-chip devices.

Keywords: capacitive boosting; slew-rate enhancement; LCD/OLED drivers; single-ended amplifier; operational transconductance amplifier (OTA); settling time optimization; low-power design; CMOS analog circuits



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1. Introduction

The driving of large capacitive loads—such as those encountered in display drivers (LCD/OLED), sensor interfaces, biomedical signal buffers, and communication circuits—demands operational transconductance amplifiers (OTAs) with high slew rate (SR) and fast settling. In display applications, stringent pixel charging requirements and energy constraints have led to various architectural strategies [1]. Early multistage class-B topologies [2,3] laid the groundwork with transient-aware biasing, achieving μA -level quiescent currents and sub-3 μs settling for multi-nF loads. In addition, the inclusion of a resistor in series to the amplifier output allowed a zero-based frequency compensation in such multistage structures, increasing stability at higher capacitive loads [4]. Dual-path push–pull structures emerged as highly efficient class-B mechanisms coupled to a class-AB main signal path [5–7]. A compact and efficient class-AB mechanism based on a floating PMOS/NMOS mesh was proposed in [8]. Innovations like distributed Miller compensation have also been introduced to enhance stability at all signal levels [9].

Moving towards general-purpose techniques tailored for large capacitive load driving, a range of amplifier topologies has been developed to address the conflicting requirements

of stability (small-signal behavior) and large-signal responsiveness (slew rate), with approaches varying significantly depending on whether a single-stage or multistage design strategy is adopted.

Single-stage architectures are often preferred in ultra-low-power applications due to their compactness, simplicity, and reduced static power consumption. However, they typically struggle to simultaneously deliver high gain, large output swing, and sufficient capacitive load drivability. Various techniques have been proposed to overcome these limitations:

- Several designs embed dynamic current-boosting elements to improve large-signal performance. For example, the amplifier in [10] employs a current-detection-based slew-rate enhancement (SRE) circuit to boost transient current during load events, leading to a $>43\times$ improvement in slew rate when driving a 470 pF load. Similarly, ref. [11] proposes current starving and feeding to achieve a 600–1100% SR enhancement while maintaining low quiescent current. The amplifier in [12] follows a super class-AB approach in a recycling folded cascode (RFC) topology, where an adaptive bias circuit and local CMFB further improve GBW and SR by factors of 3 and 34, respectively, without additional power. The work in [13] introduces a non-linear nested current mirror to push the class-AB operation further in the single-stage regime, demonstrating significant improvements in slew rate and GBW without additional power overhead.
- Some single-stage approaches focused on small-signal frequency-domain behavior. In [14], the nested current mirror (NCM) method achieves GBW scalability across a 0.15–15 nF range without requiring compensation capacitors, offering 72–84 dB gain with $>60^\circ$ phase margin, exploiting current mirroring hierarchies. A similar balance between SR and small-signal performance is achieved in [15,16], which utilizes gain-enhanced current mirrors with class-AB push–pull stages. Another example is [17], where a bulk-driven OTA with local positive feedback exploits body terminals and a dedicated SR enhancement block to sustain performance with loads up to 10 nF while maintaining quiescent current under 1.4 μA .

Multistage topologies allow higher gain and output swing but complicate frequency compensation, especially under large capacitive loads. Recent innovations mitigate these challenges through systematic compensation strategies or control-centric design frameworks:

- In [18,19], Yan et al. proposed three-stage and two-stage amplifiers employing parasitic pole cancellation and embedded capacitor multipliers (CM), respectively. The CM technique enhances SR and area efficiency by leveraging a small sub-pF capacitor. In [20], a local-feedback-enhanced compensation scheme for three-stage amplifiers is proposed, showing a GBW of 1.34 MHz and phase margin of 52.7° when loaded with 500 pF in unity-gain configuration. The amplifier in [21] employs an adaptively varied medium-impedance node, enabling ultra-high slew rate (up to 8.67 V/ μs) over a wide 0.1–15 nF load range.
- A number of works improve the GBW and phase margin through novel compensation strategies. For instance, ref. [22] uses a signal- and transient-current boosting (STCB) mechanism, extending GBW and improving SR while keeping the phase margin above 80° . Likewise, ref. [23] implements a three-stage cascode Miller-compensated amplifier with local impedance attenuation for complex-pole control, achieving both high DC gain and fast settling times. The amplifier in [24] introduces dynamic biasing and a systematic optimization of settling time using contour plot analysis, offering robust stability for three-stage designs. Ref. [25] is also noteworthy, as it utilizes inner feedforward compensation in a two-stage amplifier to achieve high current efficiency and a GBW of 2.01 MHz at just 108 μW of consumption, targeting pF-range

loads, but still relevant for scalable designs. Furthermore, ref. [26] demonstrates how local positive feedback in a folded cascode architecture can enhance SR, GBW, and DC gain simultaneously, outperforming even recycling FC-OTAs. Innovations in compensation techniques have also been introduced for high-speed designs [27]. Recently, an interesting technique for unconditional stability for any value of capacitive load in a two-stage architecture has been demonstrated, employing an output branch replica connected to the OTA virtual ground terminal when configured as a standard inverting amplifier [28].

While both single-stage and multistage designs have demonstrated competitive figures of merit (FOMs), the choice of strategy often reflects tradeoffs in complexity, power, and target load range. Parallel-type slew-rate enhancers (PSREs) appear as an alternative strategy to deal with stability vs. slew-rate trade-offs by decoupling large-signal dynamics from static power—a principle pioneered by Nagaraj in 1990 [29] and later refined for modern technology nodes (e.g., Catania et al.'s 0.18- μm design proposed in [30]). Naderi et al. employed PSRE structures in high-speed pipelined analog-to-digital converters [31,32], demonstrating superior performance even with very light capacitive loads (500 fF). The work of Koh et al. [33] stems from the PSRE idea, also introducing refined techniques for near-zero deadzone control to obtain class-C operation. The work in [34] is inspired by similar principles and implements a feedforward path using a dynamic circuit with a capacitor-based hysteresis detector. However, PSRE efficiency hinges on activation latency and seamless reintegration during settling, challenges exacerbated in advanced displays where sub-1% settling must coexist with $<20 \mu\text{W}$ power budgets. Recent PSREs, like Gagliardi et al.'s LCD-oriented design [35] (2023), demonstrate rail-to-rail capability under 1 nF loads but reveal lingering compromises between achievable slew rate and overall settling performance—a gap this work aims to bridge. Importantly, in [30], the capacitive boosting (CB) technique is introduced in the PSRE block, showing great turn-on improvement on fully differential structures. Nevertheless, to the best of our knowledge, CB boosting has not yet been demonstrated in single-ended architectures such as those employed for LCD and large external load drivers.

This paper is organized as follows: Section 2 provides the theoretical basis for the PSRE-assisted OTA topologies; Section 3 discusses, for the first time, the single-ended parallel-type slew-rate enhancer with standard capacitive boosting and its limitations, highlighting the trade-offs between achievable slew rate and the reduction in turn-on delay; Section 4 introduces a key topological improvement to overcome these limitations, namely the split capacitive boosting (SCB); Section 5 showcases SCB-PSRE-assisted OTAs under typical LCD-driver design specifications in 0.18- μm CMOS, validated through extensive electrical simulations. A state-of-the-art comparison against designs previously implemented in the same technological node is also provided. Finally, Section 6 concludes the paper.

2. Parallel Slew-Rate Enhancer Principles

The principle of a PSRE-assisted OTA is schematically represented in the block diagrams of Figure 1a, considering a single-ended capacitive load. The output currents of both the OTA and the PSRE are shown in Figure 1b, qualitatively plotted as a function of the differential input voltage (DC transconductance characteristics). While the OTA typically shows great sensitivity to the input signal within a small region around the zero differential input, the PSRE provides large output current outside of this region, where the OTA output current saturates to a constant value. These characteristics allow the PSRE to increase the overall SR exclusively during the initial phase of such a transient, when the absolute value of the input differential voltage exceeds a specific activation threshold. During the transient

[Figure 1c], the input differential voltage decreases, eventually deactivating the PSRE, which then transitions to a high-impedance state. This ensures that the final fine-tuning of the output voltage is handled by the main OTA. Hence, the presence of the PSRE does not affect the OTA DC gain, offset, noise, and stability performances at the steady state, effectively isolating the SR from other specifications and simplifying the design procedure.

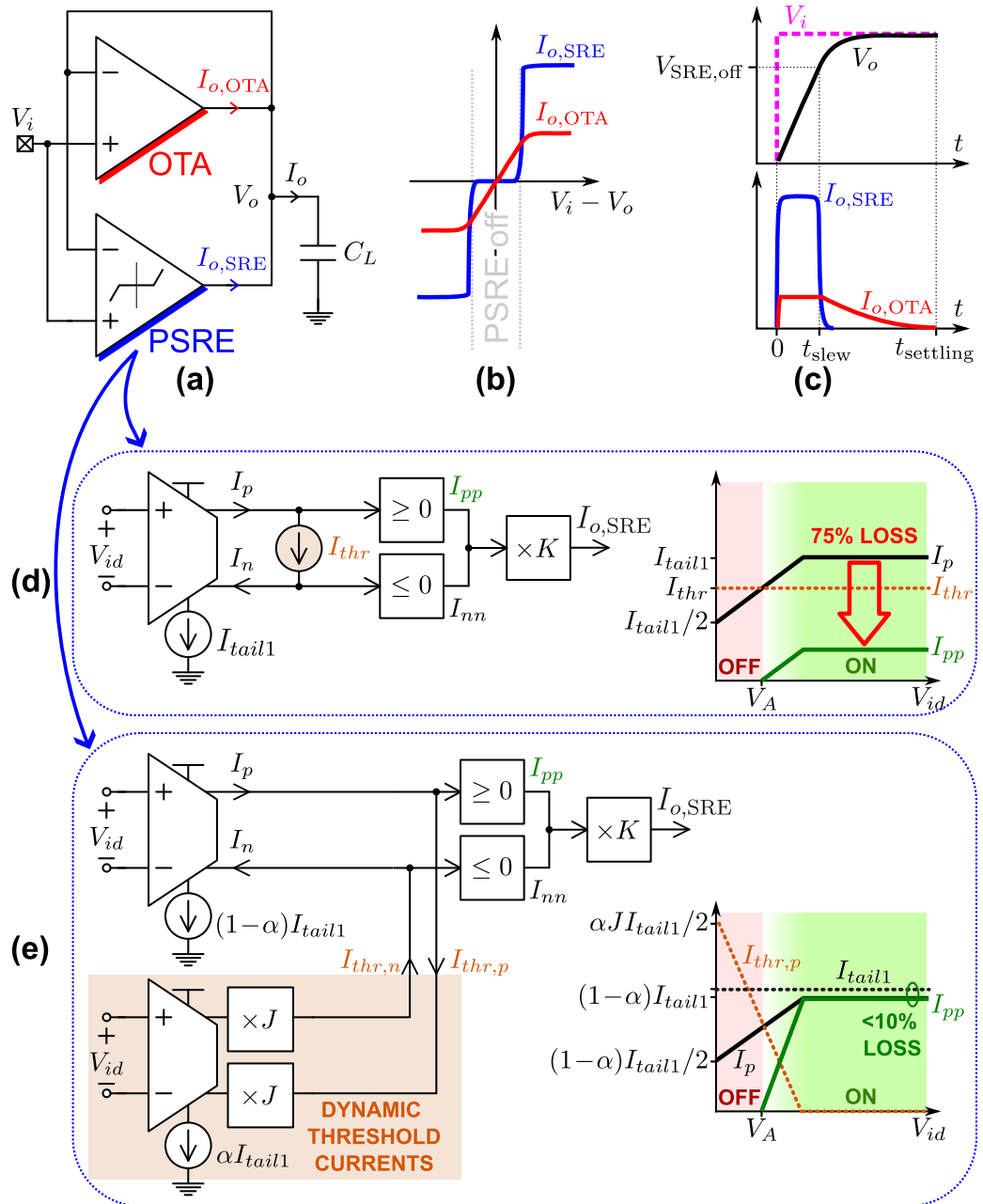


Figure 1. Operating principle of a parallel-type SRE: (a) unity-gain buffer composed of a single-ended OTA assisted by a PSRE; (b) qualitative plots of the output currents of the OTA and PSRE blocks as a function of the differential input signal; (c) qualitative waveforms of the output currents in response to an input voltage step; (d) Nagaraj’s implementation with constant threshold currents I_{thr} [29]; (e) implementation embedding the dynamic-threshold-current (DTC) technique [35], where the constant threshold currents are replaced by signal-dependent currents I'_p and I'_n .

Figure 1d shows the functional diagram of the original PSRE, introduced by Nagaraj in 1990 [29]. The circuit is based on a differential transconductive stage, supplied by the tail current I_{tail1} , which provides I_p and I_n currents at its output nodes. A fixed threshold current, I_{thr} , is subtracted from both I_p and I_n before hard-limiting blocks (≤ 0 and ≥ 0)

and the final $\times K$ current amplification. As shown in the sketched current characteristics of Figure 1d, the resulting current after the hard limiter, I_{pp} , is reduced by a factor $\times 4$ due to the restricted interval of choice of I_{thr} [$I_{thr} \in (I_{tail1}/2, I_{tail1})$], with $I_{thr} = (3/4)I_{tail1}$ representing a typical robust choice. The choice of I_{thr} also determines the value of the PSRE activation voltage, V_A .

Since the first PSRE, numerous improvements have been proposed. For example, Sakurai et al. [36] introduced a folded-cascode OTA with an internal SR enhancement circuit, while Lee and Mok [37] proposed single-point-detection circuits for single-stage amplifiers. More recently, Gambhir et al. [6] demonstrated a high-speed three-stage class-B output buffer for LCD-driving applications, achieving significant improvements in settling time and power efficiency. Similarly, Wen et al. [4] developed a rail-to-rail buffer using dynamic-current feedback, which achieved a high SR and low power consumption for OLED source drivers. Figure 1e shows an efficient PSRE implementation which incorporates a dynamic-threshold-current (DTC) technique [35]. Here, instead of using a fixed I_{thr} , an auxiliary transconductor stage, biased at a small portion (α) of the total quiescent current of the PSRE, and also sensitive to the differential input voltage V_{id} , provides signal-dependent currents $I_{thr,p}$ and $I_{thr,n}$, which are purposely amplified ($\times J$) and subtracted from I_p and I_n , respectively. The condition $V_A > 0$ is guaranteed by making $\alpha J > 1 - \alpha$. Insofar, the maximum value of I_{pp} , $I_{pp,max}$, reached when the PSRE input pairs are fully unbalanced, results to be equal to $(1 - \alpha)I_{tail1}$, which can be made reasonably close to I_{tail1} . For example, with $\alpha = 0.1$, 90% of I_{tail1} is effectively delivered to the final $\times K$ current amplification stage, leading to larger SR for the same static supply current when compared to the solution of Figure 1d.

For optimal power efficiency, the always-on PSRE current, I_{tail1} , is often designed to be much smaller than the OTA quiescent current. This leads to possible turn-on delays owing to the $\times K$ current amplifier of Figure 1d,e, hence reducing the effectiveness of the PSRE itself. The capacitive boosting (CB) technique, consisting of providing an additional impulse-like boost to I_{tail1} , addresses this issue by accelerating turn-on delays. In prior works, this technique has been demonstrated in fully-differential PSREs [30]. However, their applicability to single-ended configurations—ubiquitous in off-chip load driving—remains mostly unexplored, leaving a critical gap in power-efficient, high-speed, single-ended designs.

This work identifies a key limitation of standard CB in single-ended PSREs: slew-rate degradation due to common-mode input swings (Section 3). We then propose a novel CB-PSRE topology optimized for single-ended operation, avoiding detrimental dynamic currents, induced by common-mode swings in standard CB-PSREs, to minimize settling time without compromising static power consumption (Section 4). Electrical simulations of a SCB-PSRE-assisted OTA designed in 0.18- μm CMOS demonstrate a $\times 5.53$ settling-time reduction compared to conventional CB-PSREs when driving 1-nF loads, achieving 2.56- μs 1% settling time at 4- μA total static current consumption. The proposed design also exhibits robustness to PVT variations, making it suitable for display drivers, MEMS interfaces, and other large-capacitive-load applications.

The contributions of this work include: (i) the first analysis of CB-induced SR limitations in single-ended PSREs, linking performance degradation of the PSRE (in terms of achievable SR) to common-mode dynamics, (ii) an optimized SCB-PSRE architecture for single-ended systems, validated by comparative simulations, and (iii) a power-efficient solution (13.2 μW) for 1-nF loads, with $\times 5.53$ faster settling time than prior CB approaches.

3. Single-Ended Parallel-Type Slew-Rate Enhancer with Standard Capacitive Boosting

3.1. Implementation of the PSRE with Dynamic Threshold Currents

Figure 2 shows the transistor-level schematic view of the PSRE with dynamic threshold currents (DTC) [35], augmented by the addition of the capacitive booster C_B , as proposed in [30]. In the following, we refer to this configuration as the *standard CB* configuration to distinguish it from the novel approach introduced in Section 4.

The PSRE block is ideally designed to deliver a DC output current $I_{o,SRE}$ described by:

$$I_{o,SRE} = \begin{cases} 0 & |V_{id}| < V_A, \\ \text{sign}(V_{id}) \cdot I_{o,max,SRE} & |V_{id}| \geq V_A, \end{cases} \quad (1)$$

where $V_{id} = V_{ip} - V_{in}$ is the differential input voltage, $I_{o,max,SRE}$ is the maximum output current available during slewing transients, and V_A is the PSRE activation threshold (defining its “deadzone” around zero differential input). For optimal transient response, V_A is typically set near the boundary of the OTA linear region [see Figure 1b].

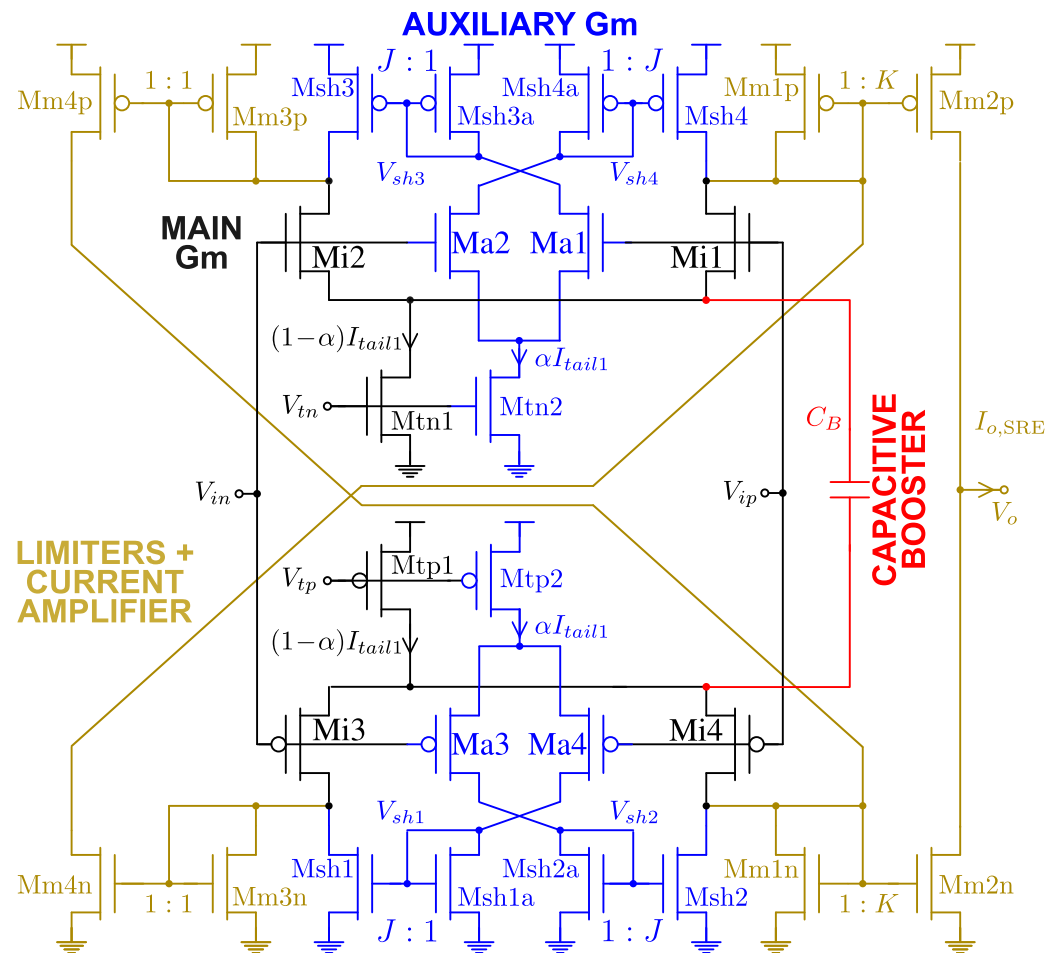


Figure 2. PSRE schematic with dynamic threshold currents (DTC), including capacitive boosting (CB) between the source terminals of the main differential pairs (standard CB).

The PSRE in Figure 2 consists of: (i) main transconductors (Mtn1-Mi1-Mi2, Mtp1-Mi3-Mi4), (ii) auxiliary transconductors (Mtn2-Ma1-Ma2-Msh3a-Msh3-Msh4a-Msh4, Mtp2-Ma3-Ma4-Msh1a-Msh1-Msh2a-Msh2), (iii) current mirrors (Mm1p-Mm2p, Mm1n-Mm2n, Mm3p-Mm4p, Mm3n-Mm4n) for hard-limiting and amplification, (iv) the capacitive booster C_B between the common source nodes of the main input pairs.

Neglecting, for the moment, the role played by C_B , it can be easily shown that the PSRE delivers maximum output current equal to:

$$I_{omax,SRE} = 2K(1 - \alpha)I_{tail1}, \quad (2)$$

when both NMOS and PMOS pairs are active. However, when the supply or ground rail is approached during rail-to-rail input swings, one pair eventually turns off, reducing $I_{omax,SRE}$ by 50% (see Section 3.3).

As analytically derived in [35], V_A depends on various factors: (i) the fraction α of the total PSRE quiescent current used to supply the auxiliary transconductor and (ii) the current-mirror gain J , defined as $J = \beta_{Msh1-4}/\beta_{Msh1a-4a}$, with $\beta = \mu C_{ox}W/L$, where symbols μ , C_{ox} , W and L indicate the carrier mobility, the gate capacitance per unit area, the channel width and the channel length of MOS transistors. In weak-inversion operating conditions, the activation threshold V_A can be expressed as in (3) after analytical manipulations relying on descriptions of MOS behavior based on the Enz-Krummenacher-Vittoz (EKV) model [38,39]:

$$V_A = nU_T \ln\left(\frac{\alpha J}{1 - \alpha}\right), \quad (3)$$

where n is the subthreshold slope factor and U_T is the thermal voltage (i.e., $U_T = k_B T/q$, with k_B indicating the Boltzmann constant, T the absolute temperature and q the elementary charge). On the other hand, in strong-inversion conditions and assuming $\beta_{ia} = \alpha\beta_i$:

$$V_A = \frac{\sqrt{\alpha J} - \sqrt{1 - \alpha}}{\sqrt{\alpha J} + 1 - \alpha} \sqrt{\frac{2nI_{tail1}}{\beta_i}}, \quad (4)$$

where symbols β_i and β_{ia} indicate the transconductance factors related to the differential pair devices fed by $(1 - \alpha)I_{tail1}$ and αI_{tail1} , respectively. To attain (4), the square-law approximation derived from the EKV model of the MOS transistor was used [38]. The assumption $\beta_{ia} = \alpha\beta_i$ is enforced directly by design through appropriate geometrical ratios for the Mi1–Mi2 and Ma1–Ma2 transistor groups in Figure 2. Specifically, $(W/L)_{a1-4} = \alpha(W/L)_{i1-4}$. It is important to emphasize that the aforementioned expressions apply to asymptotic cases corresponding to either pure weak or strong inversion operation. Real-world designs may also operate in the moderate inversion region, where V_A exhibits a dependence on the design parameters α and J that lies between the two asymptotic cases. In practical scenarios where PVT (process, voltage, temperature) variations may occur, the actual dependence of V_A on α and J can shift within the design space bounded by Equations (3) and (4). It is also worth noting that in the PSRE-assisted OTA, V_A is selected relative to the sensitivity range of the main OTA differential pair (V_{dmax}). Therefore, PVT variations tend to affect both parameters similarly, resulting in a first-order robustness of the PSRE activation mechanism.

As highlighted in [40], the PSRE current mirrors exhibit a turn-on delay (t_{ON}), degrading settling time. This phenomenon is qualitatively represented in Figure 3, where the total settling time is determined by the sequence of three distinct processes: (i) PSRE turn-on, (ii) slewing phase, and (iii) linear phase. From [40], t_{ON} is estimated to be:

$$t_{ON} \approx C_G \sqrt{\frac{2n}{\beta_m I_m}}, \quad (5)$$

where C_G is the gate capacitance of Mm1p–Mm2p and Mm1n–Mm2n, while β_m and I_m are the transconductance factor and the input current of either Mm1p or Mm1n (depending on the sign of the transient) in slewing conditions. The approximated expression of t_{ON} —a relation useful in the design process—is derived through several simplifications (e.g.,

neglecting the dependence of C_G on charge and assuming a constant I_m during turn-on). Clearly, these assumptions imply that the parameters in (5) should be interpreted as average values over the turn-on interval. Further details can be found in [40]. Thanks to the DTC approach, $I_m = (1-\alpha)I_{tail1}$ (still neglecting, for the moment, the CB effect). The C_G term is dominated by the C_{GS} parasitic capacitances of the transistors labeled with Mm, hence its effect on t_{ON} is proportional to $(1+K)$. Therefore, by increasing K in the attempt of boosting $I_{omax,SRE}$ and the SR, t_{ON} also increases. This phenomenon eventually determines the minimum achievable settling time of the considered PSRE-assisted OTA topology, when the CB technique is not used.

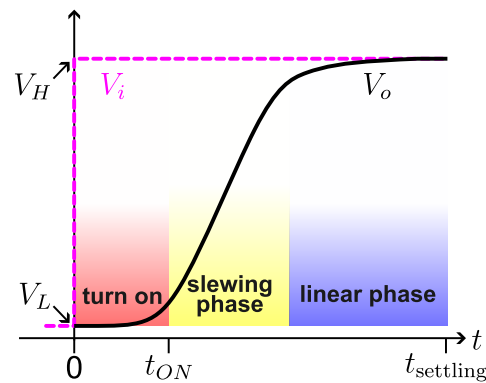


Figure 3. Qualitative plot of the output voltage, V_o , in response to an input voltage step: the total settling time is aggravated by the turn-on lag of the PSRE.

Next, we analyze the capacitive boosting achieved by placing C_B between the common-source nodes of the two complementary differential pairs in the main transconductors (Figure 2). Section 3.2 examines the effects during the turn-on phase, while Section 3.3 addresses the slewing phase effects. To the best of the authors' knowledge, the analyses reported in such two sections have not been proposed in any prior work. As for the final linear settling phase, CB has no role in it, since the PSRE output branches result in being turned off. Section 3.4 describes the main OTA implementation used alongside the PSRE of Figure 2 for the electrical simulations in Section 3.5. The limitations identified through both analytical and simulation approaches will establish the foundation for the improved CB technique proposed in Section 4.

3.2. Capacitively-Boosted Turn-On Process

We first examine the primary effect of the CB technique: reducing the turn-on delay of the PSRE. For clarity in subsequent calculations, Figure 4a reproduces the transconductive core of the PSRE from Figure 2, with annotations showing the operating states of transistors Mi1-Mi4 at the onset of a low-to-high input voltage (V_i) transition. We assume that this transition occurs at $t=0$, with V_i switching from V_L (close to ground) to V_H (close to V_{dd}), where V_{dd} denotes the supply voltage.

Prior to the transition, the n-type differential pair is turned off, with its common-source voltage V_{sn} near ground, due to the low voltage V_L applied at its inputs. Meanwhile, the common-source voltage V_{sp} of the p-type pair approximately equals $V_L + V_{SG,p}^Q$, where $V_{SG,p}^Q$ represents the source-gate voltage of Mi3-Mi4 at the steady state, [i.e., when the currents of both Mi3 and Mi4 are equal to $I_3 = \frac{1}{2}(1-\alpha)I_{tail1}$, as $V_o = V_i = V_L$]. Therefore, the initial voltage across C_B , defined as $V_c = V_{sn} - V_{sp}$, is equal to:

$$V_c(0^-) = -V_L - V_{SG,p}^Q. \quad (6)$$

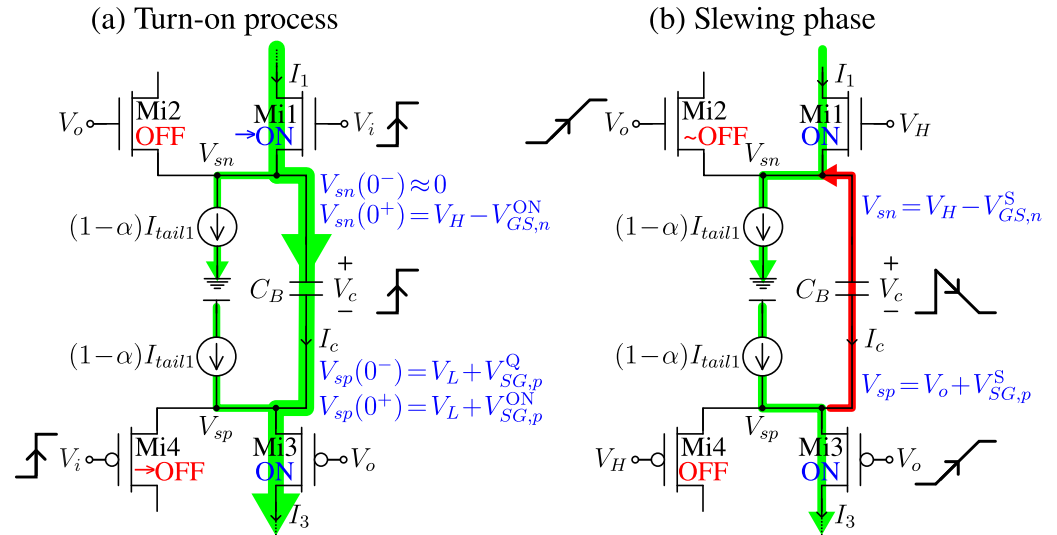


Figure 4. Operating conditions of the CB-PSRE transconductive core during a low-to-high transition of the input voltage, V_i : (a) turn-on process, analysed in Section 3.2, (b) slewing phase, analysed in Section 3.3. Both cases refer to the unity-gain configuration of Figure 1. In both sub-figures, colored arrows indicate currents flowing in each circuit branch.

Following the transition (assuming negligible rise time of V_i), Mi4 immediately turns off, while Mi3 adjusts to a new operating point characterized by $V_{SG,p}^{ON}$, corresponding to drain current $I_3 > (1-\alpha)I_{tail1}$. This new operating point is dynamic as it evolves with $I_3(t)$. However, for greater simplicity, we approximate it as an effective constant value corresponding to the average value of $V_{SG,p}(t)$ during the transient. We apply the same simplification to the gate-source voltage of Mi1.

With $V_o \approx V_L$ during the initial phase of the transient, $V_{sp}(0^+) \approx V_L + V_{SG,p}^{ON}$. Simultaneously, Mi1 turns on due to $V_i = V_H$ applied at its gate terminal, reaching gate-source voltage equal to $V_{GS,n}^{ON}$, determined by $I_1 > (1-\alpha)I_{tail1}$. This yields $V_{sn}(0^+) = V_H - V_{GS,n}^{ON}$. The updated C_B voltage becomes:

$$\begin{aligned} V_c(0^+) &= V_{sn}(0^+) - V_{sp}(0^+) = \\ &= V_H - V_L - V_{GS,n}^{ON} - V_{SG,p}^{ON}. \end{aligned} \quad (7)$$

Therefore, the voltage change occurring across C_B at the rising edge of V_i , derived from (6) and (7), results to be equal to:

$$\begin{aligned} \Delta V_c^\uparrow &= V_c(0^+) - V_c(0^-) = \\ &= V_H - V_{GS,n}^{ON} + V_{SG,p}^Q - V_{SG,p}^{ON}. \end{aligned} \quad (8)$$

The abrupt voltage variation across C_B gives rise to a charge injection phenomenon from C_B towards the input capacitance C_{Gp} of the current mirror Mm1p-Mm2p, expediting the turn-on process of transistor Mm2p, delivering the PSRE output current. Two main contributions are present: (i) charge directly injected from C_B into C_{Gp} through the n-type input transistor Mi1, acting like a closed switch, and (ii) charge injected from C_B through the p-type input transistor Mi3, the n-type mirror Mm3n-Mm4n and, finally, into C_{Gp} . The voltage variation at the gate terminal of Mm1p-Mm2p can be expressed as:

$$\Delta V_{Gp} = - \left[\frac{C_B}{C_{Gp} + C_{GS,Mi1}} + \left(\frac{C_B}{C_{Gp} + C_{Gn}^*} \right) \left(\frac{C_{Gn}^*}{C_{Gn}^* + C_{GS,Mi3}} \right) \right] \Delta V_c^\uparrow, \quad (9)$$

where we have also taken into account charge partitioning effects into the gate-source capacitances of Mi1 and Mi3, $C_{GS,Mi1}$ and $C_{GS,Mi3}$, and into the input capacitance C_{Gn}^* of current mirror Mm3n-Mm4n. The assumption of the PSRE input transistors operating in the triode region during the capacitively-boosted turn-on process is later verified in Section 3.5 based on electrical simulation results.

With sufficient ΔV_{Gp} , Mm2p enters strong inversion during the PSRE turn-on phase, producing a large instantaneous output current, equal to:

$$I_{o,SRE}^{ON\uparrow} = \frac{K\beta_m}{2n_p} \left(|\Delta V_{Gp}| - |V_{th,p}| \right)^2, \tag{10}$$

where $V_{th,p}$ and n_p are the threshold voltage and subthreshold slope factor of Mm1p-Mm2p, respectively. By designing C_B and Mm1p-Mm2p such that:

$$|\Delta V_{Gp}| > |V_{th,p}| + \sqrt{\frac{4n_p}{\beta_m} (1 - \alpha) I_{tail1}}, \tag{11}$$

the PSRE output current achieved during the turn-on process (10) overcomes the limit value it could reach without C_B , expressed by (2). However, this current level persists only during the charge injection phenomenon, lasting approximately:

$$\tau_{CI} = \frac{C_B}{g_{d1} + g_{d3}} \approx \frac{C_B}{\beta_i \left[n_n \left(V_{GS,n}^{ON} - V_{th,n} \right) + n_p \left(V_{SG,p}^{ON} - |V_{th,p}| \right) \right]}. \tag{12}$$

In the latter relationship, we assume that all input devices (Mi1-Mi4) are characterized by the same transconductance factor β_i , with n_n and n_p indicating the subthreshold slope factors of Mi1 (NMOS) and Mi3 (PMOS), respectively.

For high-to-low transitions, analogous expressions apply:

$$\Delta V_c^\downarrow = V_{dd} - V_L + V_{SG,p}^{ON} + V_{GS,n}^Q - V_{GS,n}^{ON}, \tag{13}$$

$$\Delta V_{Gn} = \left[\frac{C_B}{C_{Gn} + C_{GS,Mi4}} + \left(\frac{C_B}{C_{Gn} + C_{Gp}^*} \right) \left(\frac{C_{Gp}^*}{C_{Gp}^* + C_{GS,Mi2}} \right) \right] \Delta V_c^\downarrow, \tag{14}$$

$$I_{o,SRE}^{ON\downarrow} = -\frac{K\beta_m}{2n_n} (\Delta V_{Gn} - V_{th,n})^2, \tag{15}$$

where $V_{GS,n}^Q$ is the steady-state gate-source voltage of Mi1-Mi2 when $V_o = V_i = V_H$, C_{Gn} and C_{Gp}^* are the input capacitances of current mirrors Mm1n-Mm2n and Mm3p-Mm4p, respectively, $C_{GS,Mi2}$ and $C_{GS,Mi4}$ are the gate-source capacitances of transistors Mi2 and Mi4, respectively, and $V_{th,n}$ is the threshold voltage of Mm1n-Mm2n. We assume identical transconductance factors β_m for Mm1p and Mm1n, and equal $K\beta_m$ for Mm2p and Mm2n.

Notably, (10) and (15) may yield asymmetric currents ($I_{o,SRE}^{ON\uparrow} \neq |I_{o,SRE}^{ON\downarrow}|$) despite matched β_i and β_m , mainly due to typically different threshold voltages of n-type and p-type transistors. As demonstrated by simulations reported in Section 3.5, this asymmetry gives rise to unequal output steps upon PSRE turn-on events, namely:

$$\Delta V_o^\uparrow \approx \frac{\tau_{CI} I_{o,SRE}^{ON\uparrow}}{C_L}, \quad \Delta V_o^\downarrow \approx \frac{\tau_{CI} |I_{o,SRE}^{ON\downarrow}|}{C_L}, \tag{16}$$

where ΔV_o^\uparrow and ΔV_o^\downarrow occur at the beginning of low-to-high and high-to-low transitions of V_o , respectively. Nevertheless, both ΔV_o^\uparrow and ΔV_o^\downarrow contribute to reducing the settling time by bringing V_o closer to its steady-state value.

We conclude by noting that larger C_B values improve turn-on performance by increasing voltage steps ΔV_{Gp} and ΔV_{Gn} (9), (14) and increasing τ_{CI} (12). However, as explained in the next section, enlarging C_B in the standard CB-PSRE degrades slew-rate performance.

3.3. Capacitive-Boosting Effects on the Slew Rate

To analyze the impact of C_B on the slew rate (SR), we refer to Figure 4b in the following analysis. During the slewing phase, with $V_i = V_H$ and V_o evolving towards V_H , the output voltage can be expressed as:

$$V_o(t) = V_L + \Delta V_o^\uparrow + \frac{I_{o,SRE}^S}{C_L}(t - t_{ON}) \quad \text{for } t > t_{ON}. \quad (17)$$

This expression incorporates two key approximations: (i) the current $I_{o,SRE}^S$ delivered by the CB-PSRE remains constant during slewing, and (ii) the main OTA contribution is negligible.

During the slewing phase, both Mi1 and Mi3 remain active, with their drain currents comprising two components: the static tail current $(1-\alpha)I_{tail1}$ and the dynamic current I_c flowing through C_B . This second contribution, absent in the original PSRE configuration without CB, originates from the fact that the voltage $V_c(t)$ across C_B evolves together with $V_o(t)$. Notably, as analytically shown in the following, I_c has a detrimental impact on the SR, as it drains a portion of the static tail currents $(1-\alpha)I_{tail1}$, decreasing the current effectively delivered to the output mirrors of the PSRE.

For analytical tractability, we assume constant “effective” gate-source voltages of Mi1 and Mi3 during slewing conditions, denoted as $V_{GS,n}^S$ and $V_{SG,p}^S$, respectively. Section 3.5 eventually validates this approximation through electrical simulations. Under these assumptions, the voltage across C_B results to be equal to:

$$V_c(t) = V_H - V_{GS,n}^S - V_{SG,p}^S - V_o(t). \quad (18)$$

This yields the following dynamic current through C_B :

$$I_c = C_B \frac{dV_c}{dt} = -C_B \frac{dV_o}{dt} = -\frac{C_B}{C_L} I_{o,SRE}^S. \quad (19)$$

The current delivered to the Mm1p-Mm2p mirror equals $2[(1-\alpha)I_{tail1} + I_c]$, hence resulting in the following value for the CB-PSRE output current:

$$I_{o,SRE}^S = 2K[(1-\alpha)I_{tail1} + I_c] \implies I_{o,SRE}^S = \frac{2K(1-\alpha)I_{tail1}}{1 + 2KC_B/C_L}. \quad (20)$$

Comparison of (20) with (2) reveals a reduction factor of the PSRE output current equal to $1/(1 + 2KC_B/C_L)$ with respect to the PSRE without C_B . As anticipated, this negatively impacts the slew rate $SR = I_{o,SRE}^S/C_L$. The degradation factor worsens as either K or C_B increases.

The derivation of (20) implicitly assumes $(1-\alpha)I_{tail1} + I_c > 0$, which holds true if:

$$(1-\alpha)I_{tail1} - \frac{C_B}{C_L} I_{o,SRE}^S > 0 \implies \frac{(1-\alpha)I_{tail1}}{1 + 2KC_B/C_L} > 0, \quad (21)$$

a condition satisfied for all positive values of C_B and K .

We emphasize that this SR degradation uniquely occurs in single-ended CB-PSREs, due to the ramping behavior of $V_c(t)$ during slewing conditions, caused by either V_{sn} or V_{sp} following the output voltage evolution. Conversely, this effect is absent in fully-differential PSRE-assisted OTAs, thanks to common-mode control during differential-mode transients [30].

Finally, it is worth mentioning some additional effects not included in the model of (20). While (20) provides a reasonable approximation at the onset of the slewing phase, the actual available current diminishes towards the end of the transient due to: (i) Mi3 gradually turning off as V_o approaches V_H (because of the tail transistor of the p-type pair, Mtp2, entering the triode region and eventually deactivating, reducing the output current contribution from the p-type input pair); (ii) Mi2 turning on and competing with Mi1 for the tail current; (iii) gradual re-activation of the DTC mechanism for imposing the threshold currents (via Ma2-Msh4a-Msh4 in Figure 2). The last two mechanisms dominate at the slewing phase conclusion, whereas the PSRE leaves control to the main OTA (linear settling phase). On the other hand, the first mechanism may manifest earlier, during the last part of the ramping evolution of V_o , halving $I_{o,SRE}^S$ (and the SR with it) when the output current contribution related to I_3 vanishes [see Figure 4b].

3.4. Input-Common-Mode G_m -Stabilized Single-Stage OTA

The case-study OTA used in this work employs a rail-to-rail single-stage active-mirror topology. Its complete schematic view is shown in Figure 5. To maintain consistent transconductance (G_m) across the full rail-to-rail input common-mode range (ICMR), we implemented a modified G_m -control technique based on [35], which builds upon the approach originally presented in [41].

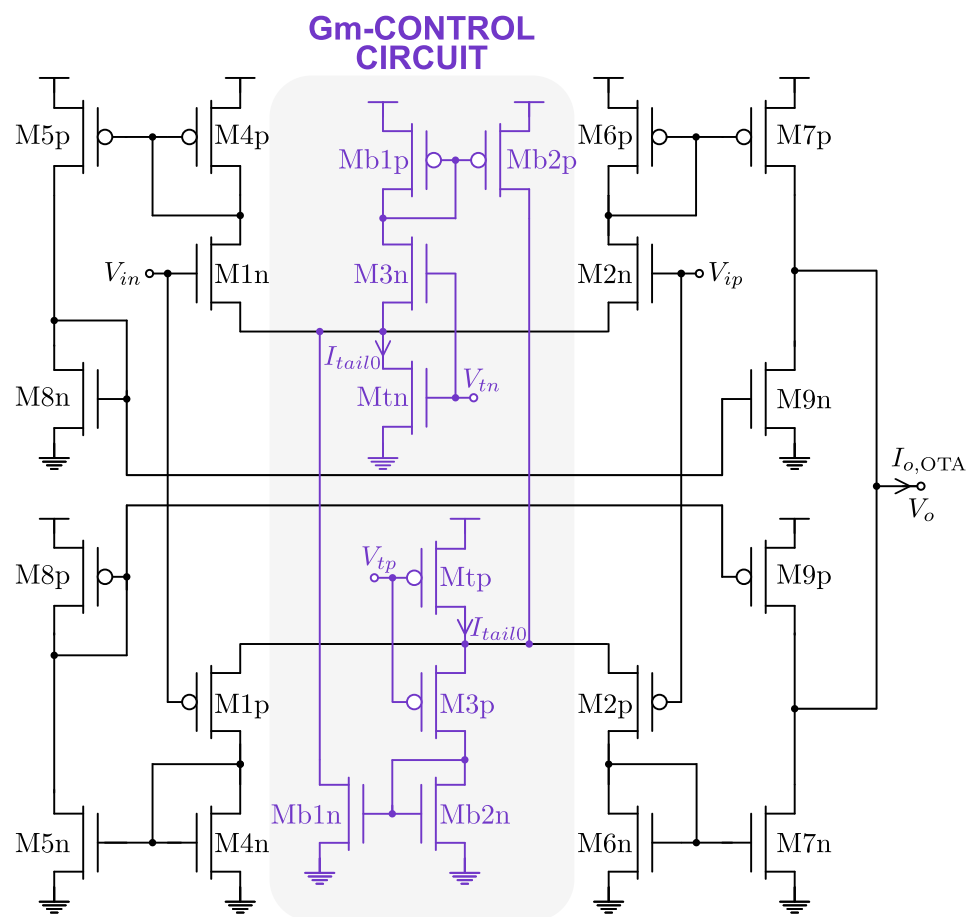


Figure 5. Single-stage single-ended OTA with G_m -control circuit for rail-to-rail input common mode operation.

For mid-range input common-mode voltages ($V_{ic} \approx V_{dd}/2$), both n-type (M1n-M2n) and p-type (M1p-M2p) differential pairs remain active (as their respective supply transistors Mtn and Mtp are biased in saturation) and jointly contribute to the total G_m . In this

condition, transistors M3n and M3p remain off, keeping Mb1p, Mb2p, Mb1n, and Mb2n in the cutoff region.

As V_{ic} approaches either rail (ground or V_{dd}), one differential pair deactivates when its supply transistor enters the triode region. Without compensation, this would typically halve the OTA G_m . The circuit in Figure 2b solves this through complementary compensation.

When $V_{ic} \approx 0$, the n-type pair (M1n-M2n) deactivates due to insufficient V_{DS} across M1n. However, in this condition, M3n activates, injecting current into the Mb1p-Mb2p current mirror. This provides supplemental tail current to the p-type pair (M1p-M2p), beyond the nominal I_{tail0} . Proper sizing of M3n, Mb1p, and Mb2p restores the total G_m to its mid-range value.

Conversely, as V_{ic} approaches V_{dd} , M3p activates the Mb2n-Mb1n path to boost current in the n-type pair. This symmetrical compensation maintains optimal OTA performance across the entire ICMR, particularly minimizing the linear settling phase duration during output transients.

3.5. Simulation Results

Electrical simulations were performed on the PSRE-assisted OTA with the standard CB technique (Figures 2 and 5) using the Spectre simulator with device models from a 0.18- μm CMOS process by UMC. The design, with device parameters detailed in Tables 1 and 2, targets LCD-driving applications with 1-nF load capacitance. I/O transistors (3.3-V supply) and metal-insulator-metal (MIM) capacitors were employed, with the OTA consuming 2.4 μA in quiescent conditions and the PSRE 1.6 μA . The PSRE was configured with current gain $K = 600$ in its output current mirrors and DTC parameters $\alpha = 1/4$ and $J = 12$, achieving 1% settling time below 10 μs upon input swings between 10% and 90% of V_{dd} . All of the simulations discussed in this section were performed in the typical process corner at room temperature ($T = 27^\circ\text{C}$).

To determine transistor sizes in Tables 1 and 2, we employed well-known intuitive guidelines that are typically used in most OTA designs. Notably, these considerations apply to both the main OTA and the PSRE block, since even the PSRE architecture closely resembles an OTA. Specifically, input-pair transistors have been sized so that to be biased in moderate/weak inversion, to maximize the g_m/I_D parameter, hence optimising transconductance and GBW for the given current budget. On the other hand, current-mirror transistors are biased in strong inversion, to reduce their noise and mismatch impact, with overdrive voltages below 200 mV to simultaneously achieve wide ICMR and output swing.

PSRE parameters α , J and K have been chosen based on parametric sweep simulations, taking into account their role in the following trade-offs: (i) smaller α maximizes the fraction of PSRE quiescent current employed to generate large output current in slewing conditions, but excessively small α might cause excessive delays in the DTC mechanism, possibly degrading settling time; (ii) J is bounded to verify $\alpha J > 1 - \alpha$, to correctly enforce the PSRE deadzone (as discussed in Section 2), but excessive J might also cause delayed DTC action; (iii) larger K increases the maximum PSRE output current, but exacerbates the tail current draining effect due to standard CB in the single-ended PSRE (studied in this work for the first time), on top of worsening the turn-on/turn-off delays of the PSRE, as discussed in [40].

Table 1. Device sizes for the PSRE block.

Device	Width (μm)	Length (μm)	Multiplicity
n-type section			
Mi1, Mi2	1.5	2.5	1
Ma1, Ma2	0.24	2.5	1
Mtn0, Mtn1, Mtn2	0.5	2.5	4, 4, 1
Msh3a, Msh3, Msh4a, Msh4	0.96	1.36	1, 12, 1, 12
Mm1p, Mm2p, Mm3p, Mm4p	0.48	0.68	1, 600, 1, 1
p-type section			
Mi4, Mi3	1.5	2.5	4
Ma4, Ma3	0.24	2.5	4
Mtp0, Mtp1, Mtp2	0.5	2.5	16, 16, 4
Msh1a, Msh1, Msh2a, Msh2	0.96	1.36	1, 12, 1, 12
Mm1n, Mm2n, Mm3n, Mm4n	0.48	0.68	1, 600, 1, 1

Table 2. OTA device sizes.

Device	Width (μm)	Length (μm)	Multiplicity
n-type section			
M1n, M2n	12	2	1
Mtn	0.75	2.5	5
M4p, M5p, M6p, M7p	2	10	4, 4, 4, 48
M8n, M9n	2	10	12
p-type section			
M1p, M2p	12	2	4
Mtp	0.75	2.5	20
M4n, M5n, M6n, M7n	2	10	1, 1, 1, 12
M8p, M9p	2	10	48
G_m -control circuit			
M3n	0.57	8	2
Mb1p, Mb2p	1.5	8	2, 8
M3p	0.62	8	8
Mb2n, Mb1n	0.34	8	2, 8

Figure 6 illustrates the competing effects of capacitive boosting during low-to-high transients [Figure 6a] and high-to-low transients [Figure 6b]. Small C_B values effectively eliminate the PSRE turn-on delay, replacing it with an initial voltage step. However, they simultaneously reduce the slew rate during the main slewing phase, as predicted by (20). The net effect on settling time depends on which phenomenon dominates. Furthermore,

focusing on the low-to-high transients of Figure 6a, we observe that when the output voltage exceeds ~ 2.6 V, the p-type pair deactivates, creating a secondary reduced slewing regime before the final linear settling phase, where the OTA operates alone. This effect has been discussed in the conclusion of Section 3.3.

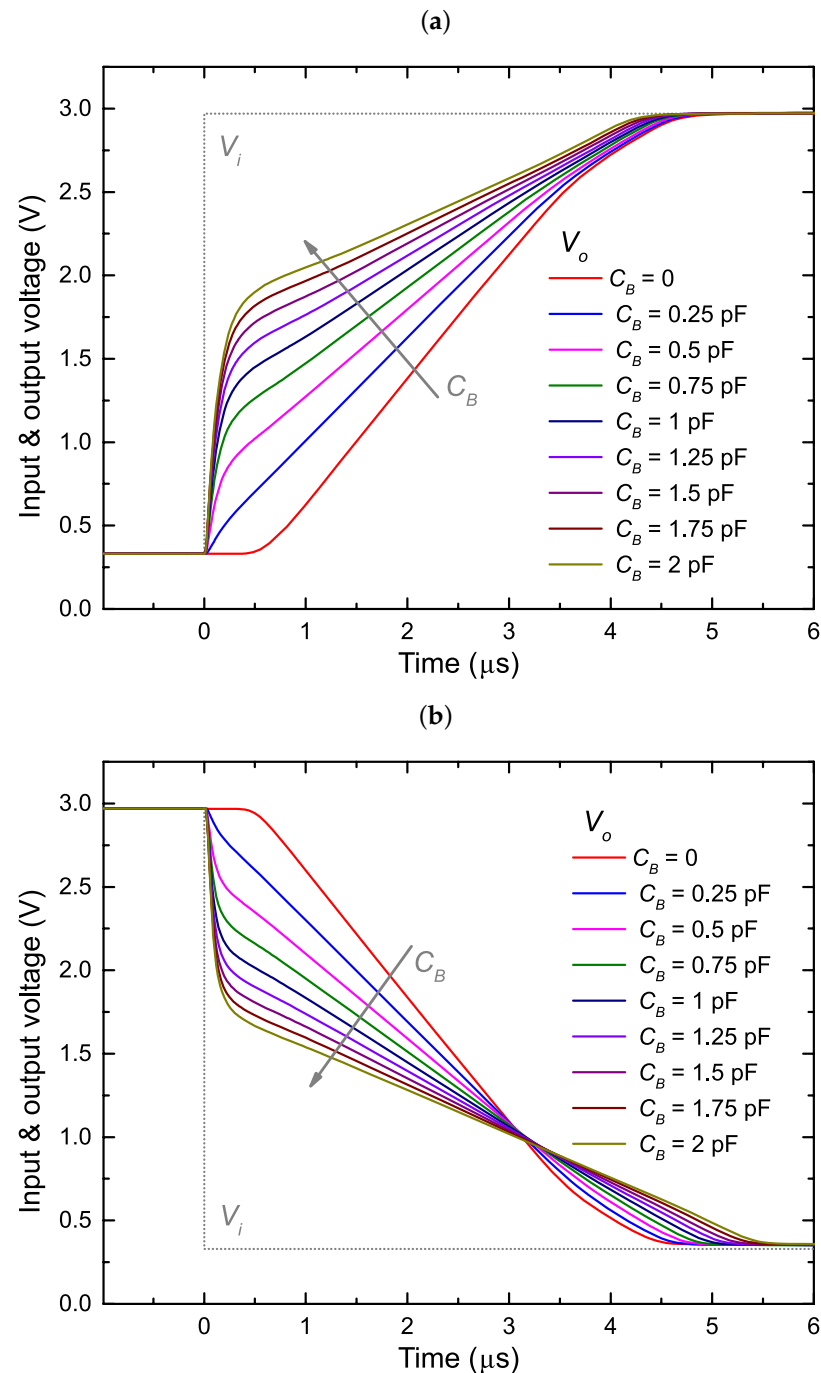


Figure 6. Standard CB technique: input and output voltage as a function of time at the low-to-high transient (a) and high-to-low transient (b), plotted for different values of capacitor C_B .

For the simulated design, settling time marginally improves with increased C_B at low-to-high transients, while it seriously worsens with C_B at high-to-low transients. These effects are highlighted in Figure 7, showing SR and settling time as a function of C_B . As previously anticipated, this asymmetry, occurring despite balanced transconductance factors of PMOS and NMOS transistors, is due to PMOS-NMOS threshold voltage differences, causing unequal current boosting during opposite transitions, as predicted by (10), (15)

and (16). This polarity-dependent behavior reveals that the standard CB technique is not effective when used for single-ended structures.

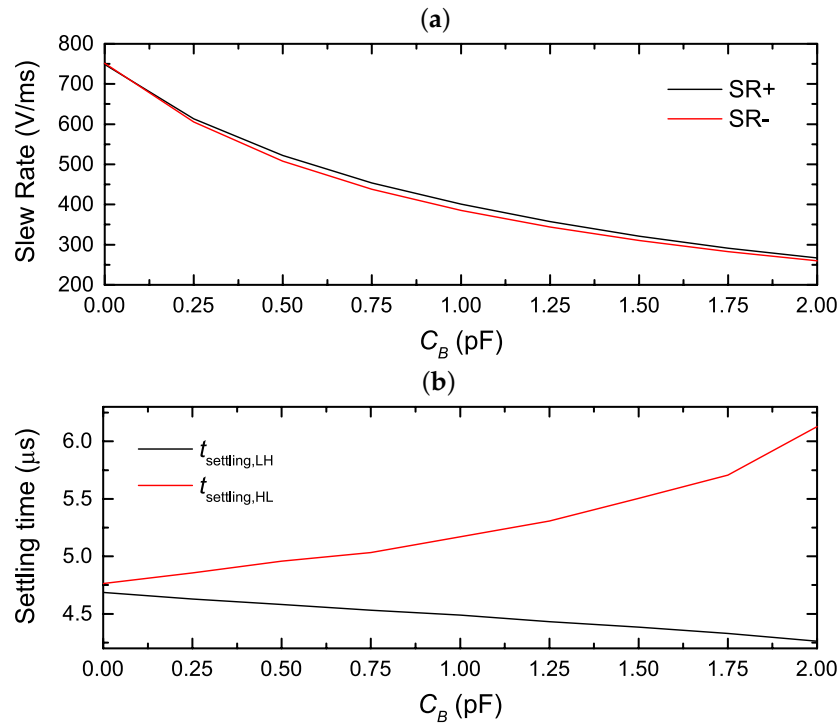


Figure 7. Standard CB technique: (a) Positive and negative slew rate as a function of C_B . (b) 1% settling time as a function of C_B at the low-to-high (LH) and high-to-low (HL) transients.

Figures 8 and 9 provide detailed validation of the analytical models presented in Sections 3.2 and 3.3. Figure 8 shows voltages V_{cb} , V_{sp} and V_{sn} across a whole low-to-high transient. V_{sn} and V_{sp} exhibit the predicted behavior [Figure 8a]: V_{sn} rapidly settles to $V_H - V_{GS,n}^S$ at the input voltage step, while V_{sp} tracks the output voltage as $V_o + V_{SG,p}^S$. The resulting evolution of the voltage across C_B , shown in Figure 8b, matches our theoretical predictions, giving rise to the dynamic current I_c (19), which lowers the SR (20).

Figure 9 shows other relevant PSRE internal voltages during the low-to-high transient. Specifically, traces marked as $V_{GS,Mi1}$, $V_{DS,Mi1}$ and V_{Gp} correspond to the gate-source voltage of Mi1, drain-source voltage of Mi1 and gate voltage of Mm1p-Mm2p, while the voltage across C_B and the input and output voltages are also plotted for reference. Interestingly, in the magnified view of Figure 9b, it appears evident how, at the very beginning of the transient, during the PSRE turn-on process, the input transistor Mi1 finds itself to shortly work in the triode region ($V_{DS,Mi1} = 120 \text{ mV} \ll V_{GS,Mi1} - V_{th,n} \approx 1 \text{ V}$), while the output transistor Mm2p markedly reaches strong inversion, thanks to the large ΔV_{Gp} step. These findings validate the analytical model proposed in Section 3.2 to describe the CB-assisted PSRE turn-on process.

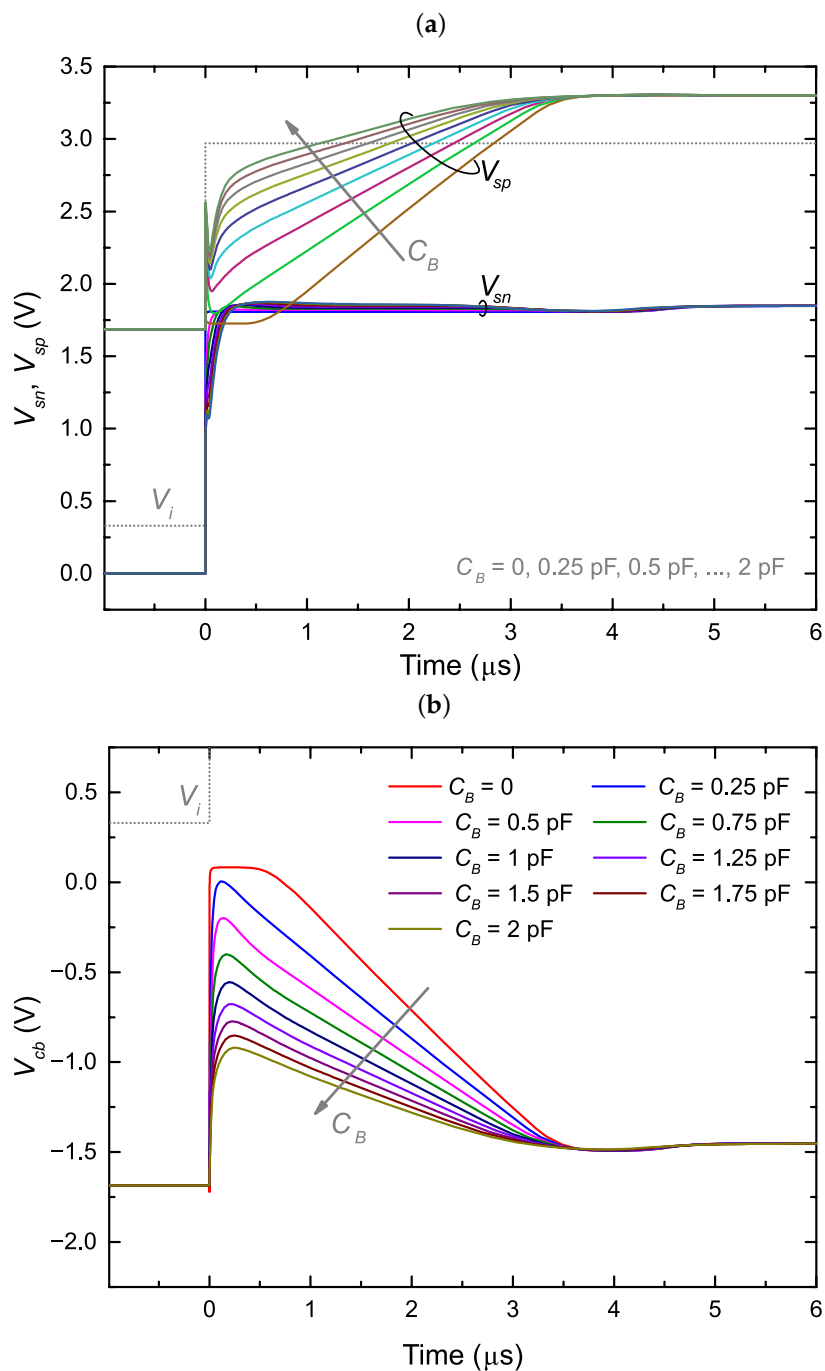


Figure 8. Internal nodes waveforms during the low-to-high transient: (a) Source voltages of the PSRE input differential pairs as a function of time at the low-to-high transient, plotted for different values of capacitor C_B . (b) Voltage across C_B as a function of time at the low-to-high transient for different values of capacitor C_B .

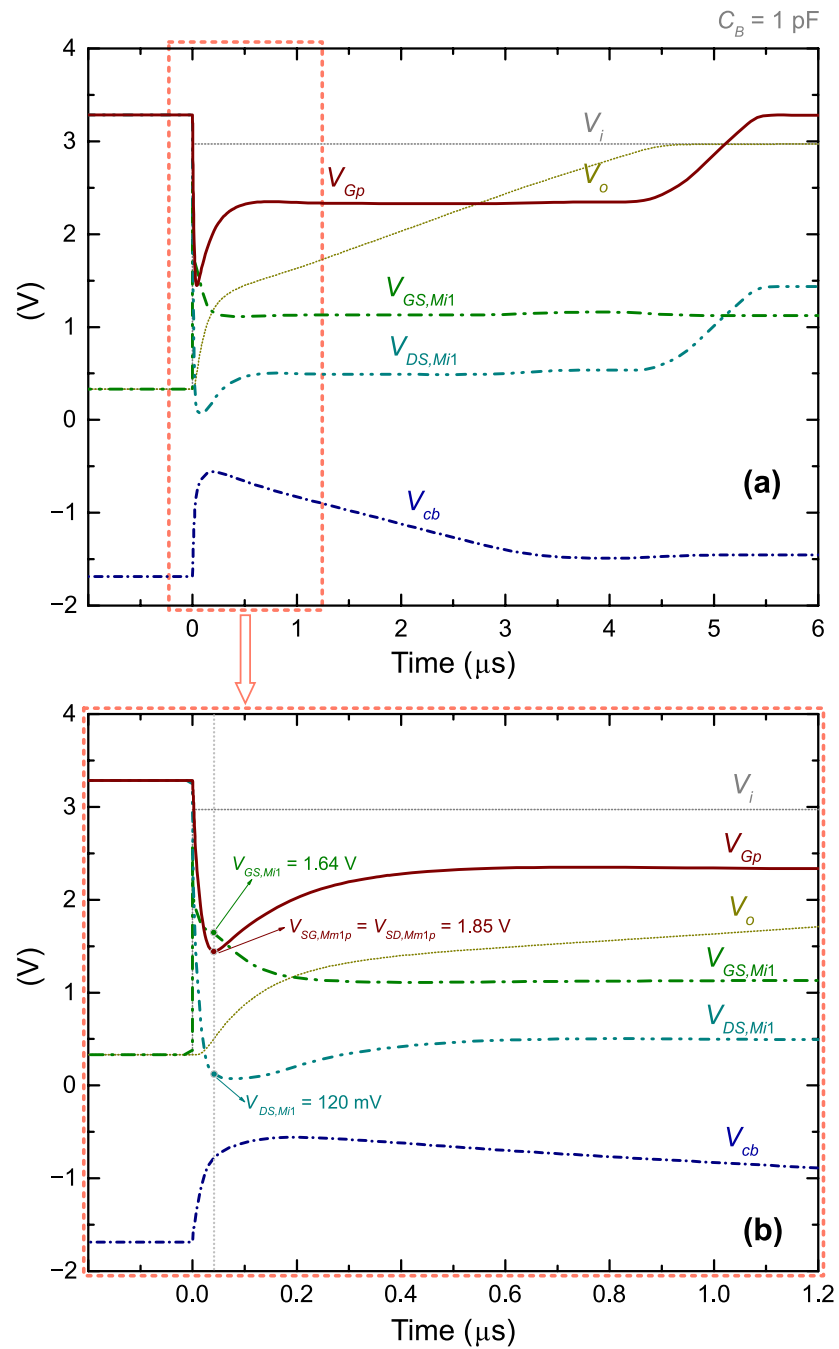


Figure 9. Internal nodes waveforms during the low-to-high transient: gate-source and drain-source voltages of the n-type input transistor, $V_{GS,Mi1}$ and $V_{DS,Mi1}$, gate voltage of Mm1p-Mm2p, V_{Gp} , and voltage across C_B , V_{cb} . For reference purposes, the input and output voltages are also shown, indicated as V_i and V_o , respectively. The employed C_B value is 1 pF. (a) Entire low-to-high transient. (b) Turn-on phase of the CB-PSRE.

4. Efficient Capacitively-Boosted Single-Ended Parallel-Type Slew-Rate Enhancer

This section presents a modified capacitive boosting technique that addresses the slew-rate reduction issues identified earlier. The proposed solution, shown in Figure 10, splits the original boosting capacitor C_B into two separate components: C_{Bn} , connected between V_{sn} and ground, and C_{Bp} , connected between V_{sp} and V_{dd} . We refer to this configuration as the *split CB* (SCB) technique.

where C_{Gn}^* and $C_{GS,Mix}$ indicate the input capacitance of current mirror Mm3n-Mm4n and the gate-source capacitance of transistor Mix, respectively. For high-to-low transitions, complementary analysis yields the following voltage variation at the gate of Mm1n-Mm2n:

$$\Delta V_{Gn} = \frac{C_{Bp} (V_{dd} - V_L + V_{SG,p}^{ON})}{C_{Gn} + C_{GS,Mi4}} + \frac{C_{Bn} (V_{GS,n}^Q - V_{GS,n}^{ON})}{C_{Gn} + C_{Gp}^*} \frac{C_{Gp}^*}{C_{Gp}^* + C_{GS,Mi2}}, \quad (25)$$

where C_{Gp}^* is the input capacitance of current mirror Mm3p-Mm4p. When $C_{Bn} = C_{Bp} = 2C_B$, these results resemble (9) and (14) related to the standard CB technique described in Section 3.2. Hence, similar ΔV_o^\uparrow and ΔV_o^\downarrow quantities can be obtained for the SCB-PSRE (16), preserving the benefits of a fast turn-on effect.

However, the SCB-PSRE behavior significantly differs from that of the standard CB-PSRE during the slewing phase. In that condition, V_{sn} stabilizes at the constant voltage level $V_H - V_{GS,n}^S$. It is worth noting that, since the bottom terminal of C_{Bn} is tied to ground, this prevents any dynamic current flowing through C_{Bn} , allowing the whole tail current of the n-type differential pair, $(1 - \alpha)I_{tail1}$, to reach the Mm1p-Mm2p current mirror. The dynamic draining effect of the tail current highlighted for the standard CB configuration only persists in the p-type pair, since V_{sp} follows the output voltage evolution as $V_{sp}(t) = V_{SG,p}^S + V_o(t)$, generating a negative current through C_{Bp} :

$$I_{cp} = -C_{Bp} \frac{dV_o}{dt} = -\frac{C_{Bp}}{C_L} I_{o,SRE}^{S+}, \quad (26)$$

where $I_{o,SRE}^{S+}$ indicates the output current during the slewing phase for low-to-high transitions. The drain current of Mi3, I_3 , consequently becomes:

$$I_3 = (1 - \alpha)I_{tail1} - \frac{C_{Bp}}{C_L} I_{o,SRE}^{S+}. \quad (27)$$

The current mirror Mm3n-Mm4n only conducts when $I_3 > 0$, leading to two operational regimes of the SCB-PSRE:

$$I_{o,SRE}^{S+} = \begin{cases} \frac{2K(1 - \alpha)I_{tail1}}{1 + KC_{Bp}/C_L} & (I_3 > 0); \\ K(1 - \alpha)I_{tail1} & (I_3 = 0). \end{cases} \quad (28)$$

Within the first regime, the negative effect of dynamic currents through CB elements still partially persists, even though it is less relevant than in the standard CB scheme, as it only affects the output current contribution originating from the p-type pair, rather than both pairs. On the other hand, in the second regime, the PSRE output current and, hence, the SR become independent from CB elements. The transition between these regimes—found elaborating (27) and (28)—occurs when:

$$I_3 = 0 \implies C_{Bp} \geq C_L/K. \quad (29)$$

This represents the key advantage of the SCB-PSRE over the CB-PSRE. When condition (29) is satisfied, only the n-type pair contributes to $I_{o,SRE}^{S+}$, allowing for effective SR improvement by enlarging K . At the same time, the CB advantages occurring at the PSRE turn-on are preserved. For $C_L = 1$ nF and $K = 600$, the condition in (29) requires $C_{Bp} \geq 1.67$ pF.

Similarly, the behavior at high-to-low transitions follows the following equations:

$$I_{o,SRE}^{S-} = \begin{cases} \frac{2K(1-\alpha)I_{tail1}}{1 + KC_{Bn}/C_L} & (C_{Bn} < C_L/K); \\ K(1-\alpha)I_{tail1} & (C_{Bn} \geq C_L/K). \end{cases} \quad (30)$$

It is also worth noting that the output current value of $K(1-\alpha)I_{tail1}$, achieved in the second operating regime, is the same that is obtained around the end of the slewing phase, when one differential pair turns off regardless of $C_{Bp,n}$ due to V_o closely approaching its steady-state value. Therefore, admittedly, satisfying (29) leads to non-maximum SR (as far as the SR dependence on $C_{Bp,n}$ is concerned); however, the problematic dependence of $I_{o,SRE}^{S-}$ on C_B affecting the standard CB approach is removed, allowing for arbitrary increase of the initial V_o jumps (by increasing $C_{Bp,n}$ and/or K) without any penalty on the SR. The SR itself can also be directly increased by acting on K , at least until slow-turn-off effects arise, as described in [40].

4.2. Simulation Results

Performances of the proposed SCB-PSRE were evaluated using the same 0.18- μm CMOS implementation described in Tables 1 and 2, with split capacitors C_{Bp} and C_{Bn} replacing the standard C_B . We assigned equal values to both capacitors: $C_{Bp} = C_{Bn} = C'_B$. The circuit was simulated in unity-gain configuration with $C_L = 1$ nF, $K = 600$, and supply currents of 2.4 μA (OTA) and 1.6 μA (PSRE), under typical conditions (3.3 V, 27 °C).

Figures 11a,b illustrate the SCB-PSRE operation during low-to-high and high-to-low transitions, respectively. For small C'_B values, the output slope decreases according to (28) and (30), while maintaining the beneficial initial boosting effect. When C'_B exceeds ~ 1.25 pF, the slope becomes constant as predicted by (28) and (30), with only one differential pair contributing current during the whole transient, while the tail current of the other differential pair is entirely drained by the dynamic current flowing through its related CB element. Isofar, a limit is set to the SR degradation phenomenon seen with the standard CB technique, while settling time remarkably decreases as a function of C'_B , thanks to increased initial V_o steps. However, excessive C'_B (> 2.25 pF) eventually causes overshoot, due to delayed PSRE turn-off. The delayed turn-off of the PSRE causes excess output current into C_L , eventually degrading the settling time (t_{settling}). A similar phenomenon has been analyzed in [40].

Figure 12a shows the expected SR behavior: after an initial decrease with C'_B , SR stabilizes when condition (29) is met; the dashed lines confirm this by showing the SR obtained when the contribution of the differential pair affected by tail current draining is entirely removed (i.e., by removing transistors Mm4p-Mm4n in Figure 10). Corresponding settling time improvements are shown in Figure 12b, where both transition polarities clearly benefit from increased C'_B beyond 1.25 pF.

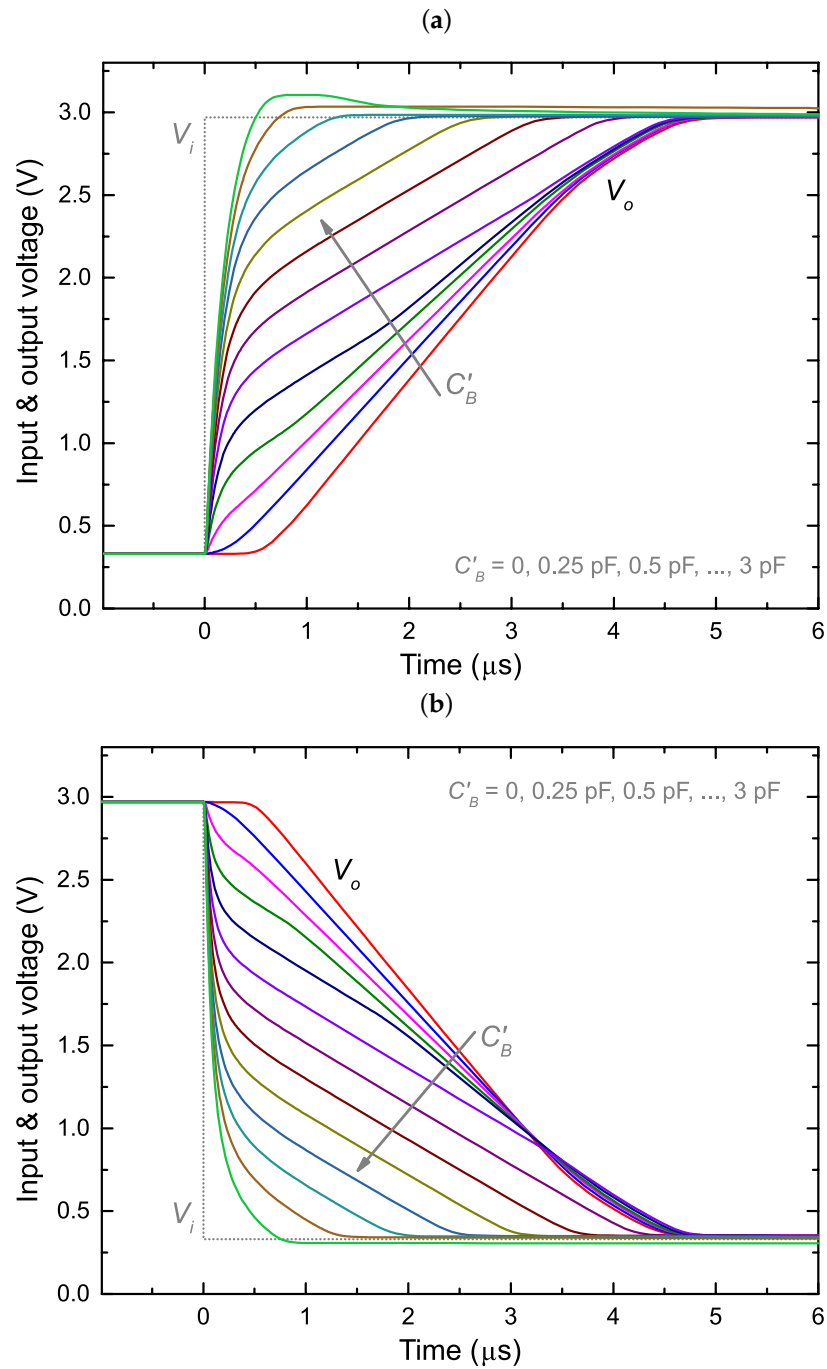


Figure 11. Split CB technique: input and output voltage as a function of time at the low-to-high transient (a) and high-to-low transient (b), plotted for different values of capacitor $C'_B = C_{Bn} = C_{Bp}$.

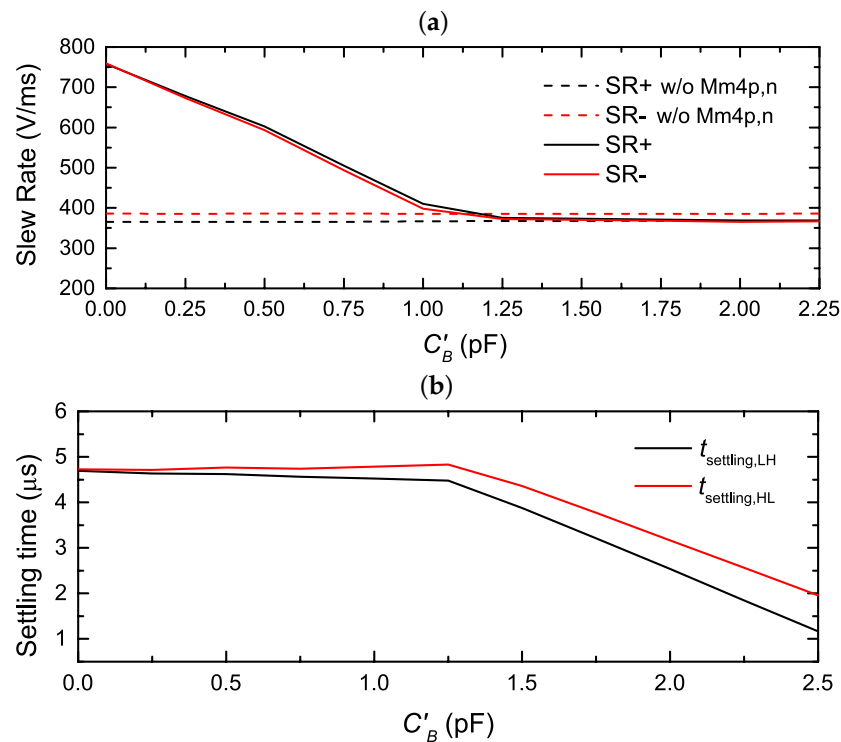


Figure 12. Split CB technique: (a) Positive and negative slew rate as a function of C'_B with the novel proposed technique. For reference purposes, traces obtained without transistors Mm4p and Mm4n of Figure 10 are also shown (dashed lines). (b) 1% settling time as a function of C'_B at the low-to-high (LH) and high-to-low (HL) transients.

5. Results and Discussion

In this section, performances of the proposed SCB-PSRE-assisted OTA are showcased. In this set of simulations, performed with the Spectre simulator using device models from a 0.18- μ m CMOS process by the UMC foundry, the PSRE and OTA blocks were implemented using the same device sizes of Tables 1 and 2, respectively, and were supplied with static currents equal to 1.6 μ A and 2.4 μ A, respectively. The C_{Bp} and C_{Bn} capacitors included in the SCB-PSRE scheme (Figure 10) were set equal to 2.25 pF each. According to the parametric sweep simulations of Figures 11, that is the highest capacitance value avoiding overshoot phenomena, hence corresponding to optimum settling behavior. Unless differently specified, simulations were performed at room temperature ($T = 27$ $^{\circ}$ C) with $V_{dd} = 3.3$ V in the typical process corner. Performances of the SCB-PSRE are first compared to prior PSRE implementations; then, they are benchmarked against previously published works on fast-settling drivers.

Figure 13 shows output voltage transients obtained in response to both low-to-high and high-to-low input voltage transitions. The following designs have been tested: (i) the OTA alone, (ii) the PSRE-assisted OTA with the standard CB technique (Figure 2), with $C_B = 4.5$ pF, and (iii) the PSRE-assisted OTA with the novel SCB technique. All three circuits were designed with a total quiescent supply current of $I_{sup,Q} = 4$ μ A and were arranged in unity-gain configuration. The load capacitor was set equal to $C_L = 1$ nF, while the input steps span from 10% to 90% of V_{dd} . The first design, only including the OTA of Figure 5, exhibits very inefficient driving capability, requiring around 400 μ A to settle to the steady-state output voltage. Conversely, the addition of the PSRE block, under the same total $I_{sup,Q}$, remarkably improves settling speed, especially with the novel SCB technique, achieving both low-to-high and high-to-low 1% settling times (indicated as $t_{\text{settling,LH}}$ and $t_{\text{settling,HL}}$ in the following) below 3 μ s.

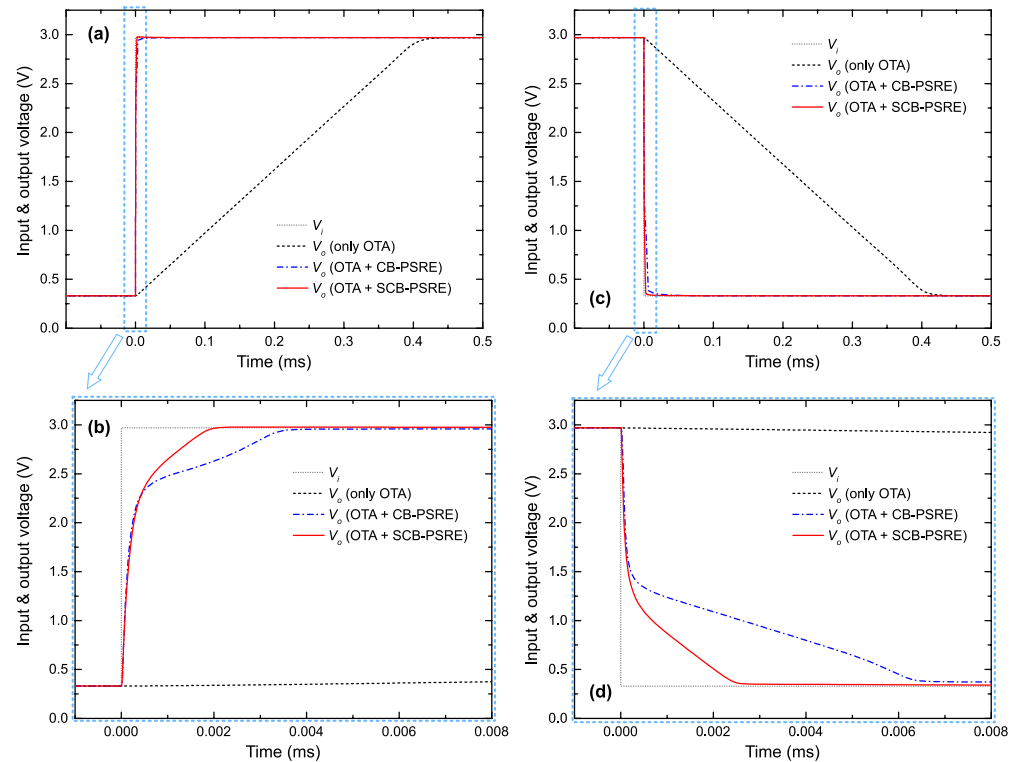


Figure 13. Response to square-wave stimulus (unity-gain configuration, $C_L = 1$ nF). The proposed SCB-PSRE-assisted OTA is compared with its previous versions, all designed with the same quiescent supply current of $4 \mu\text{A}$. The CB-PSRE and SCB-PSRE solutions have been implemented with $C_B = 4.5$ pF and $C_{Bp} = C_{Bn} = 2.25$ pF, respectively. (a,b) Transient waveforms around low-to-high input transition. (c,d) Transient waveforms around high-to-low input transitions.

In Figure 14, the same three designs are tested under sinusoidal stimuli, again in unity-gain configuration with a load capacitance of 1 nF. Specifically, Figure 14a shows the waveforms obtained when the input signal is generated with 2-kHz frequency and peak-to-peak amplitude equal to $2 V_{pp}$. While the OTA alone is unable to correctly follow the input signal, due to clear SR limitations giving rise to a triangle-wave output, the PSRE-assisted OTA correctly tracks V_i , with only small discrepancies before sine-wave peaks due to PSRE turn-off events. Figure 14b–d show total harmonic distortion (THD), peak-to-peak amplitude, and average consumption, respectively, as a function of frequency, while the input sine-wave amplitude is kept equal to $2 V_{pp}$. While the OTA alone incurs THD and amplitude degradation just above 1 kHz, the PSRE-assisted designs achieve more limited THD increase as a function of frequency, while the amplitude is roughly kept constant. As expected, no significant differences can be noticed, in this simulation, between the CB-PSRE and the SCB-PSRE designs, since the SCB technique is primarily meant to optimize responses to fast input voltage steps, rather than gradual, continuous variations of V_i as encountered with a sinusoidal stimulus. It is also worth noting that, while all designs were supplied with the same total quiescent current, the average dynamic consumption of the PSRE block increases as a function of frequency, as made evident in Figure 14d; however, this portion of consumption is entirely employed to drive the load capacitance during slewing transients. Hence, this effect highlights how the PSRE block allows efficient automatic adjustment of the average consumption depending on the load current requirement.

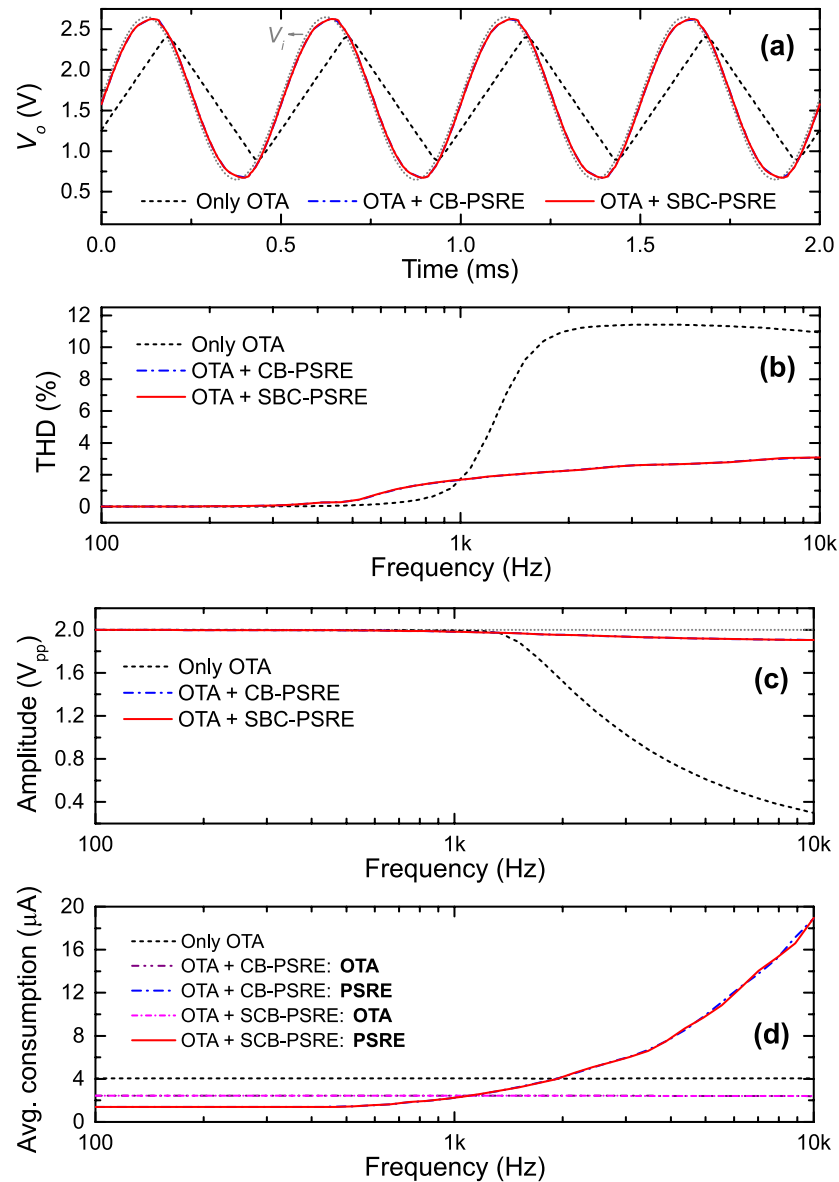


Figure 14. Response to sinusoidal stimulus (unity-gain configuration, $C_L = 1$ nF). The proposed SCB-PSRE-assisted OTA is compared with its previous versions, all designed with the same quiescent supply current of $4 \mu\text{A}$. The CB-PSRE and SCB-PSRE solutions have been implemented with $C_B = 4.5$ pF and $C_{Bp} = C_{Bn} = 2.25$ pF, respectively. (a) Waveforms at 2-kHz sine-wave frequency. (b) Total harmonic distortion as a function of sine-wave frequency. (c) Peak-to-peak amplitude as a function of sine-wave frequency. (d) Average current consumption as a function of sine-wave frequency.

Table 3 compares the SCB-PSRE against alternative implementations. In all PSRE-assisted OTA solutions, the OTA and PSRE blocks have quiescent supply currents equal to $2.4 \mu\text{A}$ and $1.6 \mu\text{A}$, respectively. Using $C'_B = 2.25$ pF, the proposed SCB-PSRE-assisted OTA achieves $\times 5.53$ lower settling time than the standard CB-PSRE, and a $\times 162$ settling time improvement over the standalone OTA with the same quiescent supply current. In terms of SR, the proposed SCB-PSRE improves over the standard CB-PSRE by 2.44 times.

Static parameters are also reported in Table 3 for all designs, including frequency-response parameters (i.e., DC gain, gain-bandwidth product and phase margin, indicated as A_0 , GBW and PM, respectively), common-mode rejection-ratio (CMRR) characteristics (i.e., the CMRR value in DC and its -3 dB bandwidth, indicated as CMRR_{DC} and BW_{CMRR} , respectively), integrated noise, and standard deviation of the input-referred offset (σ_{io}). Offset has been evaluated through sets of 500 statistical Monte Carlo simulations, including

both global and local (mismatch) process errors. All of these parameters are not affected by the presence of the PSRE block, proving correct turn-off of the PSRE output devices at the steady state, where only the main OTA operates.

Table 3. Performance comparison between the proposed SCB-PSRE-assisted OTA and its previous versions.

	Only OTA		OTA & PSRE ($C_B = 0$)	OTA & CB-PSRE ($C_B = 4.5$ pF)	OTA & SCB-PSRE ($C'_B = 2.25$ pF)
$I_{sup,Q}$ (μ A)	2.43	4.04	4.03	4.03	4.03
SR_+ (V/ms)	3.90	6.47	758	151	369
SR_- (V/ms)	3.89	6.46	760	146	367
$t_{settling,LH}$ (μ s)	683	414	4.69	3.49	1.84
$t_{settling,HL}$ (μ s)	680	410	4.73	14.2	2.56
A_0 (dB)	64.6	65.2	64.6	64.6	64.6
GBW (kHz)	7.32	11.7	7.32	7.32	7.32
PM ($^\circ$)	85.3	84.4	85.3	85.3	85.3
CMRR_{DC} (dB)	111	113	111	111	111
BW_{CMRR} (kHz)	1.02	1.26	1.02	1.02	1.02
Noise * (μ V _{RMS})	20.5	18.4	20.5	20.5	20.5
σ_{io} (mV)	1.97	1.91	1.97	1.97	1.97

* Integrated noise in 0.1–10 Hz, referred to the input.

Table 4 summarizes the performances of the SCB-PSRE-assisted OTA across mixed PVT corners. Good resilience to PVT variations is demonstrated, with all key parameters (SR, settling time, DC gain, GBW, and phase margin) showing minimal deviations from typical conditions.

Layout parasitic components (not taken into account in this work) are expected to have relevant consequences mainly concerning the choice of optimal C'_B . Specifically, considering that the PSRE output mirrors Mm1p-Mm2p and Mm1n-Mm2n have output devices with large multiplicity factors ($K = 600$), their input capacitances are likely to be higher due to routing capacitances. However, rather than disrupting the PSRE performance, this would simply require an adjustment of the C'_B value to achieve optimal transient waveforms (specifically, referring to Figure 11 selecting the fastest rising/falling behavior not presenting any overshoot).

Finally, in Table 5, the performances of the proposed design are thoroughly compared against recent state-of-the-art solutions implemented with 0.18- μ m CMOS technologies. All compared designs are single-ended amplifiers driving large capacitive loads. To allow fair comparisons, two key figures of merit are employed: the settling-time figure of merit ($FoMT = C_L / (t_{settling} \times Power)$) and the normalized charge efficiency ($FoMN = C_L \Delta V_i / (t_{settling} I_{sup})$) [42,43]. The proposed SCB-PSRE achieves competitive performance with $FoMT = 29.6$ pF $\cdot\mu$ s $^{-1}\cdot\mu$ W $^{-1}$ and $FoMN = 0.258$ while driving a 1 nF load with just 4 μ A current consumption. These results represent significant improvement over our previous work [35] and compare favorably with other implementations, particularly considering the large input swing (80% of V_{dd}) used in our simulations.

Table 4. Performance of the SCB-PSRE-assisted OTA across process-voltage-temperature (PVT) corners: TT (typical-typical), SS (slow-slow), FF (fast-fast), SNFP (slow NMOS-fast PMOS), and FNFP (fast NMOS-slow PMOS).

PVT Corner			$I_{sup,Q}$ (μ A)	A_0 (dB)	GBW (kHz)	PM ($^\circ$)	SR ₊ (V/ms)	SR _− (V/ms)	$t_{settling,LH}$ (μ s)	$t_{settling,HL}$ (μ s)
TT	3.3 V	27 $^\circ$ C	4.03	64.6	7.32	85.3	369	367	1.84	2.56
SS	3 V	0 $^\circ$ C	3.99	64.1	7.48	85.6	371	367	2.18	3.37
SS	3 V	70 $^\circ$ C	3.99	65.1	6.51	85.6	393	371	2.04	3.72
SS	3.6 V	0 $^\circ$ C	4.03	64.3	7.58	85.5	367	370	1.81	2.78
SS	3.6 V	70 $^\circ$ C	4.03	65.3	6.61	85.5	383	376	1.71	2.88
FF	3 V	0 $^\circ$ C	4.03	64.1	7.84	85.0	359	362	1.93	2.53
FF	3 V	70 $^\circ$ C	4.02	65.0	6.82	85.0	370	365	1.81	2.47
FF	3.6 V	0 $^\circ$ C	4.06	64.1	7.96	85.0	360	366	1.64	2.33
FF	3.6 V	70 $^\circ$ C	4.05	65.2	6.92	85.0	351	368	1.52	2.27
SNFP	3 V	0 $^\circ$ C	4.01	64.1	7.64	85.3	361	364	2.18	2.72
SNFP	3 V	70 $^\circ$ C	4.01	65.1	6.65	85.3	376	367	2.04	2.68
SNFP	3.6 V	0 $^\circ$ C	4.05	64.2	7.75	85.3	361	368	1.83	2.50
SNFP	3.6 V	70 $^\circ$ C	4.04	65.2	6.75	85.3	371	370	1.72	2.45
FNFP	3 V	0 $^\circ$ C	4.02	64.1	7.66	85.3	367	365	1.97	2.80
FNFP	3 V	70 $^\circ$ C	4.01	65.1	6.67	85.3	386	369	1.86	2.64
FNFP	3.6 V	0 $^\circ$ C	4.05	64.2	7.77	85.3	369	368	1.62	2.53
FNFP	3.6 V	70 $^\circ$ C	4.04	65.2	6.76	85.3	358	375	1.55	2.50

Table 5. State-of-the-art comparison with designs implemented in 0.18- μ m CMOS.

	This Work	Gambhir 2017 [6]	Wen 2022 [4]	Beloso 2023 [13]	Gagliardi 2023 [35]
Result type	Simulated	Simulated	Measured	Measured	Simulated
V_{dd} (V)	3.3	3.0	5.0	1.0	3.3
$I_{sup,Q}$ (μ A)	4.0	17.0	3.0	2.9	4.0
P (μ W)	13.2	50.9	15.0	2.9	13.2
C_L (nF)	1.00	1.00	1.00	0.16	1.00
$\Delta V_i/V_{dd}$ (%)	80	55	80	54	80
SR (V/ μ s)	0.367	2.372	4.760	0.058	0.752
$t_{settling}$ (μ s)	2.56	0.95	1.18	17.30	4.69
FoMT (pF· μ s ^{−1} · μ W ^{−1})	29.6	20.7	56.5	3.2	16.2
FoMN	0.258	0.103	1.130	0.002	0.141

While the class-B implementation in [4] demonstrates superior figures of merit through its innovative resistive compensation technique, our approach maintains important advantages in design simplicity and compliance with standard class-A OTAs. The SCB technique proves particularly valuable for display driver applications and switched-capacitor circuits,

where it enables fast settling (2.56 μs) with modest power consumption (13.2 μW) and symmetrical performance for both rising and falling edges.

6. Conclusions

This work has presented an improved split capacitive-boosting (SCB) technique for single-ended parallel-type slew-rate enhancers (PSREs). This technique overcomes the key limitation encountered when conventional capacitive boosting approaches are used in single-ended configurations: the slew-rate degradation, due to CB itself, originating from large common-mode voltage variations at internal nodes of the PSRE. By strategically splitting the boosting capacitor into two separate components (C_{Bn} and C_{Bp}), connected to ground and the supply rail, respectively, the proposed technique maintains the beneficial turn-on acceleration while minimizing the detrimental effects on the slew rate. Electrical simulations of a 0.18- μm CMOS design demonstrate the effectiveness of this approach, showing a $5.53\times$ reduction in settling time compared to standard CB-PSRE implementations, along with excellent robustness to process-voltage-temperature variations.

Several promising research directions emerge from this work. First, the SCB technique could be combined with advanced compensation methods, such as those presented in [4], for further performance enhancement. Second, low-voltage implementations could be developed for emerging IoT and wearable applications. Third, the approach could be integrated with OTAs employing class-AB or class-B output stages for additional efficiency improvements. The modular and scalable nature of the SCB-PSRE architecture makes it adaptable to a wide range of analog design contexts, offering a practical and effective solution for slew-rate enhancement without compromising power efficiency or design simplicity.

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