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Feasibility of Physical Unclonable Functions from Pre-stressed Organic Thin Film Transistors for Secure Microelectronics

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ABSTRACT

Pre-stressed commercial Organic Thin Film Transistors (OTFT) have been characterized to evaluate their suitability for Physical Unclonable Functions (PUFs) implementation, when the variability of the drain current (I_D) is used as entropy source. Different kinds of electrical pre-stresses have been considered, to study their impact on the PUF reproducibility. Uniqueness and Uniformity of the resulting PUFs have also been evaluated. The proposed pre-stressed OTFTs based PUFs show a reproducibility up to 0.99, with a uniformity and uniqueness of 0.52 and 0.50, respectively.

1. Introduction

Organic Thin Film Transistors (OTFT) have been shown to be very promising during the last years due to their low-cost, sustainability and easy fabrication over traditional silicon-based transistors [1-3]. The potential use of devices based on organic materials for, for example, Internet of Things (IoT) and wearable applications, has been explored thanks to the possibilities they offer for the fabrication of smart and flexible electronic systems [4]. Recently, several works have been devoted to the study of either the performance of OTFTs or the properties of the materials themselves [5-8]. However, the OTFTs variability/reliability still require thorough investigation [9-14]. On the one hand, as the fabrication of organic materials is not yet a mature enough process, OTFTs show high initial variability (i.e., Time-Zero Variability (TZV). On the other hand, aging mechanisms, such as Bias Temperature Instability (BTI) and Hot Carrier Injection (HCI) observed in Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs), may also occur in OTFTs, which cause a time-dependent degradation of the device performance (i.e., Time-dependent Variability).

Though the device variability can be detrimental for the circuit performance, it can be exploited in security applications. Contrarily to cryptographic protocols that store digital authentication keys in non-volatile memory (vulnerable to confidentiality breaches), Physical Unclonable Functions (PUFs) use unpredictable physical fingerprints

that are randomly generated during the manufacturing process and are not reproducible. Recently, the variability of OTFTs has been used for PUFs implementation in cryptography applications [9,15–17], leveraging the non-silicon nature of organic devices. Some studies have introduced architectural modifications to improve PUF performance. Kim et al. [16] demonstrated reconfigurable OTFT PUFs using multiscale polycrystalline entropy, and Oin et al. [17] proposed an organic current mirror PUF with enhanced stability against aging. Other works have used graphene based Field Effect Transistors for PUF implementation, reaching good uniqueness values (47-50%) and high reliability (93-100%) [18]. However, the OTFTs degradation mechanisms could negatively impact the PUFs' reliability, i.e., the reproducibility of the generated fingerprints. In one of our previous works [15], it was demonstrated that under certain electrical stress conditions, ID time variations could tend towards saturation, suggesting that introducing a certain amount of aging in the device (previously to the key generation) may be beneficial to implement reliable PUFs. Taking advantage of this issue, our work applies a pre-stress to drive the OTFT drain current toward saturation before key generation. Pre-stress, absent from earlier organic PUF research, is employed to improve reproducibility while maintaining device variability, offering a new route toward more reliable organic electronics-based security primitives. In this work, the homogeneity, uniqueness and reproducibility of PUFs implemented with pre-stressed OTFTs has been preliminary studied.

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2. Experimental

Four-terminal Organic TFTs with a top gate (G), back gate (BG), source (S), drain (D) and multiple channels and with a width of W=360μm and a length of L=2.5μm have been studied. Fig. 1 shows a 3D sketch (a), top view optical image (b) and a cross-section (c) of the analyzed devices [5]. The devices were fabricated by SmartKem Ltd. (Manchester, UK). These OTFTs incorporate SmartKem's proprietary TRUFLEXTM material stack, which consists of a glass substrate, base layer (BL), organic semiconductor (OSC), organic gate insulator (OGI), sputter resistant layer (SRL) and passivation layer (PL); source and drain are made of gold. The fabrication process involves a combination of sputtering, spin coating and photolithographic steps. To evaluate the impact of stress on the OTFTs electrical behavior, 6 or 8 cycles of measurement-stress-measurement tests, with stress durations 10s (1st cycle), 100s (2nd cycle) and 400s (the rest of cycles). BTI ($V_G \neq 0$ and $V_D = V_S = 0$) or HCI-like stresses ($V_G = V_D \neq 0$ and $V_S = 0$), with voltage values of -10V, -20V or -30V, were applied to different devices. Before and after each stress phase (i.e. during the measurement phases), the I_D-t curves were measured at $V_D = V_G = -10V$ during 100s, from which the impact of the previous stress on I_D has been evaluated.

Fig. 2 summarizes the different stages necessary to generate the fingerprints. After the device manufacture (a), devices are pre-stressed with a selected stress bias (b). Then I_D of each device will be measured (c) and binarized (d). The fingerprint of the PUF will be then generated concatenating the binarized current of several devices (e) and stored in a data center. During the authentication stage of a given product, which starts in the step shown in Fig. 1c, the obtained fingerprint of a given PUF is compared and verified with the fingerprints of all generated PUFs, previously pre-stored in a data center.

3. Results

In Fig. 3, some examples of I_D -t curves measured on several devices subjected to different kinds of stresses are plotted. In this plot, the I_D -t curve in the time interval from 0 to 100s is measured on the fresh device, while the subsequent ones correspond to those measured after each of the stress phases of the test. To better visualize the I_D -t characteristics, the current has been normalized for each device to the initial current measured before the stress (i.e. at t=0). Take into consideration that

transient and recovery effects are measured, independently of the type and magnitude of the stress. Despite the transients observed after the stress interruption, the overall $\rm I_D$ during the whole test increases, showing a trend towards saturation that is, $\rm I_D$ shows quite similar values either at the beginning or at the end of each of the measurement phases. To evaluate the stability of $\rm I_D$ after each stress cycle, the initial and final currents registered during the measurement phases have been considered as parameters.

In Fig. 4, as an example, the initial currents normalized to the current obtained in the fresh device at t=0s (that is, before any stress) are plotted. For the final currents (not shown), a similar trend is observed. In all cases, the curves have been fitted to a potential law (continuous lines), which serve as a guide to the eye. Note that in some cases, as for -30V BTI or -20V HCI, the initial $\rm I_D$ shows a continuous increasing trend but, in others, as for -10V BTI, the current tends to remain almost constant after some stress cycles. Therefore, the results indicate that, after a given stress time, the current through the device tends to saturate, suggesting that pre-stressed devices could allow the implementation of reliable PUFs based on $\rm I_D$ (i.e., the generated key would not change with time).

Given these results, PUFs have been implemented by using the $\rm I_D$ current of pre-stressed devices as entropy source. To statistically analyze the implementation of PUFs from the $\rm I_D$ current of OTFTs, the initial/final $\rm I_D$ of 100 pre-stressed OTFTs (-10V BTI) measured after each stress cycle has been binarized. Fig. 5a shows the complete $\rm I_D$ -t curves of the 100 devices recorded during the measurement phases of the MSM tests, while Fig. 5b illustrates the corresponding final $\rm I_D$. Take into account that there is a large device-to-device variability, not only before the stress (i.e., fresh device), but also after each of the stress cycles, demonstrating that the pre-stress does not reduce the device variability, so that it could still be exploited for PUF implementation.

For the generation of fingerprints, the $100~I_D$ values in Fig. 5b were digitized into 8-bit or 4-bit words. From these 8-bit or 4-bit sequences, cryptographic keys of 16 bits have been generated by concatenating 2 or 4 digitized currents of different devices. In this regard, 50 or 25 PUFs, were built, respectively. From these binary words, the reproducibility of the PUFs has been statistically evaluated, respectively, after each of the stress cycles, when the initial (not shown) and final (Table 1) I_D were binarized. The reproducibility was evaluated using the intra-HD distance. Similar results to those included in Table 1 are found when the

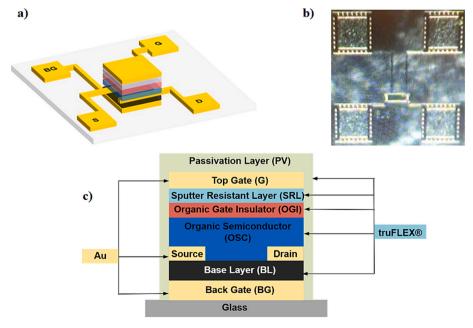


Fig. 1. a) Three-dimensional sketch of the OTFTs, b) optical top view image of the devices and c) the device cross-section schematics.

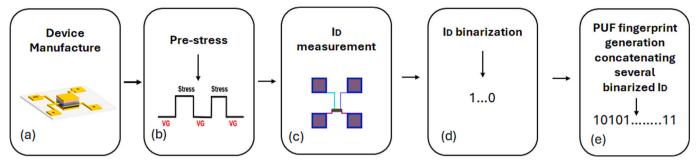


Fig. 2. Schematic diagram to generate and read the fingerprints of the proposed PUFs.

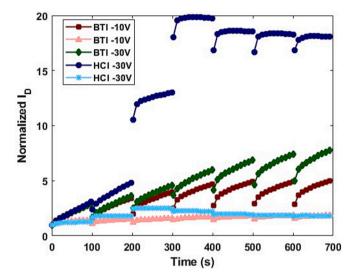


Fig. 3. Examples of the time evolution of ID registered during the measurement phases on the fresh device (from 0 to 100 s) and after the 6 stress cycles on different devices, subjected to different stresses. For each case, the current has been normalized to the initial current of the fresh device at t=0.

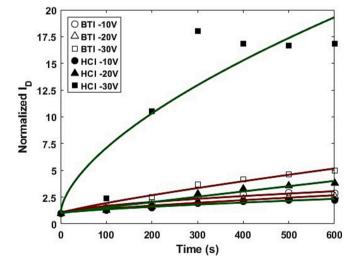


Fig. 4. Initial currents registered during the measurement phases on different devices subjected to different stresses. All currents have been normalized to the current measured in the fresh device. The lines correspond to the fittings to a potential law, for BTI (maroon) and HCI (green).

initial current is considered instead. In Table 1, each row corresponds to the PUF reproducibility obtained when the binarized I_D values after the stress cycle number 'N' are compared with those obtained after the 'N-1' cycle. Columns 1 and 3 show the average and standard deviation PUF reproducibility when ID is binarized using 8 and 4 bits, respectively. Note that, independently of the number of bits, except for the 2 first stress cycles (probably due to transient effects), as the number of stress cycles increases, the key reproducibility increases, since ID tends to saturation and, therefore, the changes in the PUFs fingerprints decrease as the stress proceeds. However, take into account that, for the 8-bit case, as could be expected, the reliability is lower than for the 4-bit case, even after the end of the test. For the 8-bit case, only when the first 4 bits are considered (the most significant bits, Column 2), the reproducibility is similar to that obtained in the 4-bit case. Therefore, from now on, 8-bit binarization will not be considered anymore and we will focus on the 4-bit binarization case. In this case, the reproducibility increases as the number of stress cycles increases, tending to saturate at a final value of 0.96, suggesting that the pre-stress methodology proposed in this work allows to get high values of reliability.

Although these results are quite good, different methods could be applied to improve even more the reproducibility of the PUFs, such as the selection of the devices (i.e., PUFs) with higher reproducibility (close to ideal value of 1.0) [19]. As examples, columns 4 and 5 indicate the average reproducibility obtained when the devices with the lowest individual reproducibility are ruled out (0 and 0.25 in Column 4 and 0, 0.25 and 0.5 in Column 5). Columns 6 and 7 show the number of devices that have been ruled out in the first and second cases, respectively. Interestingly, after device selection, the PUF reproducibility increases, as expected, reaching values of 0.97 and 0.99 (very close to the ideal 1) at the end of the stress test, respectively. Although the increase of the PUFs reproducibility is at the expense of reducing the number of devices, indeed only a reduced number of devices are eliminated (Column 6 and 7). The number of eliminated devices decreases when the stress proceeds (due to the saturation reached in I_D), representing only a 2 or 5% of the total, respectively. Therefore, the results show that the binarization of ID in pre-stressed OTFTs allows the implementation of highly reliable PUFs, with a reproducibility that can be close to 100% if selection methods are implemented.

Finally, to complete the feasibility study of the proposed PUFs, and once their reproducibility has been demonstrated, the averages (X¯) of the uniformity and uniqueness and the standard deviation (SD) of the 25 PUFs has also been investigated. The uniformity of a PUF reflects the randomness of the distribution of "0s" and "1s" and it is assessed by dividing the number of 0-bits by the total number of bits of the corresponding fingerprint and ideally should be 0.5. The uniqueness estimates the degree of correlation between two different PUFs and ideally should be 0.5. It is evaluated from inter-device Hamming Distance (HD), which determines the number of non-equal bits in the keys of two different PUFs. As an example, Table 2 shows these parameters for the 16-bit PUFs after the last stress cycle for the final I_D current (which corresponds to the highest reproducibility case). The table includes the results obtained before and after applying the selection method. Take

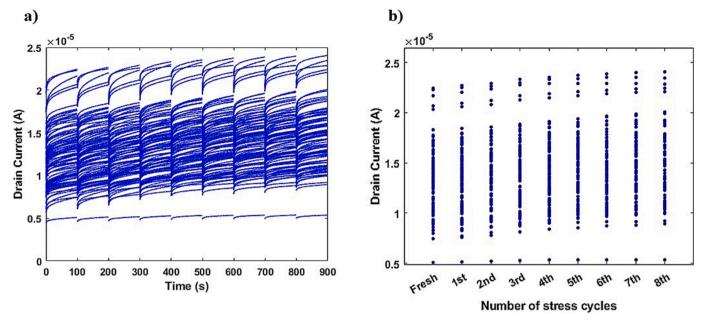


Fig. 5. (a) ID-t curves recorded during the measurement phases of the 8-cycles MSM tests in 100 different devices, stressed at -10V BTI. (b) Currents measured at the end of the measurement phases for the 100 -10V BTI stressed devices after each stress cycle. Large device-to-device variability can still be observed.

Table 1
PUFs keys reproducibility after different stress cycles, for the cases of 8 and 4 bits I_D quantification (columns 1 to 3). PUFs with reproducibility lower than a given value are eliminated to increase the reproducibility of the whole set (columns 4 to 7).

	8 bits	8 bits considering the first 4 bits	4 bits	4 bits by ruling out devices with 0 and 0.25 reproducibility	4 bits by ruling out devices with 0, 0.25, 0.5 reproducibility	Number of devices ruled out (0 and 0.25 reproducibility)	Number of devices ruled out (0, 0.25 and 0,5 reproducibility)
	X [−] ±SD	X [−] ±SD	X [−] ± SD	$\mathbf{X}^- \pm \mathbf{SD}$	$\mathbf{X}^- \pm \mathbf{S} \mathbf{D}$		
Fresh- 1st	$\begin{array}{l} 0.71 \\ \pm \ 0.18 \end{array}$	0.92 ± 0.19	$\begin{array}{c} 0.92 \\ \pm \ 0.18 \end{array}$	0.95 ± 0.12	0.97 ± 0.08	3	7
1st-2nd	$\begin{array}{c} 0.66 \\ \pm \ 0.20 \end{array}$	$\textbf{0.85} \pm \textbf{0.26}$	$\begin{array}{l} 0.85 \\ \pm \ 0.27 \end{array}$	0.93 ± 0.14	0.96 ± 0.08	10	17
2nd-3rd	$\begin{array}{c} 0.60 \\ \pm \ 0.20 \end{array}$	0.76 ± 0.32	$\begin{array}{c} 0.76 \\ \pm \ 0.31 \end{array}$	0.87 ± 0.17	0.92 ± 0.11	16	26
3rd-4th	$\begin{array}{c} 0.64 \\ \pm \ 0.18 \end{array}$	0.84 ± 0.28	$\begin{array}{c} 0.89 \\ \pm \ 0.25 \end{array}$	0.94 ± 0.13	0.95 ± 0.13	7	13
4th-5th	$\begin{array}{c} 0.69 \\ \pm \ 0.20 \end{array}$	0.91 ± 0.22	$\begin{array}{c} 0.9 \pm \\ 0.18 \end{array}$	0.95 ± 0.13	0.98 ± 0.06	2	8
5th-6th	$\begin{array}{l} 0.74 \\ \pm \ 0.18 \end{array}$	0.92 ± 0.20	$\begin{array}{c} 0.92 \\ \pm \ 0.20 \end{array}$	0.96 ± 0.12	0.98 ± 0.05	5	10
6th -7th	$\begin{array}{l} 0.77 \\ \pm \ 0.20 \end{array}$	0.93 ± 0.19	$\begin{array}{c} 0.94 \\ \pm \ 0.16 \end{array}$	0.96 ± 0.11	0.98 ± 0.06	2	6
7th -8th	$\begin{array}{l} 0.78 \\ \pm \ 0.20 \end{array}$	0.95 ± 0.17	$\begin{array}{c} 0.96 \\ \pm \ 0.16 \end{array}$	0.98 ± 0.09	0.99 ± 0.04	2	5

Table 2 Mean (X^-) and standard deviation (SD) of the uniformity and uniqueness of the 4-bit PUFs obtained when the final I_D current after the last stress cycle is the entropy source (last row in Table I), when all the devices are considered (column 1) and when PUFs with reproducibility lower than certain values are ruled out (columns 2 and 3).

	4 bits		4 bits ruling out 0 and 0.25 cases		4 bits ruling out 0, 0.25 and 0.5 cases	
	Unif.	Uniq.	Unif.	Uniq.	Unif.	Uniq
x ⁻	0.523	0.502	0.528	0.503	0.529	0.504
SD	0.188	0.291	0.186	0.290	0.189	0.289

into account that in all cases, uniformity and uniqueness are also very close to the ideal value of 0.5, which further demonstrates the good performance of the PUFs.While this study demonstrates the potential of

pre-stressed OTFTs for PUF applications under controlled conditions, further work is needed to assess their robustness under real-world environmental factors such as entropy estimation, temperature fluctuations, humidity, and long-term operational stability. These aspects will be the focus of future investigations aimed at validating the practical deployment of OTFT-based PUFs.

Finally, note that although 100s pre-stress stages have been used in this study to carefully monitor transients, recovery effects, and current stabilization after each stress cycle, such a long measurement is not required for practical PUF implementation. In real applications, only the stable $\rm I_D$ values used for binarization need to be recorded (after the pre-stress stabilitzation during the manufacture of the PUFs), which can be achieved in much shorter times without compromising their response in time-sensitive applications.

4. Conclusion

Pre-stressed OTFTs have been evaluated for PUF implementation, using the variability of $\rm I_D$ as entropy source. Although $\rm I_D$ shows transients and drifts, for some specific stress conditions, this current tends towards saturation. Large device-to-device $\rm I_D$ variability in the pre-stressed OTFTs is still observed, so that PUFs based on the binarization of this current can be implemented. Their high uniformity, uniqueness and reproducibility have been demonstrated. In particular, a reproducibility of 0.99 after device selection is reached, which is close to the ideal value of 1.0, while a uniformity of 0.52 and uniqueness of 0.50, close to ideal value of 0.5, is obtained.

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CRediT authorship contribution statement

N. Baghban-Bousari: Methodology, Software, Formal analysis, Investigation. D. Eric: Methodology, Software, Investigation. G. Palau: Software, Formal analysis. A. Crespo-Yepes: Methodology, Investigation, Supervision. M. Porti: Conceptualization, Methodology, Investigation, Resources, Supervision. E. Ramon: Investigation, Resources. S. Ogier: Investigation, Resources. M. Nafria: Conceptualization, Methodology, Resources, Supervision.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

The data that has been used is confidential.

References

- C.D. Dimitrakopoulos, Organic field-effect transistors for large-area electronics, Adv. Semicond. Org. Nano-Tech. 14 (2002) 99–117, https://doi.org/10.1016/ B978-012507060-7/50018-0.
- [2] C. Reese, M. Roberts, M. Ling, Z. Bao, Organic thin film transistors, Mater. Today 7 (2004) 20–27, https://doi.org/10.1016/S1369-7021(04)00398-0.
- [3] G. Galderisi, T. Mikolajick, J. Trommer, Impact of Bias temperature instability on reconfigurable field effect transistors and circuits, Microelectron. Eng. 300 (2025) 112374, https://doi.org/10.1016/j.mee.2025.112374.
- [4] X. Guo, Y. Xu, S. Ogier, T.N. Ng, M. Caironi, A. Perinot, L. Li, J. Zhao, W. Tang, R. A. Sporea, A. Nejim, J. Carrabina, P. Cain, F. Yan, Current status and opportunities

- of organic thin-film transistor technologies, IEEE Trans. Electron Devices 64 (2017) 1906–1921, $\label{eq:https://doi.org/10.1109/TED.2017.2677086}.$
- [5] A. Arnal, A. Crespo-Yepes, E. Ramon, L. Terés, R. Rodríguez, M. Nafría, DC characterization and fast small-signal parameter extraction of organic thin film transistors with different geometries, IEEE Electron Device Lett. 41 (2020) 1512–1515, https://doi.org/10.1109/LED.2020.3021236.
- [6] S.H. Ko, H. Pan, C.P. Grigoropoulos, C.K. Luscombe, J.M.J. Fréchet, D. Poulikakos, All-inkjet-printed flexible electronics fabrication on a polymer substrate by lowtemperature high-resolution selective laser sintering of metal nanoparticles, Nanotechnology 18 (2007) 345202, https://doi.org/10.1088/0957-4484/18/34/ 345202.
- [7] H. Jeong, S. Baek, S. Han, H. Jang, S.H. Kim, H.S. Lee, Novel eco-friendly starch paper for use in flexible, transparent, and disposable organic electronics, Adv. Funct. Mater. 28 (2017) 1704433, https://doi.org/10.1002/adfm.201704433.
- [8] N.A. Azarova, J.W. Owen, C.A. McLellan, M.A. Grimminger, E.K. Chapman, J. E. Anthony, O.D. Jurchescu, Fabrication of organic thin-film transistors by spraydeposition for low-cost, large-area electronics, Org. Electron. 11 (2010) 1960–1965, https://doi.org/10.1016/j.orgel.2010.09.008.
- [9] S. Claramunt, G. Palau, A. Arnal, A. Crespo-Yepes, M. Porti, S. Ogier, E. Ramon, M. Nafria, Exploitation of OTFTs variability for PUFs implementation and impact of aging, Solid State Electron. 207 (2023) 108698, https://doi.org/10.1016/j. sse. 2023.108698.
- [10] F. Rasheed, M.S. Golanbari, G.C. Marques, M.B. Tahoori, J. Aghassi-Hagmann, A smooth EKV-based DC model for accurate simulation of printed transistors and their process variations, IEEE Trans. Electron Devices 65 (2018) 667–673, https:// doi.org/10.1109/TED.2017.2786160.
- [11] A. Ruiz, S. Claramunt, A. Crespo-Yepes, M. Porti, M. Nafria, H. Xu, C. Liu, Q. Wu, Exploiting the KPFM capabilities to analyze at the nanoscale the impact of electrical stresses on OTFTs properties, Solid State Electron. 186 (2021) 108061, https://doi.org/10.1016/j.sse.2021.108061.
- [12] Y.A. Chen, Y.Z. Zheng, T.C. Chang, K.J. Zhou, P.J. Sun, Y.H. Hung, Y.H. Lee, T. M. Tsai, J.W. Chen, C.W. Kuo, C.H. Tsai, S. Ogier, Investigation of the self-heating effect in high performance organic TFTs with multi-finger structure, IEEE Electron Device Lett. 43 (2022) 1243–1246, https://doi.org/10.1109/LED.2022.3182721.
- [13] Y.H. Hung, T.C. Chang, Y.F. Tu, I.N. Lu, Y.Z. Zheng, C.L. Chiang, J.J. Chen, C. W. Kuo, L.C. Sun, K.J. Zhou, Improving drain-induced barrier lowering effect and hot carrier reliability with terminal via structure on half-Corbino organic thin-film transistors, IEEE Electron Device Lett. 43 (2022) 569–572, https://doi.org/10.1109/IED.2022.3149898.
- [14] K.K. Ryu, I. Nausieda, D.D. He, A.I. Akinwande, V. Bulovic, C.G. Sodini, Bias-stress effect in Pentacene organic thin-film transistors, IEEE Trans. Electron Devices 57 (2010) 1003–1008, https://doi.org/10.1109/TED.2010.2044282.
- [15] M. Porti, G. Palau, A. Crespo-Yepes, A.A. Rus, S. Ogier, E. Ramon, M. Nafria, On the aging of OTFTs and its impact on PUFs reliability, Micromachines 15 (2024) 443, https://doi.org/10.3390/mi15040443.
- [16] D. Kim, S. Im, D. Kim, H. Lee, C. Choi, J.H. Cho, H. Ju, J.A. Lim, Reconfigurable electronic physically Unclonable functions based on organic thin-film transistors with multiscale polycrystalline entropy for highly secure cryptography primitives, Adv. Funct. Mater. 33 (2022) 2210367, https://doi.org/10.1002/ adfm 202210367
- [17] Z. Qin, M. Shintani, K. Kuribara, Y. Ogasahara, T. Sato, Organic current Mirror PUF for improved stability against device aging, IEEE Sensors J. 20 (2020) 7569–7578, https://doi.org/10.1109/JSEN.2020.2986077.
- [18] A. Dodda, S.S. Radhakrishnan, T.F. Schranghamer, D. Buzzell, P. Sengupta, S. Das, Graphene-based physically unclonable functions that are reconfigurable and resilient to machine learning attacks, Nature electronics 4 (2021) 364–374, https://doi.org/10.1038/s41928-021-00569-x.
- [19] A.S. Andreo, P.S. Canflanca, H.C. Lopez, P. Brox, R.C. Lopez, E. Roca, F. V. Fernandez, A DRV-based bit selection method for SRAM PUF key generation and its impact on ECCs, Integration 85 (2022) 1–9, https://doi.org/10.1016/j.vlsi.2022.02.008.