

Letters

Simulation Study of the Pulse Shaping Effects on the Power, Energy, and Programming Time Requirements of Filamentary-Type Memristors

E. Miranda ¹, Senior Member, IEEE, E. Piros ², F.L. Aguirre, Senior Member, IEEE, X. Pérez, T. Kim, P. Schreyer ³, J. Gehringer ⁴, T. Oster, K. Hofmann ⁵, Senior Member, IEEE, J. Suñé ⁶, Fellow, IEEE, C. Hochberger ⁷, Senior Member, IEEE, and L. Alff ⁸, Member, IEEE

Abstract—As with any memory device, programming a memristor involves trade-offs between power, energy, and time. In this letter, we investigate in detail how these factors are interrelated under different programming conditions. We show that, under time constraints, lower energy consumption can be achieved using faster programming pulses at the cost of increased power dissipation. Conversely, when limiting the maximum power is the priority, longer programming times are required to minimize energy consumption. These trade-offs ultimately stem from the physical response time of ions and vacancies involved in the formation and dissolution of the conductive filament within the oxide layer of a metal-insulator-metal (MIM) structure. We begin by analytically examining the effect of applying a single trapezoidal pulse to the device. Next, we extend the analysis to multiple pulses, using a compact recursive approach to model both potentiation and depression. Finally, we perform SPICE simulations under unconstrained programming conditions. Modeling and simulations are based on the Dynamic Memdiode Model, combined with the Method of Elementary Solvers. Given the variability of device parameters and experimental conditions, we provide the complete SPICE schematic to allow interested readers to explore different scenarios and tailor the analysis to their specific use cases.

Index Terms—Memristor, resistive switching, energy, power, SPICE, LTspice.

I. INTRODUCTION

MEMRISTORS are two-terminal devices that store information in the form of an electrical resistance value [1]. This resistance can be modified by applying an appropriate

electrical stimulus and remains stable once the stimulus is removed. This combination of tunability and nonvolatility characterizes OxRAM and CBRAM devices, making them key enablers for the development of memory arrays and neuromorphic circuits based on resistive switching technologies [2]. Memristor programming can be performed using constant voltage or current sources, signal ramps, or pulses, the latter being the most commonly adopted method due to its superior control and precision [3], [4]. While the effects of duty cycle and signal polarity on the memristive state have been widely studied [5], the impact of the pulse rise and fall times on power dissipation and energy consumption remains largely unexplored. Notably, these non-ideal transition times are inevitable in practical implementations, as idealized pulse shapes exist only as mathematical tools. In this letter, we focus on bipolar-type memristors, where a conductive filament (CF) forms across the dielectric layer in a MIM structure. Although the motion of oxygen vacancies or metal ions is driven by the externally applied electric field, their dynamics are also governed by intrinsic drift properties. Using the Dynamic Memdiode Model (DMM) [6], [7], along with its implementation in the LTspice circuit simulator via the Method of Elementary Solvers (MES) [8], we investigate the influence of realistic pulse shapes on the energy, power, and time required for programming. Experimental results fitted using the DMM can be found in Refs. [7], [9], [10]. To ensure completeness, we provide analytical expressions and a circuit schematic that allow for the assessment of these performance metrics under pulsed operation conditions. This approach contributes to a deeper understanding of the interplay between signal shaping and device behavior in practical memristor-based systems [11], [12], [13], [14], [15].

II. MODEL EQUATIONS AND MAGNITUDES OF INTEREST

In the DMM, the current–voltage (I – V) characteristic and the internal memory state of a bipolar-type memristive device are described by the following system of coupled nonlinear

Received 31 October 2025; revised 17 November 2025 and 29 December 2025; accepted 8 February 2026. Date of publication 10 February 2026; date of current version 24 February 2026. The review of this article was arranged by Associate Editor X. Sun. (Corresponding author: E. Miranda.)

E. Miranda, X. Pérez, and J. Suñé are with Departament d'Enginyeria Electrònica, Universitat Autònoma de Barcelona, 08193 Bellaterra, Spain (e-mail: enrique.miranda@uab.cat).

E. Piros, T. Kim, P. Schreyer, J. Gehringer, T. Oster, K. Hofmann, C. Hochberger, and L. Alff are with Technische Universität Darmstadt, 64289 Darmstadt, Germany.

F.L. Aguirre is with Intrinsic Semiconductors, EC2V 6DN London, U.K. Digital Object Identifier 10.1109/TNANO.2026.3663487

equations [7]:

$$I(V_A, g) = [(I_{on} - I_{off})g + I_{off}] \sinh(\alpha V_C) \quad (1)$$

$$\frac{dg}{dt} = \frac{1-g}{\tau_S(V_B)} - \frac{g}{\tau_R(V_B)} \quad (2)$$

where α is a constant, and I_{on} and I_{off} represent the maximum and minimum current factors, respectively. V_A is the applied voltage, while V_B and V_C correspond to the voltage drops after the snapback and internal series resistances R_S and R_I , respectively (see Fig. 3 for details). The parameter $0 \leq g \leq 1$ denotes the normalized low-voltage conductance of the device, i.e., its memory state at the reading voltage. For simplicity, symmetric switching characteristics are assumed for the set ($V > 0$) and reset ($V < 0$) transition times:

$$\tau_{S,R}(V) = T_0 \operatorname{csch}\left(\frac{V}{V_0}\right) \quad (3)$$

T_0 and V_0 are constants. (3) describes the exponential drift times of oxygen vacancies and metal ions within the dielectric layer [16], incorporating a correction to enforce detailed balance at zero voltage, i.e., $\tau(V=0) \rightarrow \infty$ [17]. This expression can also be extended to account for asymmetric switching transitions if required. In the following analysis, we focus on three key metrics: the maximum dissipated power ($P_{MAX} = I_{MAX} V_{MAX}$), the energy consumption ($E = \int P(t) dt$), and the programming time Prt (time required to reach a target memory state, i.e., $time@g_f$). Representative simulation results for a single pulse obtained using (1)-(3) are shown in Fig. 1. Note that the time units are arbitrary, as (2) is nondimensional.

III. SINGLE PULSE PROGRAMMING: ANALYTIC APPROACH

Let's analyze first the application of a single voltage pulse of height V_M , rise time t_r , fall time t_f , pulse width τ , and period T :

$$V(t) = \begin{cases} \frac{V_M t}{t_r} & t \leq t_r \\ V_M & t_r < t \leq t_r + \tau \\ V_M \left\{ 1 - \frac{1}{t_f} [t - (t_r + \tau)] \right\} & t_r + \tau < t \leq T_P \\ 0 & T_P < t \leq T \end{cases} \quad (4)$$

where $T_P = t_r + \tau + t_f$ is the write pulse duration (Fig. 1(a), (d)). Neglecting the effect of the CF series resistances, i.e., $V_A \gg I \cdot (R_S + R_I)$, the solution to (2) is given by the set of nested expressions g_1 - g_4 :

$$\begin{aligned} g_1(0 \leq t \leq t_r) &= (g_0 - 1) \cdot \\ &\cdot \exp\left\{ \frac{V_0 t_r}{V_M T_0} \left[1 - \cosh\left(\frac{V_M t}{V_0 t_r}\right) \right] \right\} + 1 \\ g_2(t_r < t \leq t_r + \tau) &= [g_1(t = t_r) - 1] \cdot \\ &\cdot \exp\left\{ -\sinh\left(\frac{V_M}{V_0}\right) \left(\frac{t - t_r}{T_0}\right) \right\} + 1 \\ g_3(t_r + \tau < t \leq T_P) &= [g_2(t = t_r + \tau) - 1] \cdot \\ &\cdot \exp\left\{ \frac{V_0 t_f}{V_M T_0} \left[\cosh\left\{ \frac{V_M}{V_0} \left[1 - \left(\frac{t - (t_r + \tau)}{t_f}\right) \right] \right\} \right] \right\} \end{aligned}$$

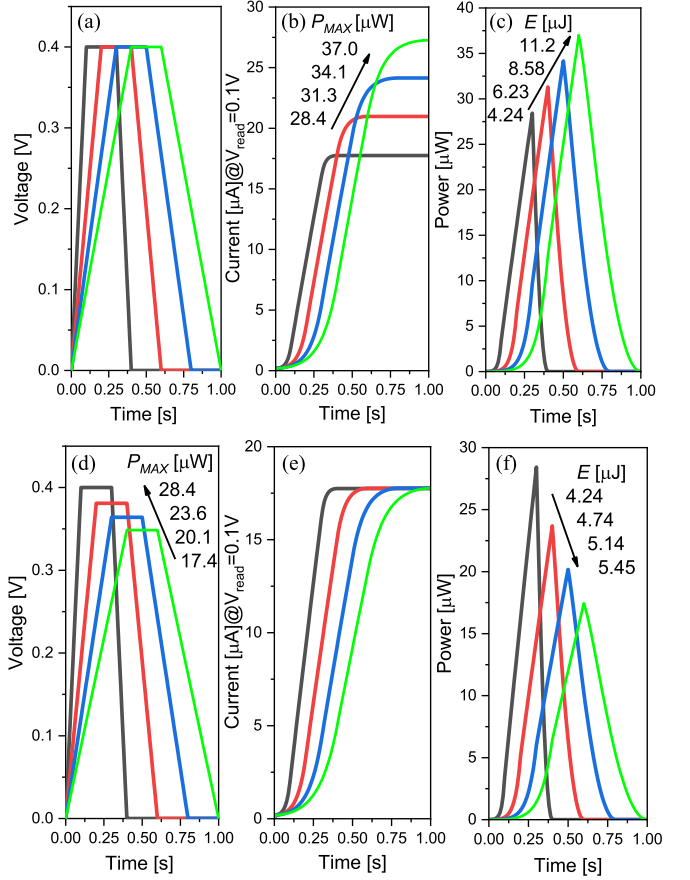


Fig. 1. Panels (a)–(c) show a constant-height pulse with varying rise/fall times, the current at a low fixed bias, and the corresponding power dissipation. Panels (d)–(f) display the same quantities for a fixed memory state. In the first case, power and energy increase with the rise time, whereas in the second, higher powers correspond to lower energies. Power and energy refer to the complete write cycle. Model parameters are given in Fig. 2(a).

$$- \cosh\left\{ \frac{V_M}{V_0} \right\} \left. \right\} + 1$$

$$g_4(T_P < t \leq T) = g_3(t = T_P) \quad (5)$$

where $g_0 = g(t = 0)$. Similar expressions can be found for reset pulses but are not included here. Fig. 1(b) and (c) show the time evolution of the current at a low fixed bias voltage $V_{read} = 0.1V$ and the corresponding power dissipation (write pulse), respectively. As expected, longer programming pulses result in higher read currents, increased peak power P_{MAX} , and greater overall energy consumption as indicated in the legends of Fig. 1(b) and (c). However, since memristor programming targets a specific final state (i.e., identical current at V_{read}), Fig. 1(d)–(f) demonstrate that achieving this state with shorter pulses requires an increase in the pulse amplitude. This, in turn, leads to higher P_{MAX} but a reduction in the total energy consumed E , as shown in the legends of Fig. 1(d) and (f). We can calculate:

$$P_{MAX} = V_M \cdot I(V_M, g_2(t = t_r + \tau)) \quad (6)$$

so that, if $\tau > t_r, t_f$, we can approximate:

$$E \approx \frac{1}{2} P_{MAX} \cdot T_P \quad (7)$$

In light of the results shown in Fig. 1(f), (7) indicates that E is primarily determined by the pulse duration rather than the peak power. Furthermore, (5) highlights the relationship between the programming signal features (V_M and T_P) and the intrinsic switching characteristics of the device (V_0 and T_0).

IV. MULTIPLE PULSE PROGRAMMING: RECURSIVE METHOD

In this section, we analyze the effect of the series resistance R_S on the programming dynamics. From the constant voltage region g_2 in (5), a recursive solution to (1)-(2) can be obtained:

$$I_t = [(I_{on} - I_{off}) g_t + I_{off}] \sinh[\alpha(V_t - R_S I_{t-1})] \quad (8)$$

$$g_t = [g_{t-1} - H(V_t)] \cdot \exp\left[-\sinh\left(\frac{|V_t - R_S I_{t-1}|}{V_0}\right) \frac{\Delta t}{T_0}\right] + H(V_t) \quad (9)$$

Here, t denotes the time, Δt is the simulation timestep, and H the Heaviside function. For simplicity, the condition $R_S \gg R_I$ in the DMM is assumed here. In what follows, we analyze the effect of applying a fixed number of positive (potentiation) and negative (depression) pulses, with particular emphasis on the influence of R_S , a factor not addressed previously. First, as illustrated in Fig. 2(a), the presence of R_S reduces the effective programming voltage $V-I \cdot R_S$, leading to a decrease in the read current, as shown in Fig. 2(b). Consequently, and in line with the results of Fig. 1(d), the pulse amplitude V_M must be adjusted to reach the target memory state. Fig. 2(c) and (d) further confirm that, under constraints on pulse duration or count, maximum power and energy consumption exhibit an inverse relationship. As the pulse ramp rate $RR = V_M/t_r$ increases, P_{Max} rises while the total energy E decreases, both of which are adversely affected by the presence of R_S . The staggered appearance of the curves is solely due to discretization artifacts and can be mitigated by reducing the timestep Δt .

V. MULTIPLE PULSE PROGRAMMING: SPICE SIMULATION

To obtain a comprehensive understanding of the device's behavior under multiple pulse stimulation, SPICE simulation is the most effective approach we can rely on. SPICE not only ensures compliance with Kirchhoff's laws but also optimizes the time discretization automatically. (2) was implemented in LTspice XVII from Analog Devices [18] using the MES [8], which enables the numerical solution of differential equations by configuring two opposing behavioral current sources in a single mesh (see Fig. 3). The voltage at node g corresponds to the solution of the differential equation. This method fully exploits the behavioral modeling capabilities available in LTspice. The solver is coupled to the $I-V$ circuit via the current source labeled M (see Fig. 3). The reset term is considered irrelevant during the programming phase (positive voltage only). The parameter g_f represents the target memory state, and the *Pulse* source provides the input signal. The operators ddt and

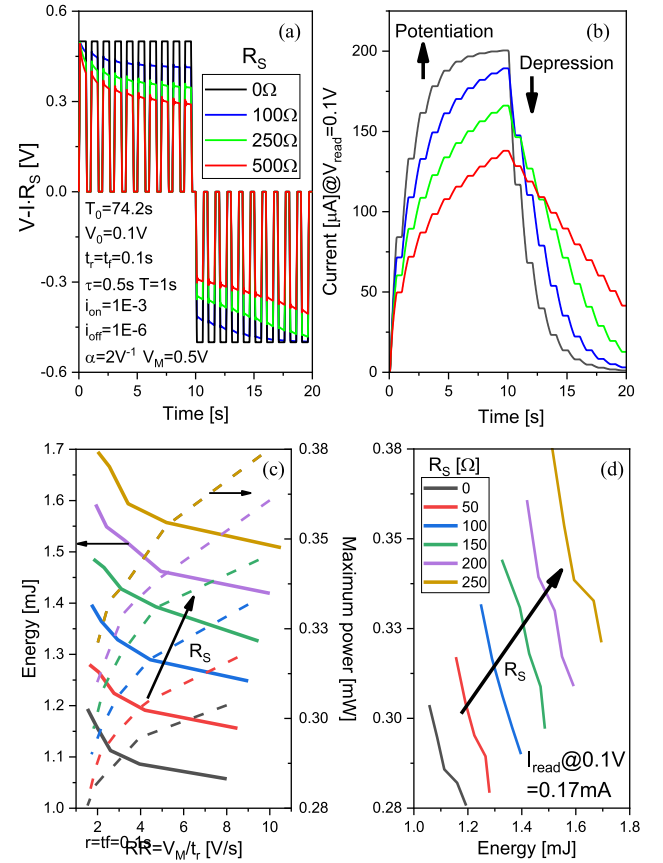


Fig. 2. (a) Effect of the series resistance on the effective magnitude of the pulses. (b) Potentiation and depression of the programming current. (c) Energy and power as a function of RR . (d) Correlation between energy and power.

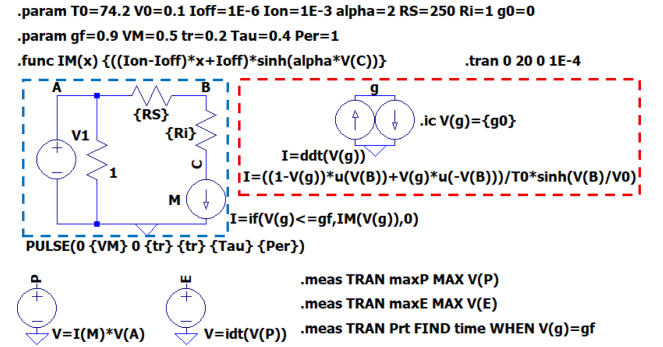


Fig. 3. LTspice model schematics for simulating the memristor behavior under pulsed stimulation. The $I-V$ circuit in blue and the memory solver in red.

idt represent the time derivative and time integral, respectively. u is the step (Heaviside) function. Once g_f is reached, the programming current is redirected through a 1Ω shunt resistor. The *.meas* statements are used for post-processing computations. Fig. 4(a) and (b) illustrate the evolution of power dissipation and energy consumption, respectively, for two different rise times ($t_r = t_f$). Although during potentiation the peak power per cycle reaches higher values for longer rise times (t_r), the maximum power P_{Max} remains unchanged (Fig. 4(a)). However, differences become apparent in both the energy consumption E and the programming time Prt (Fig. 4(b)).

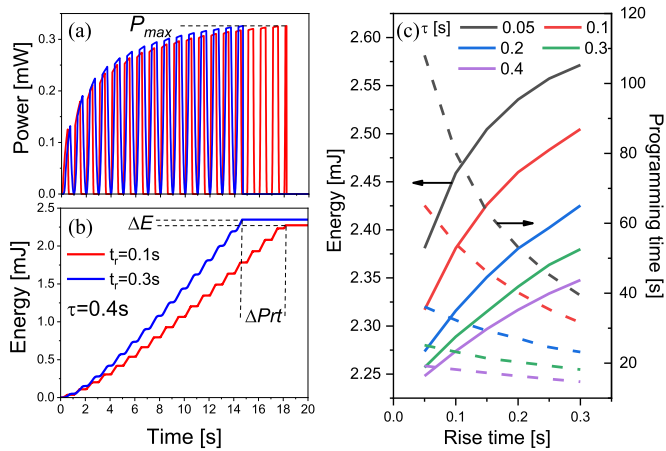


Fig. 4. (a) Dissipated power as a function of time for pulses with different rise times. (b) Consumed energy as a function of time. (c) Energy (E) and programming time (Prt) as a function of the rise time for different pulse lengths. Model parameters in Fig. 2(a). ΔE and ΔPrt are the variations of E and Prt .

As summarized in Fig. 4(c), pulses with shorter rise times combined with longer pulse widths reduce energy consumption, albeit at the cost of increased programming times. These findings are consistent with results reported for memory state-controlled programming trajectories [19] and for application of unconstrained ramped signals [20] in which a trade-off between energy and power was reported. Note that as a side effect of decreasing the rise/fall times of the programming pulses, the voltage/current spectrum extends to higher frequencies, which can significantly impact the parasitic capacitances and inductances present in the system [21]. These higher-frequency components may lead to unwanted reactive effects, such as signal distortion, increased electromagnetic interference, and potential degradation of device performance. Therefore, careful consideration of the rise time is essential to balance programming efficiency with the mitigation of parasitic phenomena in practical implementations.

VI. CONCLUSION

The trade-offs between power dissipation, energy consumption, and programming time in filamentary-type memristor when stimulated with voltage pulses were investigated using the Dynamic Memdiode Model. While power dissipation is primarily associated with Joule heating and the power supply, energy consumption and programming time are critical metrics for evaluating device efficiency and sustainability. To analyze these key technological features, three complementary methods of increasing complexity were presented. The study began with a fully analytical formulation for a single pulse (neglecting series resistance), proceeded with a recursive computational approach for multiple pulses (valid for both potentiation and depression), and concluded with a comprehensive SPICE simulation (compact behavioral approach with post-processing capabilities). This multi-level methodology provides both theoretical insight and practical evaluation tools for optimizing memristive device performance.

REFERENCES

- [1] A. Isah and J. Bilbaut, "Review on the basic circuit elements and memristor interpretation: Analysis, technology and applications," *J. Low Power Electron. Appl.*, vol. 12, 2022, Art. no. 44, doi: [10.3390/jlpea12030044](https://doi.org/10.3390/jlpea12030044).
- [2] F. Aguirre et al., "Hardware implementation of memristor-based artificial neural networks," *Nature Commun.*, vol. 15, 2024, Art. no. 1974, doi: [10.1038/s41467-024-45670-9](https://doi.org/10.1038/s41467-024-45670-9).
- [3] V. Milo et al., "Accurate program/verify schemes of resistive switching memory (RRAM) for in-memory neural network circuits," *IEEE Trans. Electron Devices*, vol. 68, no. 8, pp. 3832–3837, Aug. 2021, doi: [10.1109/TED.2021.3089995](https://doi.org/10.1109/TED.2021.3089995).
- [4] W. Song et al., "Programming memristor arrays with arbitrarily high precision for analog computing," *Science*, vol. 383, pp. 903–910, 2024, doi: [10.1126/science.ad9405](https://doi.org/10.1126/science.ad9405).
- [5] S. Brivio, S. Spiga, and D. Ielmini, "HfO₂-based resistive switching memory devices for neuromorphic computing," *Neuromorphic Comput. Eng.*, vol. 2, 2022, Art. no. 042001, doi: [10.1088/2634-4386/ac9012](https://doi.org/10.1088/2634-4386/ac9012).
- [6] E. Miranda, "Compact model for the major and minor hysteretic I-V loops in nonlinear memristive devices," *IEEE Trans. Nanotechnol.*, vol. 14, no. 5, pp. 787–789, Sep. 2015, doi: [10.1109/TNANO.2015.2455235](https://doi.org/10.1109/TNANO.2015.2455235).
- [7] F. L. Aguirre, J. Suñe, and E. Miranda, "SPICE implementation of the dynamic memdiode model for bipolar resistive switching devices," *Micromachines*, vol. 13, 2022, Art. no. 330, doi: [10.3390/mi13020330](https://doi.org/10.3390/mi13020330).
- [8] E. Miranda, "The method of elementary solvers in SPICE," *Electronics*, vol. 13, 2024, Art. no. 2480, doi: [10.3390/electronics13132480](https://doi.org/10.3390/electronics13132480).
- [9] F. L. Aguirre, S. M. Pazos, F. Palumbo, J. Suñe, and E. Miranda, "Application of the quasi-static memdiode model in cross-point arrays for large dataset pattern recognition," *IEEE Access*, vol. 8, pp. 202174–202193, 2020, doi: [10.1109/ACCESS.2020.3035638](https://doi.org/10.1109/ACCESS.2020.3035638).
- [10] F. Aguirre et al., "Simulation of the effect of material properties on yttrium oxide memristor-based artificial neural networks," *APL Mach. Learn.*, vol. 1, 2023, Art. no. 03610, doi: [10.1063/5.0143926](https://doi.org/10.1063/5.0143926).
- [11] L. Deng, D. Wang, Z. Zhang, P. Tang, G. Li, and J. Pei, "Energy consumption analysis for various memristive networks under different learning strategies," *Phys. Lett. A*, vol. 380, pp. 903–909, 2016, doi: [10.1016/j.physleta.2015.12.024](https://doi.org/10.1016/j.physleta.2015.12.024).
- [12] H. Liu, M. Wei, and Y. Chen, "Optimization of non-linear conductance modulation based HHon metal oxide memristors," *Nanotechnol. Rev.*, vol. 7, pp. 443–468, 2018, doi: [10.1515/ntrev-2018-0045](https://doi.org/10.1515/ntrev-2018-0045).
- [13] S. Saleh and B. Koldehofe, "On memristors for enabling energy efficient and enhanced cognitive network functions," *IEEE Access*, vol. 10, pp. 129279–129312, 2022, doi: [10.1109/ACCESS.2022.3226447](https://doi.org/10.1109/ACCESS.2022.3226447).
- [14] A. Baroni et al., "An energy-efficient in-memory computing architecture for survival data analysis based on resistive switching memories," *Front. Neurosci.*, vol. 16, 2022, Art. no. 932270, doi: [10.3389/fnins.2022.932270](https://doi.org/10.3389/fnins.2022.932270).
- [15] F. Aguirre et al., "Simulation of the effect of material properties on yttrium oxide memristor-based artificial neural networks," *APL Mach. Learn.*, vol. 1, 2023, Art. no. 036104, doi: [10.1063/5.0143926](https://doi.org/10.1063/5.0143926).
- [16] D. Wouters, S. Menzel, J. Rupp, T. Hennen, and R. Waser, "On the universality of the I–V switching characteristics in non-volatile and volatile resistive switching oxides," *Faraday Discuss.*, vol. 213, pp. 183–196, 2019, doi: [10.1039/C8FD00116B](https://doi.org/10.1039/C8FD00116B).
- [17] R. Rodríguez-Fernández, J. Muñoz-Gorri, J. Suñe, and E. Miranda, "A new method for estimating the conductive filament temperature in OxRAM devices based on escape rate theory," *Microelectronics Rel.*, vol. 88–90, pp. 142–146, 2018, doi: [10.1016/j.microrel.2018.06.120](https://doi.org/10.1016/j.microrel.2018.06.120).
- [18] LTspice simulation software, Accessed: Feb. 17, 2026. [Online]. Available: <https://www.analog.com/en/resources/design-tools-and-calculators/ltspace-simulator.html>
- [19] E. Miranda et al., "The role of the programming trajectory in the power dissipation dynamics and energy consumption of memristive devices," *IEEE Electron Device Lett.*, vol. 45, no. 4, pp. 582–585, Apr. 2024, doi: [10.1109/LED.2024.3368146](https://doi.org/10.1109/LED.2024.3368146).
- [20] E. Miranda et al., "Analysis of the voltage ramp rate effects on the programming characteristics of bipolar-type memristive devices," *IEEE Trans. Nanotechnol.*, vol. 24, pp. 205–208, 2025, doi: [10.1109/TNANO.2025.3556856](https://doi.org/10.1109/TNANO.2025.3556856).
- [21] S. Ramo, J. Whinnery, and T. Van Duzer, *Fields and Waves in Communication Electronics*, 3rd ed. Hoboken, NJ, USA: Wiley, 1994.