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SPICE-Compatible Compact Modeling of Cuprate-Based Memristors Across a Wide Temperature Range

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ABSTRACT

Cryogenic memristors based on the high-temperature superconductor $\text{YBa}_2\text{CuO}_{7-\delta}$ offer significant potential as nonvolatile memory elements or unit cell for analog artificial neural networks for future applications such as control units for quantum processors, cryogenic data centers or space-related electronics. In this work, the experimental switching capabilities of cuprate-based memristors are analyzed in terms of the material-specific physics. This work investigates the experimental switching behavior of cuprate-based memristors across temperatures from cryogenic to room temperature. The underlying interpretation, namely the trapping of injected charge carriers at a metal interface and field-induced detrapping, is incorporated into a physically inspired compact model. The core equations of this model consist of a differential balance equation and a current equation, which is derived from space-charge limited conduction. Comparison with experimental data shows that the model successfully reproduces the key features of the measured switching behavior across a wide temperature range, spanning from 80 to 300 K. Additionally, we implement the model in SPICE, enabling circuit-level simulations. The resulting compact model provides a useful framework for guiding experimental studies, capturing key features of the switching behavior, and bridging the gap between device-level characterization and circuit-level design.

1 | Introduction

Artificial intelligence (AI) has become an important driver of modern computing, but its rapid expansion is accompanied by a growing energy demand, particularly in large-scale data centers and latency-critical applications [1–4]. This has motivated the exploration of alternative computing paradigms beyond the classical von Neumann architecture. Neuromorphic computing, based on memristive devices as nonvolatile memory and computational elements, offers a route toward improved energy efficiency by reducing data transfer between memory and processing units [5–8]. This perspective motivates the extension of hardware-based neuromorphic concepts to niche applications,

such as real-time onboard computing for navigation and control in satellite systems, thereby requiring memristive devices and circuits that can operate under extreme conditions, including cryogenic temperatures and high-energy radiation [9, 10].

Besides neuromorphic computing, quantum computing represents another rising computing approach beyond classical computing architectures that potentially will impact, for example cryptography, simulation of molecule folding or exploring exotic material phases [11–13]. As this technology is still in its early stages, for the up-scaling of quantum computers from tens to thousands of logical qubits architectural problems need to be addressed. One of the main problems is given by the number

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of wires, connecting the control electronics to the quantum processor, because thermal leakage affects the coherence times of the qubits. Thus, technological advancement of quantum computers demands the development of processors and, in particular, memory and control technologies suitable for operation at the 4 or 77 K stages of a dilution refrigerator [14]. Recent experimental work has demonstrated that integrating a cryogenic FPGA with a switch matrix at the 4 K stage enables efficient routing of microwave waveforms and enhances the control of quantum-dot-based spin qubits [15]. Complementary approaches have proposed the use of memristor-based cryogenic programmable DC sources, such as TiO_2 devices, for local biasing of quantum dots, highlighting the potential of nonvolatile elements for cryogenic control architectures [16]. Beyond control electronics, large-capacity memories are also required at low temperatures to store data generated by quantum error correction and to avoid thermally induced decoherence of the qubits [17]. While the suitability of DRAM in a cryogenic environment has been investigated, the search for high-density memories compatible with single-flux quantum (SFQ) electronics is one of the main challenges to make use of superconducting electronics as a low-power and high-performance alternative to conventional CMOS technology [17, 18]. Although memristive devices such as filamentary resistive random-access memory (RRAM), phase-change memory (PCM), or magnetic tunnel junctions (MTJs) have been widely explored due to their high integration density at room temperature, each of these technologies exhibits significant drawbacks when operated at cryogenic temperatures, including increased latency, reduced endurance, and limited ON/OFF ratios. On the other hand, memories and neuromorphic circuits based on superconducting electronics are lacking a high integration density given to their complexity [14, 19]. In this regard $\text{YBa}_2\text{Cu}_3\text{O}_{7-\delta}$ (YBCO) has attracted increasing attention for cryogenic memory applications in recent years [20–23]. This high-temperature superconductor shows promise not only as a cryogenic memory medium but also as a bridge between neuromorphic computing and SFQ logic. The realization of cryogenic resistive random-access memories (RRAMs) based on YBCO thus opens pathways toward integrated hardware AI implementations at cryogenic temperatures, where memory units, SFQ circuits, and quantum processors could coexist within a unified technological platform to tackle challenges in deep-space application, quantum computing and cryogenic data centers [17, 18, 24–27].

Recently, we have demonstrated that multiple resistance states can be stabilized in heterostructures composed of $\text{La}_{0.7}\text{Sr}_{0.3}\text{MnO}_3$ (LSMO) and YBCO [28]. This multilevel switching behavior is attributed to the unique layered crystal structure of cuprate superconductors, consisting of alternating CuO -chains, acting as a charge reservoir, and CuO_2 -planes, being the main driver of the metal-insulator transition (MIT) [29, 30]. As a resistive switching mechanism a charge trapping induced MIT, similar to the situation described in $\text{Bi}_2\text{Sr}_2\text{CaCu}_2\text{O}_{8+\delta}$, has been proposed [28, 31, 32]. Furthermore, conduction in the memristive cells follows space-charge-limited current (SCLC) with an exponential trap distribution in the high-resistance state (HRS), while the low-resistance state (LRS) exhibits a temperature-independent power-law behavior over a wide voltage range [33, 34].

The memristor, first postulated by Leon Chua in 1971, was theoretically predicted as the fourth fundamental passive circuit

element—complementing the resistor, capacitor, and inductor—linking electric charge and magnetic flux for reasons of circuit symmetry [35, 36]. However, it was not until the experimental realization of a TiO_2 -based memristor in 2008 that the concept attracted widespread attention [37]. The integration of memristors into large-scale circuits requires suitable modeling approaches, which can broadly be divided into physical models and compact models. Physical models aim at relating the device's electrical behavior to its underlying physical mechanisms, whereas compact models provide a mathematical description intended to capture the essential device macroscopic electrical properties [38–40]. The two approaches involve a trade-off: physical models offer higher accuracy but demand longer simulation times, while compact models are less precise yet more versatile, enabling efficient simulation of various memristive devices in circuit environments with tools such as SPICE (Simulation Program with Integrated Circuit Emphasis) [41–43]. The connection between both approaches is established through the definition of a state variable determined by the physics of the switching process [44]. Having defined the state variable, the model should provide suitable equations to determine its time evolution under the application of arbitrary input signals. In this work, we define a state variable and we propose a behavioral compact model based on two coupled equations, a differential equation for the evolution of the state variable and an algebraic equation relating the current to the state variable and to the applied voltage. In this way we can calculate the response of the YBCO memristor both for the current as a function of voltage and the resistance hysteron (hysteretic resistance versus voltage) at small read voltages for a wide range of temperatures. The model is inspired by a physical picture in which the SET transition is related to the trapping of electrons in oxygen vacancies, thus increasing the effective hole density, and the RESET to the detrapping of the electrons under opposite bias. Trapping during the SET transition is related to the number of injected electrons and to their energy while the electric field is responsible for the detrapping. On the other hand, according to the experimental results, the SCLC model is assumed for the current-voltage relation.

The manuscript is organized as follows. First, the most important experimental results are summarized and the physical interpretation is discussed based on these findings. Afterward the formalism of the model and its underlying concepts are introduced. Finally, we show that the model captures the main trends of the experimental data and we present some results showing that the model is adequate for SPICE simulation.

2 | Results and Discussion

2.1 | Methodology and Relevant Experimental Results

To highlight the relevance of a compact model for capturing the dynamics of cuprate-based cryogenic memristors, this section provides a brief overview of the methodology and key experimental results. Figure 1a shows a schematic of the devices, which consist of a bottom layer of LSMO and an active YBCO layer. Gold electrodes are deposited on top of the LSMO and YBCO layers to operate the devices, while short circuits are

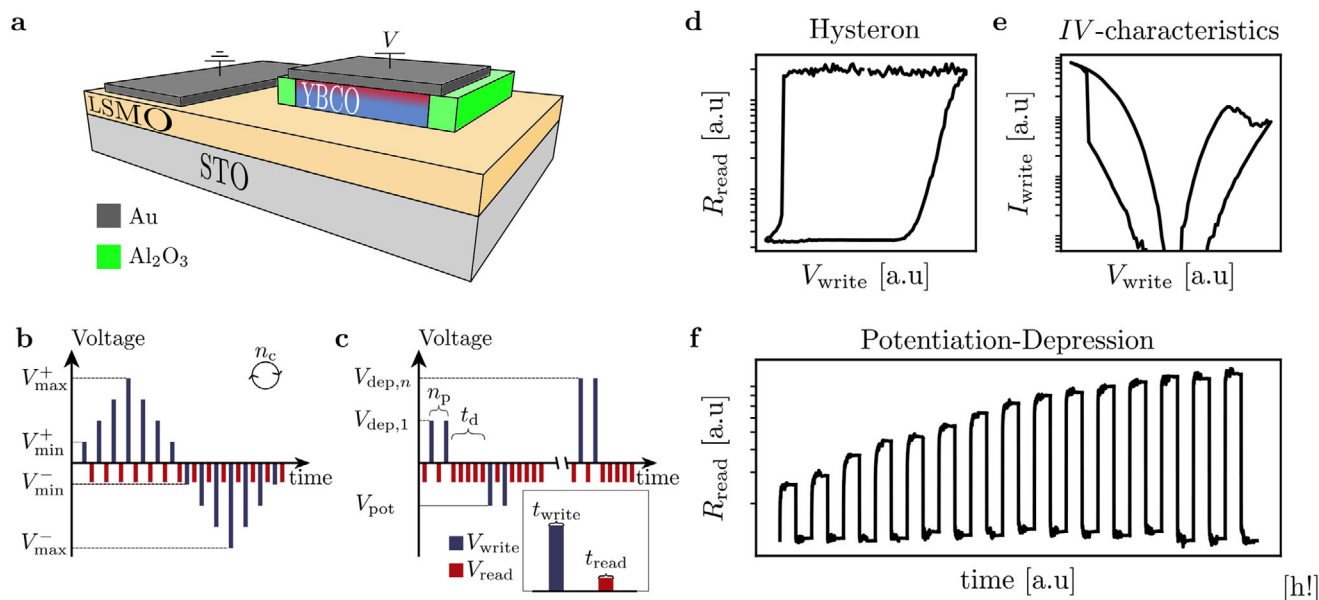


FIGURE 1 | Characterized devices and applied methodology: (a) Schematic of the device layout. (b) Illustration of the Voltage sweep experiment. (c) Pulse-based experiments to extract reversibility and stability of programmed memristive states. The inset in Figure (c) is valid for panel (c) and (b). From (b) the Hysteron in (d) and the *IV*-characteristics in (e) are extracted. (f) Potentiation and depression experiments obtained from (c). The results in (d–f) are measurement results, however, as this Figure is only meant to illustrate the methodology, data are presented in arbitrary units.

prevented by an insulating alumina (Al_2O_3) layer. All layers are grown on SrTiO_3 (STO) substrates. Details about the thicknesses are found in the Methods section. Two distinct pulse schemes are applied to operate the devices. In the first scheme, reading and writing pulses are alternated with steadily increasing and decreasing writing amplitudes: $V_{\min}^+ \rightarrow V_{\max}^+ \rightarrow V_{\min}^+$ for the positive branch and $V_{\min}^- \rightarrow V_{\max}^- \rightarrow V_{\min}^-$ for the negative branch. This “voltage sweep” scheme, illustrated in Figure 1b, probes the hysteretic behavior of the devices, resulting in the hysteron and *IV*-characteristics in Figure 1d,e. The second scheme in Figure 1c tests reversibility and stability of programmed resistance states. Negative voltages, V_{pot} , potentiate the device (decreasing resistance), while positive voltages, V_{dep} , induce depression (increasing resistance). The amplitudes of potentiation and depression pulses can be independently controlled, whereas the number of potentiation/depression pulses, n_p , and the decay time, t_d , are held constant throughout the measurement. For the potentiation and depression experiment presented in Figure 1f, alternating periods of potentiation and depression pulses are applied. The number of pulses is 100 to ensure saturation of the device resistance. All potentiation cycles are done with the same voltage amplitude, while the depression voltage is steadily increased in between the potentiation cycles. Experiments following this scheme are referred to as pulse-based experiments throughout the manuscript. Pulse durations for the writing (t_{write}) and reading (t_{read}) pulses are both set to 0.3 ms. The reading voltage $V_{\text{read}} = -1$ V is chosen to prevent any unintended potentiation or depression. These parameters are maintained constant for both the voltage sweep and pulse-based experiments presented in this manuscript. The main advantage of the voltage-sweep scheme in Figure 1b is that it provides both the hysteron and the hysteretic *IV*-characteristics in a single measurement, making it easier to detect changes in the device state. Saturated pulse-based experiments (Figure 1c) provide additional information about the reversibility of the switching mechanism as shown in

Figure 1f, while progressive depression pulses test the stability of programmed resistive states (Figure S1).

A temperature dependent study of the *IV*-characteristic in Figure 2a and the Hysteron in Figure 2b revealed that the resistance of the HRS decreases exponentially with temperature, while the resistance of the LRS increases exponentially, as depicted in Figure 2c. This behavior was found in samples with a 30 and 50 nm thick YBCO layer. The different ratios between R_{HRS} and R_{LRS} shown in Figure 2d are related to the thickness of the YBCO layer, which leaves room for future studies and device optimization. Crucially for the development of the compact model, the extracted SET voltages V_{SET} (Figure 2e) and RESET voltages V_{RESET} (Figure 2f) exhibit no dependence on either temperature or YBCO thickness over the full temperature range. Based on this argument ion motion is excluded as a responsible switching mechanism and instead a physical interpretation based on charge trapping is introduced. Because the pristine devices are in the HRS, it is assumed that an underdoped, insulating layer of YBCO exists beneath the gold contact, containing fragmented CuO -chains between the CuO_2 -planes of the epitaxial lattice [28]. Photodoping experiments have demonstrated that electrons can be trapped in oxygen vacancies, effectively introducing holes into the CuO_2 -planes and stabilizing non-volatile transitions [45, 46]. Applying a negative bias voltage, or equivalently injecting electrons from the top electrode, may lead to charge trapping within the oxygen vacancies if a certain threshold voltage, V_{SET} , is exceeded. These localized charges, in turn, enhance the interlayer coupling between the copper oxide planes, triggering a insulator-metal transition and resulting in the LRS of the device [47–49]. Similar experiments performed on $\text{Bi}_2\text{Sr}_2\text{CaCu}_2\text{O}_{8+\delta}$ (BSCCO) support this interpretation [31, 32].

To conclude this section, experiments focused on intermediate resistance states are introduced. In Figure 3a it is found that, by

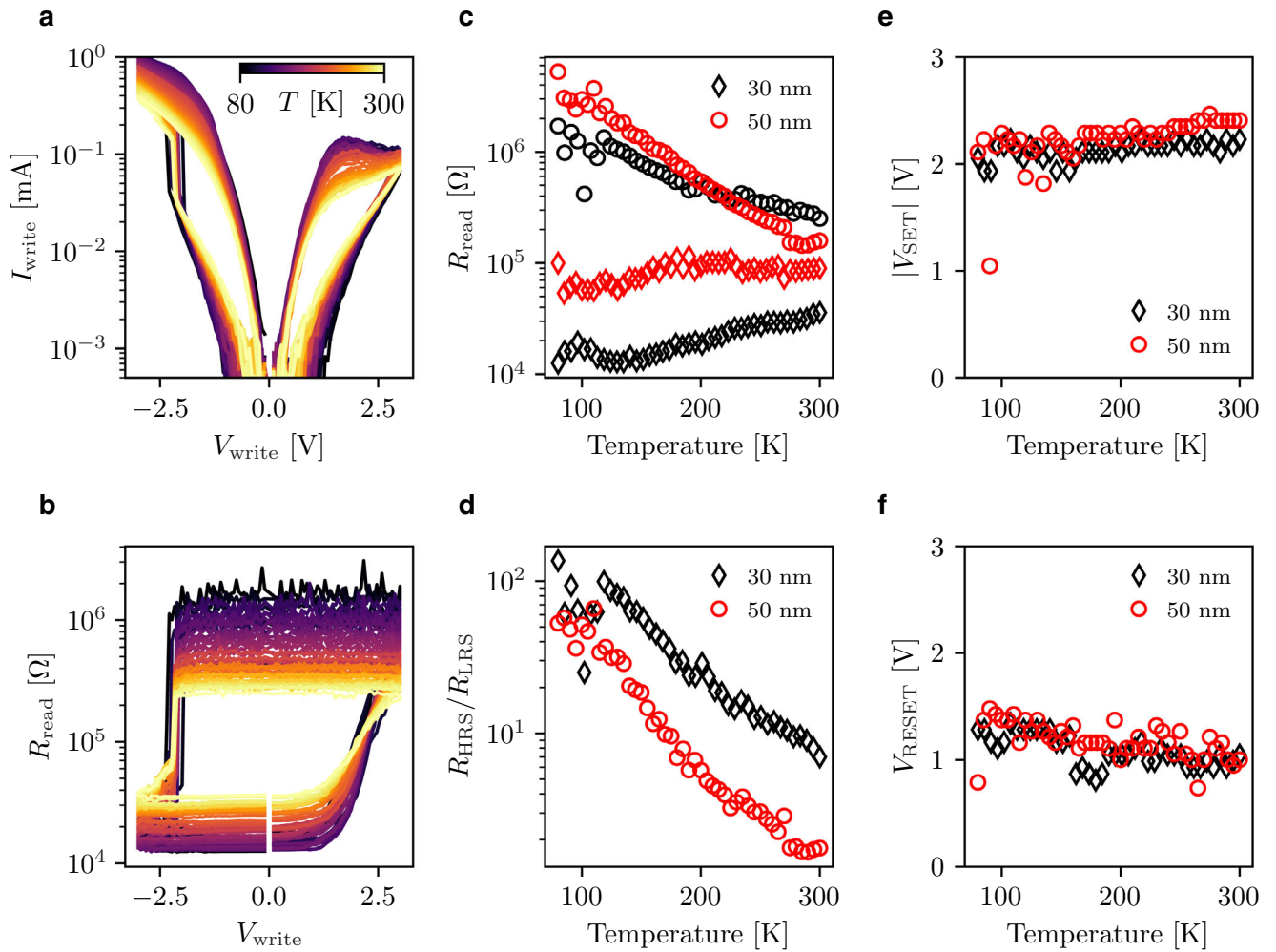


FIGURE 2 | Temperature dependence of the memristor for different thicknesses of YBCO: (a) IV-characteristics extracted in a temperature range from 80 to 300 K for a device of 30 nm thickness. (b) Experimentally obtained Hysteron in the same temperature range. The color code indicated by the legend in (a) is also valid for (b). (c) Comparison between the HRS (open circles) and LRS (open diamonds) resistances for devices with a 30 nm and 50 nm thick YBCO layer. (d) Resistance ratio as a function of temperature for the two considered device thicknesses. In (e) extracted SET voltage and in (f) extracted RESET voltage for the two different devices across the measured temperature range.

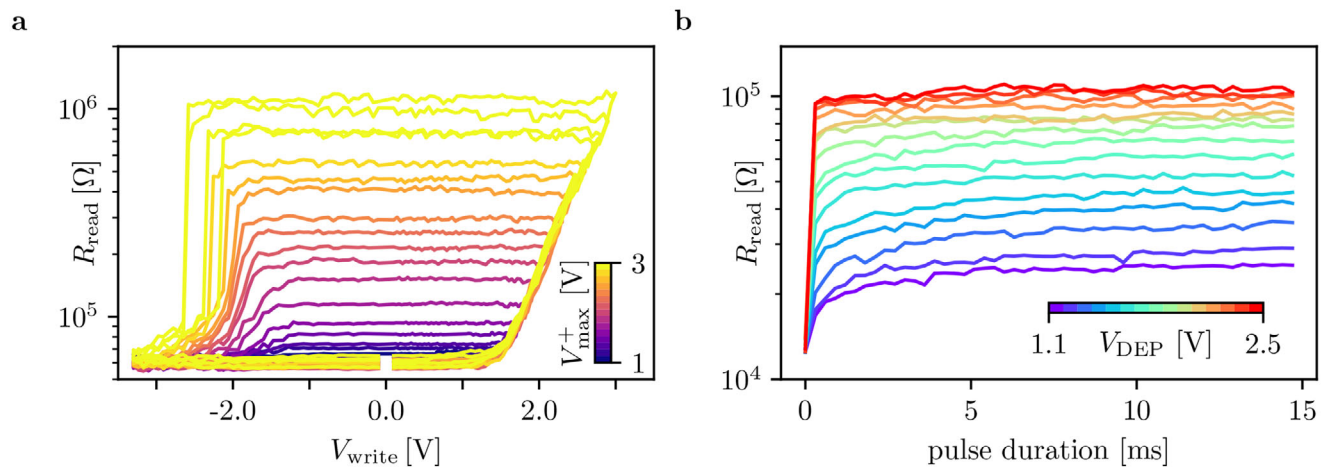


FIGURE 3 | Programming intermediate states: (a) extracted Hysteron after the application of steadily increasing voltage bias, V_{max} , during the RESET transition as indicated by the color bar. (b) Depression measurement for voltages of increasing amplitude against the pulse duration. The amplitude of the depression pulses is indicated by the color bar.

controlling the maximum voltage applied to induce the RESET transition, during voltage sweeps, intermediate states can be stabilized. The minor loops resulting from this experiment, also show a clear dependence of V_{SET} based on the initial intermediate resistance state, R_{init} . On the other hand, it is emphasized that intermediate states can also be prepared through the application of RESET pulses with different amplitude. As illustrated in Figure 3b, the resistance is found to saturate at different values (different intermediate states) for different pulse voltage. It is notable, that this saturation is reached almost instantaneously in the time scale of the conducted depression experiments. This suggests that the devices can be operated at much higher speeds. Some of the key experimental observations—such as the abrupt SET transition, the gradual RESET occurring across a wide temperature range, the state-dependent SET voltage, and the voltage-dependent saturation of different states during the RESET transition—are incorporated into the compact model introduced in the following section.

2.2 | Compact-Physical Model

As a starting point, we represent the electrical behavior of the device as a series connection of several resistances. This is a very simplistic viewpoint that assumes linear conduction, but it is useful for discussing key aspects such as the definition of the state variable, and for illustrating its limited development during the RESET transition. Then, we address the actual device conduction properties by considering its strongly non-linear IV -characteristics. The resistance of the actively switching YBCO layer is divided into a high-resistance layer (HRL) and a low-resistance layer (LRL), while the passive components of the device, such as the contact resistances and the resistance of the LSMO layer are lumped together into a series resistance R_s . The thickness of the active YBCO layer is denoted by t_{ox} and an internal state variable g is defined to describe the fraction of the layer thickness occupied by the LRL. If the thickness of the HRL and LRL are t_{H} and t_{L} , respectively, it follows that $t_{\text{ox}} = t_{\text{H}} + t_{\text{L}}$, with $g = t_{\text{L}}/t_{\text{ox}}$ and $1 - g = t_{\text{H}}/t_{\text{ox}}$. The resistance of each layer is then given by $R_{\text{L}} = \rho_{\text{L}} t_{\text{L}}/A$ and $R_{\text{H}} = \rho_{\text{H}} t_{\text{H}}/A$, where A is the area and ρ_{L} and ρ_{H} are the resistivities of each layer. Thus, the voltage drop in the LRL V_{L} is given by a voltage divider as

$$V_{\text{L}} = \frac{R_{\text{L}}}{R_{\text{L}} + R_{\text{H}}} V = \frac{g \rho_{\text{L}}}{(1 - g) \rho_{\text{H}} + g \rho_{\text{L}}} V \quad (1)$$

And the electric field in the LRL is given by

$$F_{\text{L}} = \frac{V_{\text{L}}}{t_{\text{L}}} = \frac{\rho_{\text{L}}}{(1 - g) \rho_{\text{H}} + g \rho_{\text{L}}} \left(\frac{V}{t_{\text{ox}}} \right) \quad (2)$$

A schematic representation of the SET transition is given in Figure 4a. The SET transition is not expected to depend on the electric field but on the applied voltage, since this voltage increases both the number and energy of the injected charge carriers as illustrated in Figure 4c. According to SCLC-theory the injected carrier density, n_{e} , increases strongly with applied voltage and peaks at the injecting interface following $n_{\text{e}} \propto V x^{-2}$ (in the simplest case when the measurement temperature T equals the characteristic temperature T_{c}) [33]. When a sufficiently large number of high-energy electrons is injected, they become

trapped in oxygen vacancies within the HRL, triggering an abrupt insulator-to-metal transition in the whole HRL. After the SET, the LRL occupies the whole YBCO thickness and hence, $g = 1$. On the contrary, when the voltage is reversed and the electric field reaches a certain threshold, electrons are detrapped and the HRL begins to grow from the Au/YBCO interface into the YBCO layer, as schematically shown in Figure 4b. The development of the field within the HRL and LRL is sketched in Figure 4d. The electric field in the HRL is always larger in the HRL. However, detrapping depends on the field at the boundary of the LRL. When the HRL grows, the field in the LRL decreases. Eventually, if this field reaches a minimum critical value, no more detrapping is possible and the HRL reaches a maximum thickness. This means that the transformation of the complete thickness of the YBCO layer is not possible, unless a high-enough voltage is applied. Thus, the state variable reaches a minimum, g_{min} , which depends on the applied voltage. It is notable that, although the device-to-device variability is high, the same characteristic features, where found not only within the same sample with different device areas (Figure S2), but across different samples with different thicknesses of the YBCO layer. The notable area dependencies of the hysterons and current-voltage characteristics rule out filamentary switching and support our assumption of homogeneous switching [28, 34]. These features include an abrupt SET transition, if a certain threshold voltage is surpassed and a gradual RESET transition, suitable to program multiple resistive states. The progressive RESET transition has been found both, under ramped voltage stress and pulsed experiments, as shown in Section 2.1. Particularly significant is the fact that the resistance saturates to different values during depression experiments with pulses of different amplitudes. This is fully consistent with the existence of a voltage-dependent minimum value of the state variable, i.e., a voltage-dependent maximum resistance. According to the previous discussion, we explicitly consider that there is a critical electric field in the LRL below which the RESET transition cannot further proceed. This field is given by

$$F_{\text{crit}} = \frac{V_{\text{L}}}{t_{\text{L}}} = \frac{\rho_{\text{L}}}{(1 - g_{\text{min}}) \rho_{\text{H}} + g_{\text{min}} \rho_{\text{L}}} \left(\frac{V}{t_{\text{ox}}} \right) \quad (3)$$

if we define a critical voltage $V_{\text{crit}} = F_{\text{crit}} t_{\text{ox}}$ and the resistance ratio as $r = \rho_{\text{H}}/\rho_{\text{L}} > 1$. Thus, from Equation (3) we can obtain g_{min} , which is given by

$$g_{\text{min}} = \frac{1}{r - 1} \left(r - \frac{V}{V_{\text{crit}}} \right) \quad (4)$$

This equation yields a straight line with the two limits

$$g_{\text{min}}(V) = \begin{cases} 0 & \text{if } V \geq r V_{\text{crit}} \\ 1 & \text{if } V \leq V_{\text{crit}} \end{cases} \quad (5)$$

From Equation (5) it becomes clear, that the HRL can not be formed at all if the applied voltage is below the critical voltage and on the other hand that the whole thickness is transformed into a HRL if the applied voltage exceeds $r V_{\text{crit}}$. This is a piecewise function and for modeling purposes it is convenient to approximate it by a continuous function. For this purpose a logistic function with a smooth transition between the limits

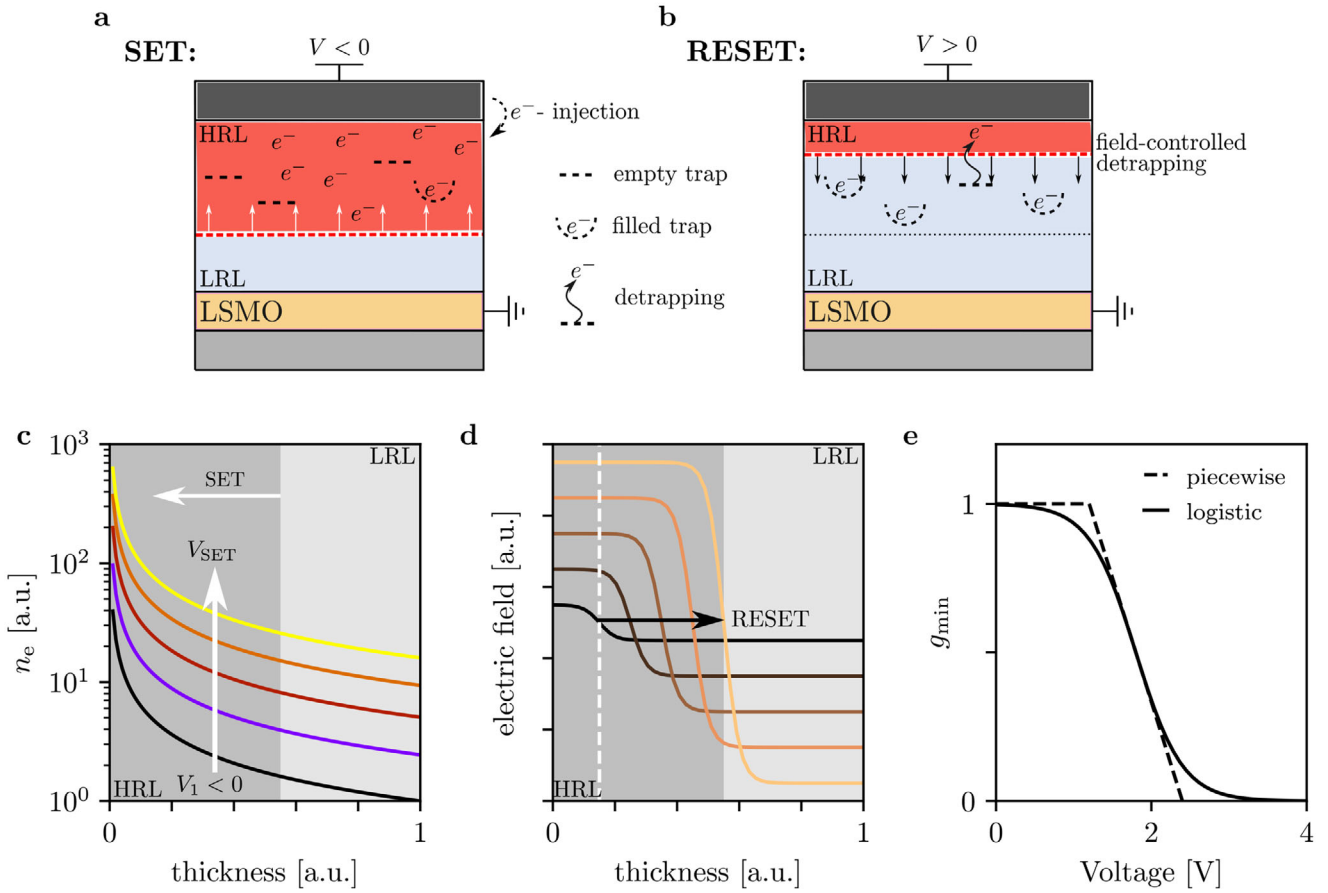


FIGURE 4 | Schematic illustration of the physics-inspired compact model to describe the switching dynamics: (a) negative bias injects electrons, which are captured in traps, leading to an effectively decreasing thickness of the HRL (white arrows) and thus, to a SET transition. The RESET transition is triggered due to detrapping of electrons, through an increasing thickness of the HRL (black arrows) under positive bias in (b). The density of the injected carriers ρ is calculated according to the SCLC for different voltages in (c). Reaching the threshold voltage V_{SET} or a critical density of carriers leads to the SET transition. The development of the field for different t_H and t_L is plotted in (d). Units in (c) and (d) are arbitrary and serve solely to visualize the underlying physical mechanisms proposed in the model. The justification for the approximation of the piecewise, by a logistic function is provided in (e).

$g_{min} = 0$ and $g_{min} = 1$ is proposed as

$$g_{min} = \frac{1}{1 + \exp\left(\frac{V - V_{log}}{\xi}\right)} \quad (6)$$

As shown in Figure 4e, the logistic function of Equation (6) is a good approximation to the piecewise function obtained from the model. Given the simplicity of the physics-based model, the use of the logistic approximation does not represent any limitation and might even be a more realistic description with a smoother transition of the involved phenomena.

Up to this point, we have described the resistance state in a stationary situation. This part of the model provides a simplified description of the switching process, with emphasis in the RESET transition, it allows to define the state variable g and it establishes a voltage-dependent limit g_{min} during RESET. To capture the dynamics of the SET and RESET transitions we introduce a model including two coupled equations. The first equation, called the memory equation, describes the evolution of the state variable, g , and the other one is an expression for the current-voltage charac-

teristics. The memory parameter, g , couples these two equations. For the memory equation, we depart from a differential balance equation previously proposed to describe filamentary switching [50], but incorporating the formerly described limit g_{min} .

$$\frac{dg}{dt} = K_p(1 - g) - H(g - g_{min})K_d(g - g_{min}) \quad (7)$$

The Heaviside function $H(g - g_{min})$ is required to avoid unphysical potentiation when the initial conductance during RESET is smaller than g_{min} . The depression rate K_d and the potentiation rate K_p are modeled as

$$K_d(V) = H(V)K_{d0} \exp(\eta_d V) \quad K_p(V) = H(-V)K_{p0} [G(g)V^{m(g)}]^\alpha \quad (8)$$

K_{p0} and α are fitting parameters for the potentiation rate and K_{d0} and η_d for the depression rate, respectively. The depression rate is considered to depend exponentially on the electric field (voltage), according to the assumption that field-assisted electron detrapping is the underlying mechanism for the RESET transition. On the other hand, as briefly discussed above, the potentiation rate is assumed to be related to the current, which is given by the SCLC

mechanism, in which $I \propto V^m$. As shown in the following section, this is inspired by the fact that the SET voltage depends on the resistance of intermediate states. The exponent α is introduced to give flexibility to the model and, given that it is larger than one (accordingly to the fitting results), the dependence on the voltage is larger than that of the current itself. Thus, as expected, voltage and current may play a role in the SET transition. This is consistent with the fact that the trapping of electrons in oxygen vacancies is related to both the energy and the density of the injected carriers. In the SCLC model, the density of carriers strongly peaks at the injecting interface, as shown in Figure 4c and this supports that trapping of electrons near this interface can explain the SET transition. Here, the Heaviside function, H , is introduced to avoid potentiation for positive voltages and depression for negative voltages, respectively. Interestingly, this allows to separate Equation (7) into two parts which are solved independently by a recursive method. For the SET transition ($V < 0$) the solution yields

$$g_t = [1 - \exp(-K_p \Delta t)] + g_{t-1} \exp(-K_p \Delta t) \quad (9)$$

and for the RESET transition ($V > 0$)

$$g_t = g_{\min} [1 - \exp(-K_p \Delta t)] + g_{t-1} \exp(-K_D \Delta t), \quad \text{if } g_{t-1} > g_{\min} \quad (10a)$$

$$g_t = g_{t-1}, \quad \text{if } g_{t-1} \leq g_{\min}. \quad (10b)$$

Where g_t and g_{t-1} are the values of g at times t and $t - 1$. On the other hand, Δt is the integration time step, defined as the time difference between two consecutive calculation steps. By solving for g using Equations (9) and (10) the equivalent conductance can be calculated

$$G(g) = G_{\max} g + G_{\min} (1 - g) \quad (11)$$

with the maximum conductance $G_{\max} = 1/R_{\min}$ and the minimum conductance $G_{\min} = 1/R_{\max}$. As it will be shown in the following section, $R_{\max}$ and $R_{\min}$ are parameters (the maximum and minimum resistances at the read voltage, as found in the hysteron), which can be extracted experimentally.

The second equation of the compact model should yield the current as a function of the voltage and the state variable. Since it was demonstrated that the conduction is consistent with SCLC, both in the LRS and the HRS, as well as in intermediate states, the voltage dependence of the current is a power law of the voltage [34]. Thus, the current equation is proposed to be

$$I(g, V) = G(g) V^{m(g)} \quad (12)$$

Notice that the dependence on the internal state of the memristor is given by $G(g)$, with the resistance given by $R(g) = 1/G(g)$. Experimentally $m_{\max}$ decreases toward $m_{\min}$ across the development of intermediate states. For this relation we propose a simple linear equation

$$m(g) = m_{\min} g + m_{\max} (1 - g) \quad (13)$$

Based on the introduced model, the calculation of the hysteretic IV -characteristics requires the joint solution of Equations (9), (10) and (12).

2.3 | Model Results

To highlight the capabilities of the model, in this section simulations are compared with experiments. First, in order to justify the functional form of the potentiation rate considered in the model, we deal with the dependence of the SET voltage on the resistance of the intermediate states. Figure 5a shows the SET voltage versus the resistance of intermediate states, prepared by changing the maximum voltage applied during the RESET transition. A clear trend toward lower SET Voltages for lower resistance states is revealed. This behavior can not be captured by a simple exponential dependence on voltage of the potentiation rate. Since, what changes for different resistance states is the current, and the SET transition occurs at smaller voltages for lower resistances, it is reasonable to consider that the potentiation rate depends on the current as assumed in Equation (8). Assuming that there is a critical current I_{crit} that triggers the SET transition, from Equation (12) it follows that the SET voltage depends on g as

$$V_{\text{SET}} = [I_{\text{crit}} R(g)]^{\frac{1}{m(g)}} \quad (14)$$

V_{SET} is arbitrarily defined as the voltage at which the measured resistance drops below 85 % of the initial resistance, R_{init} . In Figure 5a the model is compared with the experimental V_{SET} proving that the trend can be well captured by Equation (14), thus showing the consistency of the approach. This behavior indeed suggests that the current plays a critical role during the SET transition and justifies the introduction of the functional form of the potentiation rate considered in Equation (8). To further compare with experimental results, we will consider matching the model to the experimental hysterons. Therefore, the value of the state variable g , which corresponds to R_{init} , is calculated. Departing from Equation (11) this yields

$$g(R_{\text{init}}) = \frac{R_{\max} R_{\min} - R_{\text{init}} R_{\min}}{R_{\text{init}} R_{\max} - R_{\text{init}} R_{\min}} \quad (15)$$

With R_{init} and $R_{\min}$, extracted from the measurement, and estimating $R_{\max}$ to be around 1.3 M Ω (this resistance cannot be directly determined from the measurements because R_{init} does not saturate to $R_{\max}$). The experimentally obtained hysterons, corresponding to different intermediate states, can be nicely reproduced as shown in Figure 5b. For this purpose $m_{\min} = 3.5$, $m_{\max} = 4.5$, $\alpha = 5$ and $K_{p0} = 5 \times 10^{19}$ were the considered parameters.

To further emphasize the capabilities of the model, the temperature dependent data presented in Figure 2a,b are compared with the model at six different temperatures. For clarity only one temperature is shown in Figure 6a,b in the main manuscript, while the other ones are presented in Figure S3. The fitting parameters are summarized in Table 1. It is clearly demonstrated that the model reproduces the dynamics of the hysteron in Figure 6a and the IV -characteristics in Figure 6b.

Although the IV -curves are rather symmetric with respect to bias polarity (as expected for a bulk-controlled conduction mechanism), a slight asymmetry is always found. Thus, the fitting of the

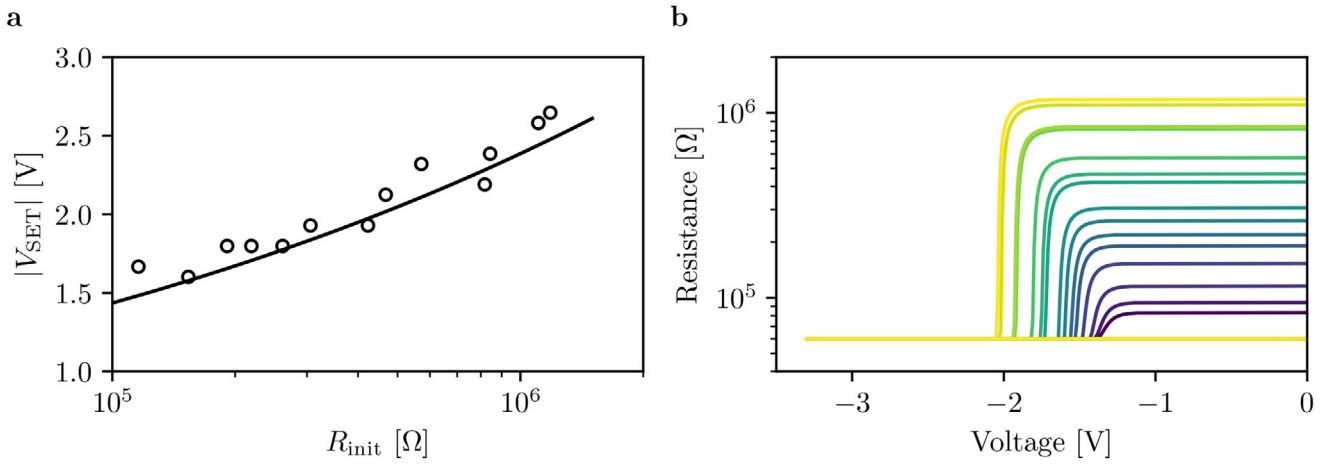


FIGURE 5 | Model potentiation: In (a) open circles represent the extracted SET voltages depending on the initial resistance state. The solid line is calculated according to Equation (14). The development of the potentiation of the hysteron for different intermediate states is given in (b).

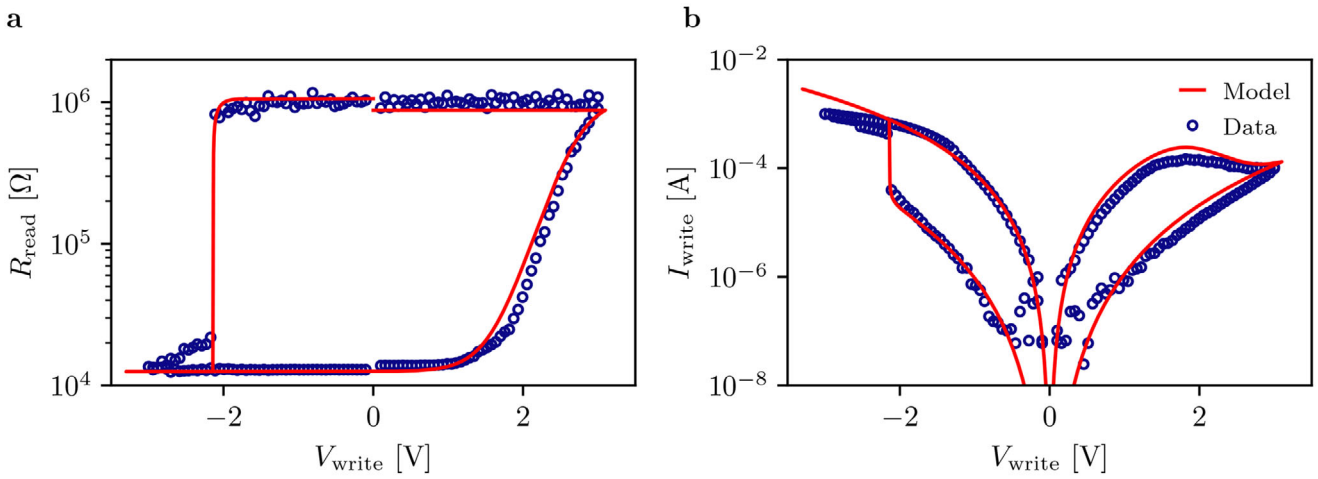


FIGURE 6 | Temperature dependent fitting: The data (open circles) of the hysteron in (a) and the IV -characteristics in (b), collected at 150 K, are compared with the model (solid lines).

TABLE 1 | Model parameters as a function of temperature. The depression rate $K_{d0} = 1.5$, $\eta_d = 0.75$, $\xi = 0.25$ and $V_{log} = 1.6$ were kept constant for all the simulations.

T (K)	m_{max}	m_{min}	$R_{max}(\Omega)$	$R_{min}(\Omega)$	K_{p0}	α
150	4.2	3.0	1.50×10^6	1.25×10^4	1×10^{23}	5
160	4.0	3.0	8.00×10^5	1.30×10^4	1×10^{23}	5
180	3.4	3.4	6.50×10^5	1.60×10^4	4×10^{23}	5
225	3.0	3.0	5.00×10^5	2.00×10^4	7×10^{23}	5
250	3.0	2.9	3.80×10^5	2.80×10^4	1×10^{23}	5
300	2.5	2.5	2.45×10^5	3.50×10^4	2×10^{23}	5

IV -characteristics can be improved by taking into account a slight asymmetry of the conduction for positive and negative bias. This is done considering different values of the power law exponents $m_{max/min}$ and the maximum and minimum resistances $R_{max/min}$. For positive polarity, we consider $(m_{max/min})^+$ and $(R_{max/min})^+$

and for negative polarity $(m_{max/min})^-$ and $(R_{max/min})^-$, respectively. The comparison between experimental results and fitting with polarity-dependent power law exponents is shown in Figure S4. However, there are still some disagreements in the high-current region of the IV -curves and the end of the SET transition of the hysteron (see Figures S3 and S4). In the first case, the current grows faster in the model compared with the experiments. In the second, the model does not capture the final progressive tail of the SET transition but it drops abruptly to the LRS. In this regard, we have checked the role of the series resistance introduced above. When there is a resistance in series to the active switching layer, a part of the applied voltage drops at the series resistance, R_s . The voltage drop is higher if the device is in the LRS and the effective voltage drop at the active layer is reduced to be $V_{eff} = V_{in} - IR_s$. Here V_{in} denotes the total input voltage. Thus, both the balance equation for the state variable in Equations (7) and (8) and the current Equation (12) must be rewritten in terms of the effective voltage. Following this approach Figure S5 reveals that the series resistance can fix the disagreement in the high-voltage region of the IV - characteristics, but it can not

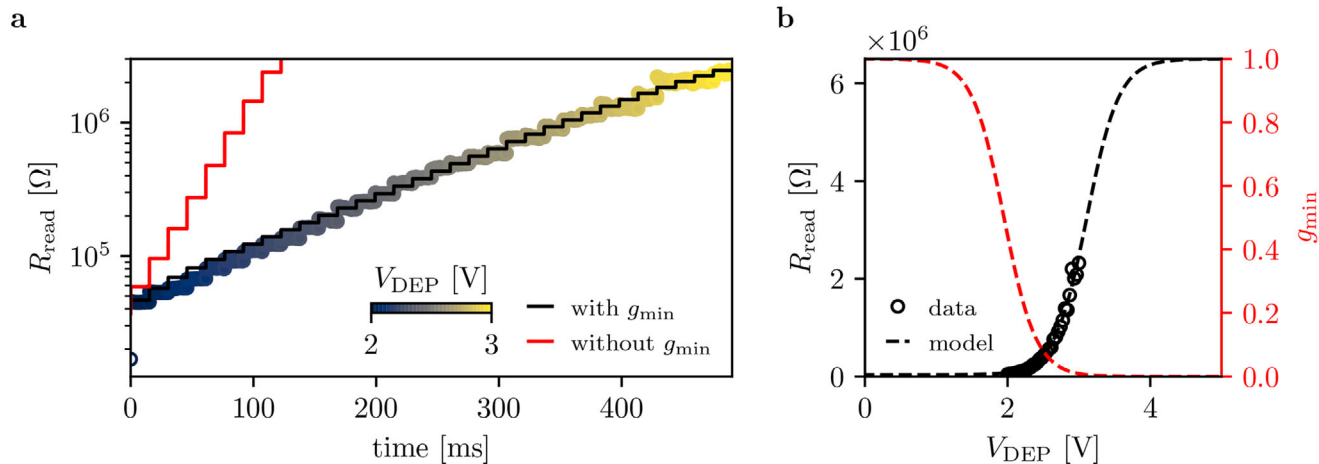


FIGURE 7 | Role of $g_{\min}$ during depression: (a) Progressively increasing resistive states after applying single writing pulses with amplitudes indicated by the color bar. The compact model is fitted to the data both with (black line) and without (red line) accounting for $g_{\min}$ during depression. (b) Resistance states as a function of the applied depression voltage (left axis). Experimental data (open circles) are compared with the model. The logistic function defining $g_{\min}(V)$ is shown in red (right axis).

account for the gradual tail of the hysteron in the last stages of the SET transition. This disagreement could be subject for further investigations.

To conclude the comparison between model and experiments, we emphasize the necessity of $g_{\min}$ to limit the programmed resistive states during the RESET transition. In Figure 3b, the resistance states saturate essentially instantaneously on the experimental timescale. We therefore present an experiment in which the device state is altered with single writing pulses of progressively increasing amplitude, V_{DEP} . In between the depression pulses the stability of the programmed states is assured through reading pulses. This method results in a progressive increase of the resistance states depending on the applied voltage amplitude. As it can be seen in Figure 7a attempts to fit these data without incorporating $g_{\min}$ fail. In contrast, including the logistic function with parameters $V_{\log} = 1.96$ and $\xi = 0.22$ accurately reproduces the resistance evolution shown in Figure 7b. To fit the data it was assumed that $R_{\max}$ is higher than the experimentally observed maximum Resistance, because saturation was not reached during the experiment. The comparison between the resistance limit and the logistic function $g_{\min}$ indicates that the changes of the resistance state are much more sensitive to changes of the memory parameter g , when it approaches zero.

3 | SPICE-Simulation

In the previous sections, we have presented a compact behavioral model to describe the electrical behavior of our YBCO memristors. A compact model is useful to check whether the device characteristics can be reproduced under a series of assumptions. This is certainly useful to extract conclusions about the considered device physics and might suggest changes in the device design and fabrication processes. However, the main goal of compact models is circuit simulation and, although the model can reproduce the device behavior (as we have already demonstrated above), it is not assured that it can successfully

work in the framework of a standard analog circuit simulation framework such as SPICE. Here we demonstrate that our compact model can be seamlessly implemented in LTspice, a widely used SPICE-based circuit simulator owned by Analog Devices.

The LTspice schematic, solving the compact model is shown in Figure 8a. Since SPICE-frameworks natively handle only voltages and currents as output quantities, the equations of the compact model are introduced through behavioral voltage and current sources. Behavioral voltage sources are indicated by the circle labeled “+” and “-,” whereas behavioral current sources are indicated by circles containing arrows. Each variable that depends on the memory parameter g is implemented this way. Thus, $R(g)$ is computed according to Equation (11) at node **R**, while $m(g)$ is defined via Equation (13) at node **m**. The behavioral current source at node **g** solves the differential memory equation (Equation 7), driven by the input voltage at node **v** in the closed circuit. To enable the solution of the model an initial state variable is forced at node **g** by **.ic** directive. The resulting IV -characteristics are obtained from the behavioral current source in the closed mesh, which is excited for simplicity by a sinusoidal input function. The use of a sinusoidal signal is straightforward in SPICE and, in our case, it plays exactly the same role as the voltage ramped loops used in our experiments. The fitting parameters are introduced using **.params** and the auxiliary functions, those independent of g , are defined using **.func**.

The simulation results obtained from the schematic in Figure 8a are depicted in Figure 8b. To further verify the compatibility of the compact model with LTspice, a second, more complex input signal is simulated in Figure 8c. In this case, negative voltages are generated by a simple sinusoidal function with fixed amplitude, while positive voltages follow an exponentially damped sinusoidal waveform. The case of this damped sinusoidal is particularly interesting, because it shows that the SPICE implementation reproduces the experimentally observed intermediate states and the V_{SET} dependence on the intermediate state resistance. Since both input signals are processed without

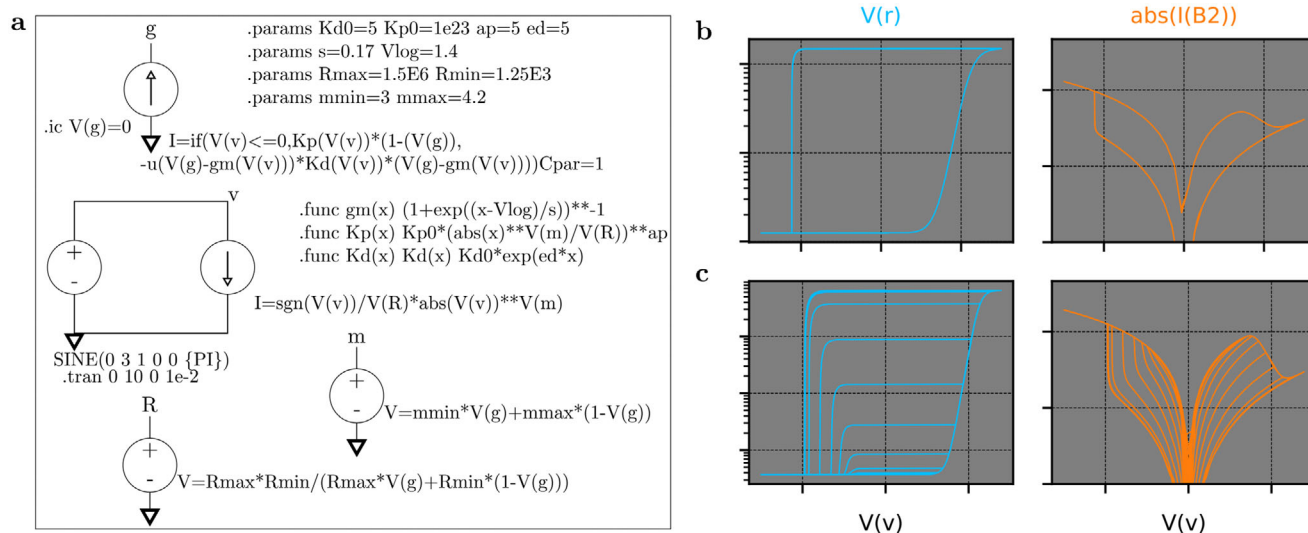


FIGURE 8 | LTspice Simulations: (a) Implementation of the compact model into a LTspice schematic. The diagram is explained in more detail in the main text. Simulation results of the hysteron $V(r)$ and the IV -characteristics $abs(I(B2))$ depending on the input signal $V(v)$ are given for a simple sinusoidal input signal in (b) and a damped waveform in (c).

numerical divergence, the implementation is expected to remain stable for arbitrary input waveforms. The complete netlists used to generate the results in Figure 8b,c are provided in Figure S6.

The presented results confirm that our compact model is perfectly suitable for its implementation in standard analog circuit simulation environments such as SPICE. The obtained results are in full agreement with those obtained numerically in custom-designed Python code and presented in the previous section. In particular, we have reproduced the resistance hysteron, the IV loop, intermediate resistance states and the reduction of V_{SET} with decreasing resistances of intermediate states programmed by changing the maximum positive voltage applied for RESET (damped sinusoidal waveform).

4 | Conclusions

The resistive switching behavior of YBCO-based memristors has been investigated over a wide temperature range for devices with different YBCO thickness. Based on the temperature and thickness independent SET and RESET voltages, a charge-trapping/detrapping related switching mechanism is discussed. Trapped electrons in oxygen vacancies of broken CuO-chains may lead to an enhanced interlayer-coupling between copper-oxide-planes, thereby triggering a resistive switching event. Building on this material-specific interpretation a more generalized physical picture is introduced.

For the SET transition, this generalized picture takes into account that the governing conduction mechanism of the devices in the HRS/LRS is SCLC. According to SCLC the density of injected carriers peaks at the injecting electrode and thus, the abrupt SET transition occurs, if a certain threshold voltage is surpassed and carriers are trapped in the HRL. We incorporate this fact into the model by defining a potentiation rate, which reflects the power-law dependence of current on voltage.

The gradual RESET transition is linked to the electric field distribution within a bilayer system comprising high- and low-resistance regions. To ensure graduality during reset a limiting factor stemming from a critical electric field in the LRL, restricting detrapping, is proposed. Both of these physical pictures are introduced into a compact model with two main components: a differential balance equation describing the SET/RESET dynamics and an algebraic equation for the current-voltage characteristics based on the SCLC model.

To highlight the capabilities of the developed compact model, simulation results are directly compared with the experimental observations. First, using the introduced potentiation rate, the model successfully reproduces the experimentally observed evolution of the SET voltage for different intermediate resistance states. Subsequently, the hysteron and IV -characteristics are accurately fitted over a wide range of temperatures. The extracted fitting parameters indicate that the temperature dependence originates primarily from changes in the conduction mechanism rather than from the switching process itself. Finally, the necessity of a limiting factor during RESET is demonstrated by comparing pulse-based saturated and progressive depression experiments. The model fails to describe the progressive experiments when this limiting mechanism is omitted, whereas incorporating a logistic function for the minimum value of the state variable as a function of the applied voltage allows the memory parameter's dependence on the applied depression voltage to be reproduced with high accuracy. It should be stated that, given the complexity of the materials involved, modeling the system as a bilayer composed of a LRL and a HRL represents an oversimplification of the underlying microscopic mechanisms. A more detailed understanding of the conduction processes in the LRS is necessary to develop a more accurate physical picture of the gradual RESET transition.

The results are complemented by the implementation of the compact model in LTspice. Two different input signals are simulated as a proof of concept, demonstrating the suitability

of the compact model for circuit-level simulations. Finally, we note that the proposed model is a behavioral one, capable of responding to arbitrary input signals. Although it was developed on the basis of experiments in YBCO, it can be adapted to other memristive materials, as the physical assumptions embedded in the model are intentionally simplified—given the complexity of the materials involved—to ensure compatibility with circuit simulations. Consequently, its quantitative predictive accuracy is limited. Nevertheless, the model provides a mathematical framework for quantitative studies of hysteretic behavior and can support both the design of future YBCO-based memristors and the interpretation of the underlying physical mechanisms.

5 | Methods

5.1 | Thin Film Growth

La_{0.7}Sr_{0.3}MnO₃ thin films, with a thickness of 30 nm, were grown by off-axis radio frequency sputtering on (001)-oriented SrTiO₃ single-crystal substrates. During growth the temperature is kept constant at 850°C with a pressure of ≈ 20 mbar with constant Argon (2 sccm) and Oxygen (20 sccm) flow. Annealing was performed at 850°C and 500 mbar in a pure oxygen atmosphere for 1 h. The epitaxial 30, 50, and 100 nm thick YBCO films were grown, ex situ, by pulsed laser deposition (PLD). Substrates were heated up to 810°C, with an oxygen partial pressure of 0.3 mbar and a distance of 52.5 mm from the target. Ablation of the target material is induced by a high fluence laser (≈ 2 J/cm²) working at a frequency of 5 Hz. During cool down to room temperature, the sample is kept in an oxygen atmosphere of 1 bar to ensure proper oxygenation of the deposited thin films [20]. Gold electrodes of 100 nm thickness were deposited in a TSST sputtering system. Insulating Alumina films are deposited at 150 °C in a *Atomic Layer Deposition System Savannah from Cambridge NanoTech*. Standard fabrication techniques were used to pattern the memristors [28].

5.2 | Voltage Pulses

Voltage pulses: The pulse trains described in the main section were generated using *Keithley 2604B and 2601 Source Measure Units* (SMUs), controlled by a custom measurement software. Measurements at cryogenic temperatures were carried out either in a *Quantum Design PPMS System* or in a *Lake Shore VPF-100* cryostat.

5.3 | Simulation

Simulations were performed using LTspice (version 24.1.10) and a homemade Python script.

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Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Supporting Information

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