

Algorithmic Exploration of Matching Network Topologies for Power Amplifiers

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Abstract—In this article, a novel exploration algorithm for the design and optimization of matching networks (MNs) in power amplifiers (PAs) is presented. The methodology is based on the automatic generation and optimization of both input and output MNs (IMNs/OMNs) according to a set of design rules and constraints that ensure technological feasibility. All candidate MN topologies are optimized and ranked using a unified cost function, enabling the automatic selection of the most suitable solution while facilitating a comprehensive tradeoff analysis among key performance metrics such as power-added efficiency (PAE), gain, bandwidth, physical size, and expected yield. As a result, the designer obtains a global view of the solution space and can objectively compare different MN configurations within a consistent optimization framework. To validate the proposed algorithm, a PA covering 1.1–1.9 GHz—fully encompassing the Galileo navigation bands E5, E6, and L1—and targeting high efficiency with harmonic control, was designed, fabricated, and experimentally characterized.

Index Terms—Cost function, GaN, harmonic control, harmonic matching, high efficiency, matching networks (MNs), non-Foster impedance, optimization techniques, power amplifier (PA), topology optimization.

I. INTRODUCTION

ONE of the main challenges in power amplifier (PA) design is defining appropriate criteria for selecting the input and output matching network (IMN/OMN) once the transistor has been chosen to deliver the required output power. A key question arises when deciding which topology is better suited for wideband or narrowband matching to maximize power-added efficiency (PAE) and output power over the desired frequency range. This challenge becomes even more complex when additional constraints, such as compact size, specific output power levels, or efficiency requirements across the entire band, must be satisfied. In practice, these decisions are often based on the designer's experience rather than on a systematic methodology. In the literature, active techniques to enhance PAE, such as supply modulation and load modulation, have been widely investigated [1]. In contrast, this article focuses exclusively on passive solutions, specifically addressing the design of the IMN and OMN.

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Impedance and admittance circles on the Smith Chart (SC) are effective tools for narrowband PA design. However, as the operating bandwidth increases, the design complexity grows significantly, making the process highly time-consuming. To address this limitation, a new algorithm for the automatic generation and evaluation of the MN to obtain good initial candidates for layout optimization.

Several works employ algorithmic approaches for matching network (MN) synthesis, such as those based on the simplified real frequency technique (SRFT) and the real frequency technique (RFT) [2], [3], [4]. As in most synthesis methods, prior knowledge of the topology and frequency response is required to extract the element values. In addition, these techniques mainly rely on lumped elements, which typically exhibit limited performance for large fractional bandwidths. The use of distributed elements to implement reactive components may also introduce transmission-line (TL) periodicities within the band of interest, which becomes critical when harmonic matching is considered.

In the SRFT and RFT, the topology is evaluated only after synthesis and cannot account for structures with cross-coupling [5], multipath [6], or multibranch configurations [7]. In contrast, the proposed algorithm enables parallel concatenation of elements such as TLs/capacitor and avoids nonfeasible topologies by imposing boundary conditions before optimization; therefore, it is primarily used as a topology exploration tool. Other optimization approaches, such as Bayesian methods, rely on predefined topologies, including Chebyshev or step-impedance structures [8], [9], [10], [11], which inherently limit the design flexibility to a single topology.

Layout-level optimization techniques have also been reported using commercial tools or full-wave electromagnetic (EM) solvers [12], [13]. Although effective, these approaches typically require long simulation times. Deep-learning-based methods have also been proposed [14], [15], but they demand significant expertise and training effort, with optimization times ranging from days to weeks. Moreover, retraining is required whenever the transistor technology changes, which limits their flexibility.

In contrast, the proposed exploration tool can be implemented in MATLAB and can be easily adapted to open-source programming languages. Its main novelty lies in the ability to rapidly evaluate thousands of candidate topologies per hour without relying on EDA software, providing an efficient starting point for PA layout optimization. Additionally, the method supports hybrid MNs combining distributed and

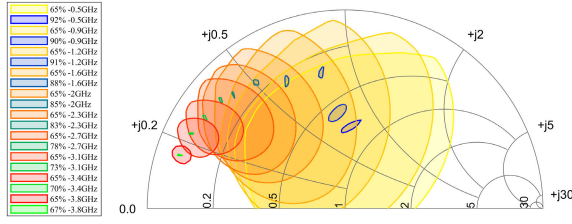


Fig. 1. Constant PAE contours at maximum and 65% for the MACOM CG2H40010F transistor from 0.5 to 3.8 GHz.

lumped elements, including biasing and stabilization circuits. This capability enables large-scale topology exploration, with evaluation times of less than one hour for topologies with ten elements, demonstrating a clear advantage in speed over existing approaches. The objective is to establish a systematic and automatic topology-evaluation system: topologies are generated, filtered, optimized, and ranked under common constraints.

This article is organized as follows. First, the main challenges in PA design are discussed, including non-Foster impedance behavior and harmonic overlapping, to provide context for the proposed optimization method. Next, the algorithm is introduced and divided into four main stages: input data and design constraints, topology generation and filtering, topology optimization and evaluation, and result analysis. The particularization of the wideband cost function is then presented. Using the proposed algorithm, a PA focused on harmonic control with a relative bandwidth of 53% is designed, fabricated, and experimentally characterized. Finally, the conclusions are presented.

II. DESIGN CHALLENGES IN PAS

A. Non-Foster Impedance Behavior

One of the main challenges in wideband PA design is the non-Foster impedance trajectory exhibited by many transistors, such as GaN devices, as reported in [16] and [17]. As shown in Fig. 1, these impedances rotate counterclockwise on the SC, whereas passive MNs inherently produce a clockwise rotation due to their passive nature, as described by the reactance theorem [18]. Consequently, identifying an MN topology capable of accommodating the non-Foster impedance trajectory is essential to achieve wide operational bandwidths while minimizing the number of series and shunt TL elements. Fig. 1 shows the load—pull impedances for PAE from 0.5 to 3.8 GHz, assuming optimal second- and third-harmonic terminations and recalculating the fundamental after loading the harmonics. As frequency increases, the 65% PAE contours shrink, making it increasingly difficult for the MN to achieve the required impedance match for wideband operation.

B. Harmonic Overlapping

The challenge of matching non-Foster impedances becomes more pronounced when PAE enhancement is pursued through harmonic matching. In high-efficiency PA design, the achievable bandwidth is inherently limited by the deliberate manipulation of harmonic terminations required to improve efficiency. Consequently, as higher efficiency levels are

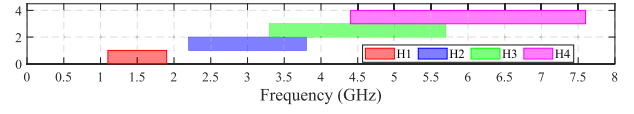


Fig. 2. Harmonic overlap, the fundamental in red (1.1–1.9 GHz), second harmonic in blue (2.2–4.4 GHz), third in green (3.3–6.6 GHz), and fourth in magenta (4.4–8.8 GHz).

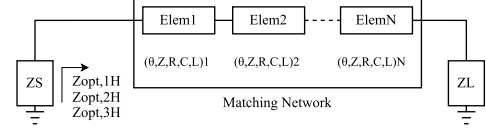


Fig. 3. Core block diagram of the algorithm based on the concatenation of ABCD matrices.

TABLE I
ELEMENTAL ELEMENTS TO BUILD THE MNS

	$[ABCD] = \begin{bmatrix} 1 & Z \\ 0 & 1 \end{bmatrix}$ (1)
	$[ABCD] = \begin{bmatrix} 1 & 0 \\ Y & 1 \end{bmatrix}$ (2)
	$[ABCD] = \begin{bmatrix} \cos(\beta l) & jZ_0 \sin(\beta l) \\ jY_0 \sin(\beta l) & \cos(\beta l) \end{bmatrix}$ (3)
	$[Y_T] = [Y_1] + [Y_2]$ (4)

targeted, the MN must simultaneously satisfy fundamental and harmonic impedance conditions, further constraining bandwidth performance. This spectrum limitation can be expressed as $f_{\text{high}}(1H) < f_{\text{low}}(2H)$, meaning that the second harmonic of the lower band-edge frequency must lie above the upper band-edge frequency of the fundamental, thereby avoiding in-band overlap of the second harmonic, as illustrated in Fig. 2. Within the frequency ranges 3.3–3.8 GHz and 4.4–5.7 GHz, the load impedance cannot simultaneously satisfy the harmonic terminations required for high-efficiency operation, such as Class F, inverse Class F, continuous Class F [19], or inverse continuous Class F, due to harmonic overlapping.

III. AUTOMATIC TOPOLOGY SEARCHER FOR THE DESIGN OF THE MNS

The core of the algorithm is the evaluation of all feasible MN topologies for PA design, selecting the best solution based on a defined cost function. The algorithm leverages the properties of the $[ABCD]$ and $[Y]$ matrices to provide a systematic and automatic tool for topology optimization, as illustrated in Fig. 3. This procedure enables a fair, fast, and efficient comparison among different solutions. All possible elements that may constitute the MN are constructed from the elemental blocks listed in Table I, including parallelly connected structures. This approach allows the use of lumped and/or distributed elements in the search for the optimal network.

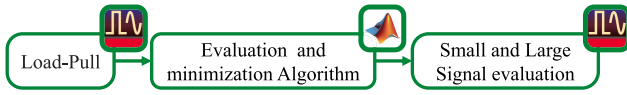


Fig. 4. Block diagram of the interface between MATLAB and ADS for the proposed algorithm.

Since the fundamental impedance exhibits non-Foster behavior and, in high-efficiency designs, the achievable bandwidth is further limited by harmonic overlap, the algorithm adopts an optimization method based on the joint minimization of reflection-coefficient magnitude and phase to address both challenges simultaneously.

MATLAB is used for implementation as an interface between the advanced design system (ADS) load—pull data extraction and ADS large-signal simulation. The extracted load—pull data is exported to MATLAB, where a massive topology generation and evaluation framework is implemented. Within this framework, candidate MN topologies are automatically generated and assessed. The selected topologies are then evaluated under large-signal conditions using the nonlinear transistor model in the ADS. The overall design and evaluation procedure is illustrated in Fig. 4.

The algorithm is divided into four main blocks.

- 1) *Input Data and Design Constraints*: This block defines the input data, including the load—pull impedances, as well as the PA design constraints that must be satisfied, such as maximum device ratings, power-handling limits, and bias conditions.
- 2) *Generation and Filtering of Feasible Topologies*: In this block, all candidate MN topologies are generated. Non-feasible solutions are filtered out based on realizability criteria and predefined technological constraints.
- 3) *Topology Optimization*: Each feasible topology is then optimized using the defined cost function, taking into account the selected performance metrics and, when applicable, nonlinear constraints.
- 4) *Data Sorting and Visualization*: Finally, the optimized solutions are ranked according to their cost-function values, and the results are organized and visualized to facilitate comparison and analysis.

A. Input Data and Design Constraints

The input data of the algorithm consists of the load—pull impedance vector extracted from the nonlinear transistor model. This impedance is defined as a frequency-dependent vector specified by the designer. It can be chosen to target maximum PAE, maximum gain, an intermediate tradeoff, or operating points that provide improved performance in back-off. In this work, the selected fundamental impedance corresponds to the maximum PAE points for a constant input power, obtained by recalculating the fundamental load—pull while simultaneously loading the second and third harmonics at their respective optimal frequencies.

The MN optimization is performed using the MATLAB `fmincon` function, which carries out constrained nonlinear optimization by minimizing a user-defined cost function subject to equality, inequality, and bound constraints. Within this

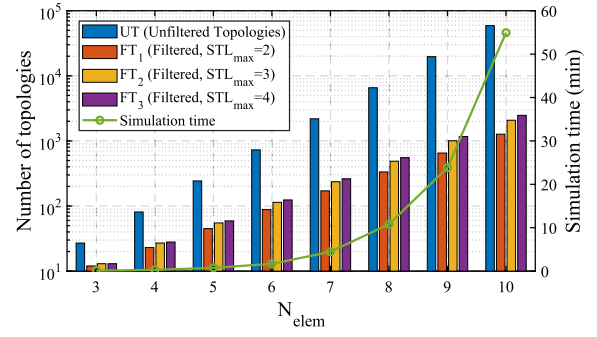


Fig. 5. Number of topologies and simulation times as a function of the number of elements that form the MN N_{elem} .

framework, lower and upper bounds must be specified for all design variables. These bounds define the feasible design space and correspond to the minimum and maximum physical dimensions of the elements, including electrical lengths and characteristic impedances of TLs, as well as capacitance and inductance values for lumped elements.

Electrical lengths (θ_{min} , θ_{max}) referenced to a central frequency f_c and characteristic impedances (Z_{min} , Z_{max}) can be limited to specific values depending on the substrate properties and power-handling requirements.

B. Topology Generation

The next step of the algorithm is the generation of MN topologies, followed by a filtering stage based on a predefined set of constraints. To enable this process, each topology is defined through a numerical codification scheme, where a series TL (STL) is represented by 0, a shunt open-stub (SOS) TL by 1, and a shunt short-stub (SSS) TL by 2. Each element in the topology is thus uniquely encoded, and different topologies are generated through the concatenation of these codes. Initially, all topologies are generated sequentially rather than randomly, ensuring that no possible solutions are omitted. In this way, each topology is uniquely defined through the concatenation of the encoded elements. Additional elements, such as lumped components, can be incorporated by extending the codification with new codes.

The total number of generated topologies directly impacts the computational cost, as it translates into simulation time. Therefore, particular emphasis is placed on the topology-generation algorithm. All possible codes are first generated and then filtered by eliminating those that do not satisfy a predefined set of feasibility rules. With this approach, only realizable and meaningful topologies are passed to the optimization stage.

As the number of elements in the topology increases, the dimensionality of the problem grows rapidly. This effect is illustrated in Fig. 5, where it can be observed that the number of unfiltered topologies (UTs) exhibits exponential growth. This behavior highlights the importance of the filtering process to keep the problem computationally tractable

$$N_{top} = A_{elem}^{N_{elem}}. \quad (5)$$

Fig. 5 shows the number of possible topologies as a function of the number of elements in the MN. Equation (5) formulates

TABLE II

SIMULATION TIMES AS A FUNCTION OF THE NUMBER OF TOPOLOGIES AND THE NUMBER OF ELEMENTS

N_{elem}		3	4	5	6	7	8	9	10
Num. of Top.	UT	27	81	243	729	2187	6561	19683	59049
	FT ₁	12	23	45	88	171	334	651	1269
	FT ₂	13	27	55	114	236	487	1006	2079
	FT ₃	13	28	59	124	262	554	1170	2471
Time	AT (s)	0.503	0.633	0.775	0.805	1.022	1.170	1.222	1.334

FT: Filtered Topologies, UT: Unfiltered Topologies

AT: Average Time of simulation for each topology,

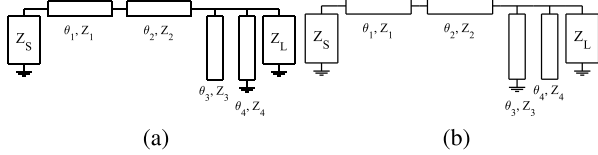
FT₁ are when $STL_{max} = 2$, FT₂ when $STL_{max} = 3$ and FT₃ when $STL_{max} = 4$ 

Fig. 6. Redundant topologies coded as (a) [0, 0, 1, 2] and (b) [0, 0, 2, 1], where 0 denotes an STL, 1 denotes a shunt open-circuit stub, and 2 denotes a shunt short-circuit stub.

the total number of UTs, where A_{elem} represents the set of available elements used to build the MN (e.g., STL, SOS, and SSS). In the proposed case, $A_{elem} = 3$, while N_{elem} denotes the total number of elements used to design the MN.

The total number of UTs is reported in Table II, where the worst case scenario corresponds to $N_{elem} = 10$, with no topology filtering applied. The total simulation time can be estimated by multiplying the average evaluation time per topology (1.334 s) by the total number of topologies, $N_{top} = 59\,049$, resulting in approximately 22 h.

Fig. 6 illustrates an example of redundant topologies, where two different codifications lead to an identical MN structure. This redundancy grows exponentially as the number of elements in the MN (N_{elem}) increases. As shown in (6), eight different codes can represent the same topology, since adjacent shunt open and SSSs can be permuted without altering the electrical behavior of the network, provided that their values are kept constant. This observation motivates the need for topology filtering

$$\begin{aligned}
 &[1, 2, 0, 1, 2, 0, 1, 2] & [2, 1, 0, 2, 1, 0, 2, 1] \\
 &[1, 2, 0, 1, 2, 0, 2, 1] & [2, 1, 0, 2, 1, 0, 1, 2] \\
 &[1, 2, 0, 2, 1, 0, 1, 2] & [2, 1, 0, 1, 2, 0, 2, 1] \\
 &[1, 2, 0, 2, 1, 0, 2, 1] & [2, 1, 0, 1, 2, 0, 1, 2]. \quad (6)
 \end{aligned}$$

To significantly reduce the evaluation time, nonfeasible and redundant topologies are eliminated before optimization.

The rules applied in the algorithm to filter out undesired topologies are summarized in Algorithm 1.

N_{STL} in Algorithm 1 denotes the maximum allowed number of STLs, accounting for step-impedance MNs. After applying the proposed filtering rules, the simulation time is recalculated for the three filtered cases listed in Table II, resulting in total simulation times of 0.47 h (FT₁), 0.77 h (FT₂), and 0.91 h (FT₃), respectively. Fig. 5 and Table II compare the number of evaluated topologies when considering all possible configurations and when retaining only feasible topologies for $N_{STL} = 2, 3$, and 4. Even in the worst case scenario, corresponding

Algorithm 1 Filtering Rules for Feasible Topologies

Generate all UT codes based on available elements (STL, SOS, SSS, lumped elements)
for each generated topology **do**
 if more than two adjacent shunt stubs (open and/or short) are concatenated **then**
 Discard topology
 end if
 if more than N_{STL} STLs are concatenated **then**
 Discard topology
 end if
 if two lumped elements (capacitors and/or inductors) are the same and appear consecutively and share the same connection nodes **then**
 Discard topology
 end if
 if topology is equivalent to an existing one due to permutation of shunt-connected elements **then**
 Discard topology (redundant)
 end if
end for
Store remaining topologies as feasible topologies

to FT₃, the total simulation time remains below 1 h for 2471 evaluated topologies, demonstrating the effectiveness of the proposed filtering strategy.

Different types of elements can be included to build the MNs, such as parallelly connected structures (e.g., parallel RC series networks) or some complex structures, such as the coupled-structure block presented in [5]. Additionally, certain elements, such as DC blocks or biasing lines, can be fixed at predefined positions to satisfy specific design constraints.

C. Topology Evaluation and Optimization

Once the feasible topologies have been identified, they are subsequently evaluated and optimized. The complete algorithmic workflow is illustrated in the block diagram shown in Fig. 7. The optimization process is carried out using the MATLAB `fmincon` function, which is a gradient-based nonlinear optimizer that minimizes a user-defined cost function subject to bound and constraint conditions. In this work, the sequential quadratic programming (SQP) algorithm is employed, which solves a sequence of quadratic subproblems that locally approximate the original nonlinear optimization problem. At each iteration, the objective function is approximated by a quadratic model, while the constraints are linearized, providing fast convergence and robust performance for smooth, constrained optimization problems such as the one addressed in this study. All candidate networks are compared with identical optimization settings, so the ranking reflects the method rather than manual tuning.

For a given network, the first step consists of defining the upper and lower bound vectors, ub and lb , respectively, as given in (7a) and (7b). These bounds define the feasible range of the design variables and are directly related to the physical limitations of the elements constituting the MN.

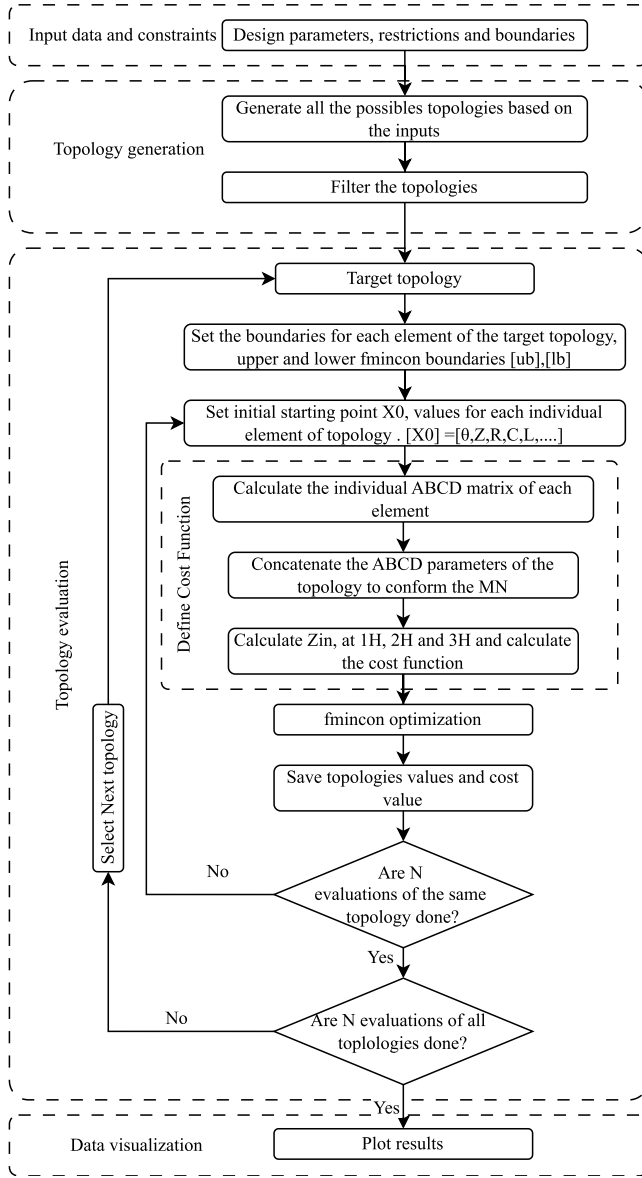


Fig. 7. Block diagram overview of the algorithm.

Next, an initial starting point X_0 for the `fmincon` optimization is selected within the interval defined by lb and ub . The starting points are randomly generated, although they may also be explicitly defined by the user. To reduce the likelihood of convergence to local minima, each topology is evaluated multiple times using different initial conditions. By performing N_{eval} optimization runs per topology with distinct starting points X_0 , the probability of identifying the global minimum is significantly increased. The vector X_0 , containing the initial values of the optimization variables illustrated in Fig. 3, is defined in the following equations:

$$ub = [\theta_{max}, Z_{max}, \theta_{max}, \theta_{max}, Z_{max}, \dots, \theta_{max}, Z_{max}] \quad (7a)$$

$$lb = [\theta_{min}, Z_{min}, \theta_{min}, \theta_{min}, Z_{min}, \dots, \theta_{min}, Z_{min}] \quad (7b)$$

$$X_0 = [\theta_1, Z_1, \theta_1, \theta_2, Z_2, \dots, \theta_n, Z_n]. \quad (7c)$$

D. Cost Function

The defined cost function to be minimized is the one proposed in (8). As can be observed, the cost function can be

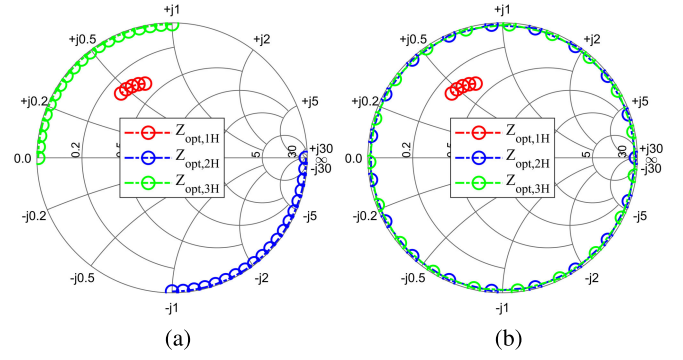


Fig. 8. Harmonic matching conditions: (a) predefined regions for the second and third harmonics and (b) matching based on the magnitude of the harmonics.

decomposed into three terms corresponding to the fundamental, second, and third harmonics. Each harmonic is associated with a weighting coefficient; these coefficients (α , β , and γ) represent the relative contribution of each harmonic to the total cost function. In the wideband case, where harmonic components fall within the operating band, β and γ are set to zero to suppress harmonic matching

$$\min(\Delta\Gamma_T) = \alpha\Delta\Gamma_{1H} + \beta\Delta\Gamma_{2H} + \gamma\Delta\Gamma_{3H}. \quad (8)$$

As explained in Section I, there are two main challenges in the design of PAs: the non-Foster impedance trajectory and the overlap of harmonic components. To address these issues, a methodology based on magnitude and phase control is proposed. As depicted in Fig. 8(a), a traditional approach for designing high-efficiency PAs is illustrated, where target impedances are defined for the fundamental (red), second (blue), and third (green) harmonics. In this approach, the harmonic impedances are imposed as mandatory conditions, and an MN that satisfies these conditions must be synthesized. In Fig. 8, the proposed approach is presented, where the fundamental remains identical, and the second and third harmonics have an extra degree of freedom to lie in the unitary circle of the SC, which allows an overlap of the harmonics and permits exploring other types of configuration and topologies. This methodology will be discussed and demonstrated throughout the article. Setting priority on the magnitude rather than forcing the second and third harmonics to lie at specific points on the SC relaxes the design constraints, enabling bandwidth enhancement

$$\Delta\Gamma_d = \frac{1}{N_s} \sum_{i=n_1}^{N_k} \omega_{f,i} \left[\omega_{ph} \cdot \left| \frac{\angle\Gamma_{in,50\Omega}(f_i) - \angle\Gamma_{opt,50\Omega}(f_i)}{360} \right| + \omega_{mag} \cdot \left| |\Gamma_{in,50\Omega}(f_i)| - |\Gamma_{opt,50\Omega}(f_i)| \right| \right]. \quad (9)$$

The cost function of each harmonic (9) is defined as the difference between the optimum reflection coefficient, $\Gamma_{opt,50\Omega}$, obtained from load—pull simulations at maximum PAE, and the input reflection coefficient provided by the OMN, $\Gamma_{in,50\Omega}$, both normalized to 50Ω calculated using (10). Here, n_1 and N_k denote the initial and final frequency indices, respectively, over which the cost function is evaluated. That is, the matching

is performed at each frequency point based on the optimum impedance variation with frequency

$$\Gamma_{opt,50\Omega} = \frac{Z_{opt} - 50}{Z_{opt} + 50}, \quad \Gamma_{in,50\Omega} = \frac{Z_{in} - 50}{Z_{in} + 50}. \quad (10)$$

To compute $\Gamma_{in,50\Omega}$, several intermediate steps are required. First, the individual ABCD matrix of each building block is calculated according to Table I using the corresponding values of X_0 (7c). Once the individual [ABCD] matrices are obtained, the overall ABCD matrix of the MN is computed by multiplying each individual matrix. This matrix is then used to calculate the input impedance of the MN through standard ABCD-to-impedance conversions, as described in [20].

The minimization is performed in terms of magnitude and phase rather than real and imaginary components, since this representation provides a better-bounded optimization space. Specifically, magnitude and phase are constrained between 0 and 1, and the phase difference is normalized by dividing by 360° . In contrast, the real and imaginary parts of the impedance span the ranges $[0, \infty)$ and $(-\infty, \infty)$, respectively, where N_s denotes the number of samples. This term is introduced to evaluate the fundamental, second, and third harmonics under equivalent conditions, since their corresponding bandwidths are not identical. The factor $\omega_{f,i}$ is a weighting coefficient applied to the fundamental component to compensate for the increased difficulty of matching higher impedance levels, which arises because constant-efficiency circles shrink as frequency increases, as illustrated in Fig. 1.

For the proposed case of high-efficiency PAs, where harmonics are considered, and the bandwidth is relatively narrow, this weighting factor can be omitted since the number of frequency points is reduced. However, it plays a significant role in wideband designs, where impedance matching becomes increasingly challenging at higher frequencies.

E. Wideband Particularization

The particularization for the wideband domain is addressed, that is, when the harmonic frequencies fall within the operating band. First, it should be noted that in (8), the weighting factors are set to $\alpha = 1$, $\beta = 0$, and $\gamma = 0$, meaning that harmonic control is not considered in this scenario. Additionally, the frequency weighting factor $\omega_{f,i}$ in (9) is applied as it is depicted in Fig. 9. This weighting emphasizes frequency regions where the PAE circles become smaller, assigning them a higher impact on the optimization process. This approach is consistent with the methodologies presented in [17], where the same algorithm is employed to design wideband PAs.

F. Data Sorting and Visualization

Once the algorithm has evaluated all topologies N_{eval} times, the results are sorted and exported as .s2p files for large-signal evaluation in the ADS. To illustrate the behavior of the proposed cost function and the impact of the number of elements in the MN, the following example is presented.

1) *Proposed Example:* A PA with a 53% relative bandwidth (1.1–1.9 GHz) is designed to cover all Galileo satellite navigation bands, including E5, E6, and L1. An OMN is optimized

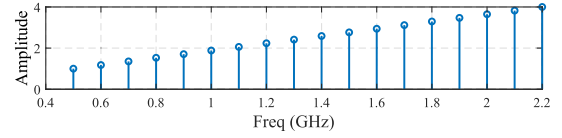


Fig. 9. Weighting factor wideband cases $\omega_{f,i}$.

using the optimum PAE load impedances, as illustrated in Fig. 1. The theoretical maximum achievable bandwidth without harmonic overlap is 1.0–2.0 GHz. Considering the finite quality factor (Q) of the TLs, a guard band between 1.9 and 2.2 GHz is introduced between the fundamental and the second harmonics.

Due to the substrate permittivity and the power levels involved, the electrical lengths are constrained to the range $\theta_{min} > 15^\circ$ and $\theta_{max} < 120^\circ$ at the design frequency $f_{design} = 1.5$ GHz, which corresponds to the center of the band f_c , while the characteristic impedances are limited to $Z_{min} > 20 \Omega$ and $Z_{max} < 80 \Omega$. The upper bound on the electrical length is imposed to prevent the MN from becoming excessively large. This constraint implicitly excludes 180° short- and open-circuited resonators. Although such resonators are commonly used for harmonic control, they would result in TL sections that are excessively long for the targeted substrate and frequency range, making them impractical for compact, high-power implementations.

The algorithm is executed to evaluate all feasible topologies with $N_{elem} = [4 \text{ to } 8]$ elements. All MNs are evaluated under identical conditions, with weighting factors yielding the best PAE flatness over the bandwidth experimentally determined as $\alpha = 0.7$, $\beta = 0.15$, and $\gamma = 0.15$ in (8). The optimum fundamental impedance is defined according to the load–pull simulation results, with weighting factors $\omega_{ph} = 0.15$ and $\omega_{mag} = 0.85$ for the fundamental component. For the harmonic components, only the magnitude of the input reflection coefficient is optimized ($\omega_{mag} = 1$), while the phase weighting factor ω_{ph} in (9) is set to zero, and $\Gamma_{opt,50\Omega}$ is fixed to 0.98. This ensures that the harmonic impedances follow the unit circle, providing a high-reflection condition without imposing a strict phase requirement.

Each topology was evaluated $N_{eval} = 20$ times to avoid convergence to local minima. The resulting total number of evaluated topologies for the FT3 case is reported in Table II, leading to total simulation times of 0.09, 0.25, 0.55, 1.48, and 3.60 h for $N_{elem} = 4, 5, 6, 7$, and 8 elements, respectively. The reflection coefficients of the fundamental, second, and third harmonics shown in Fig. 10 are analyzed, where the 50 best solutions are displayed, and the configuration with the lowest cost function is highlighted. The fundamental is shown in the left column, the second harmonic in the center, and the third harmonic in the right column. In all cases, a trend can be observed for the second harmonic to converge toward an open-circuit condition on the SC. Both the second harmonic (purple) and the third harmonic (maroon) closely follow the unit circle of the SC for most configurations. However, as observed in Fig. 10(i) and (o), increasing the number of elements causes the third harmonic to deviate from the unit circle, mainly due to the periodic behavior of the TLs.

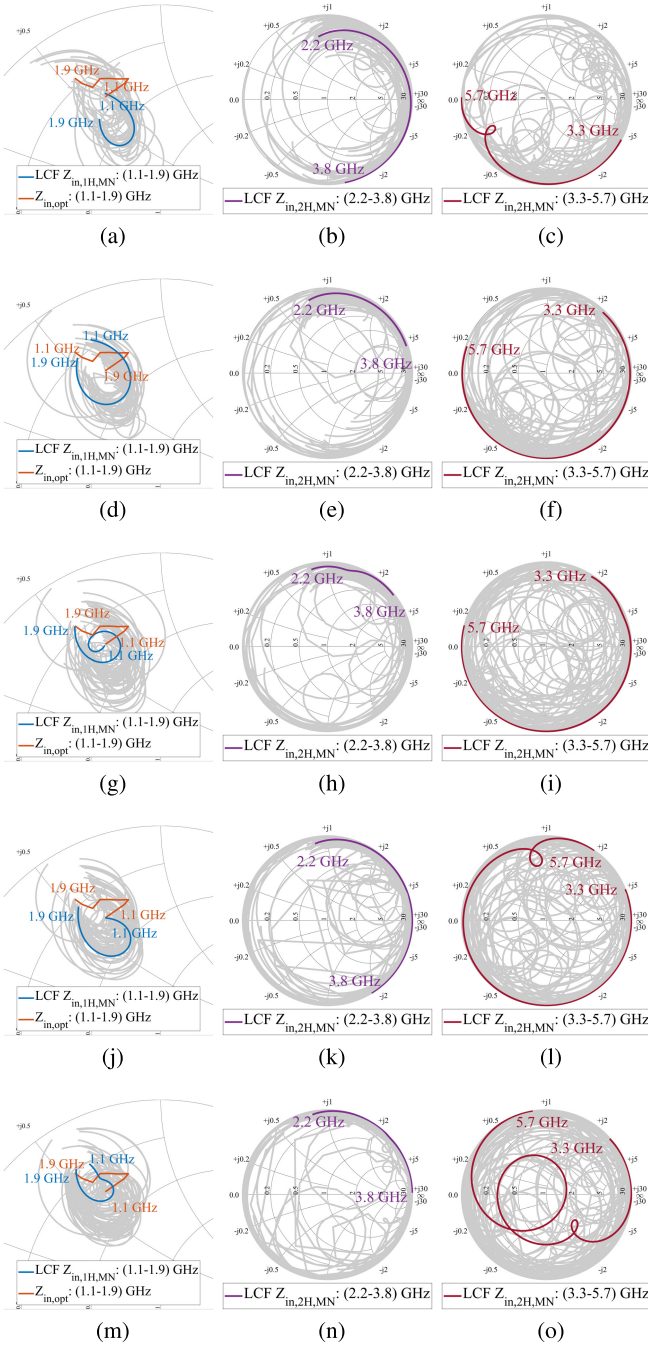


Fig. 10. Top 50 solutions, with the lower cost function (LCF) highlighted in color, for $N_{elem} = 4$: (a) fundamental, (b) second harmonic, and (c) third harmonic; $N_{elem} = 5$: (d) fundamental, (e) second harmonic, and (f) third harmonic; $N_{elem} = 6$: (g) fundamental, (h) second harmonic, and (i) third harmonic; $N_{elem} = 7$: (j) fundamental, (k) second harmonic, and (l) third harmonic; $N_{elem} = 8$: (m) fundamental, (n) second harmonic, and (o) third harmonic; evaluated from 1.1 to 1.9 GHz.

The large-signal simulations of the different MNs are shown in Fig. 11. It is verified that the solution associated with the lowest cost function exhibits the best performance in terms of PAE flatness over the bandwidth. All simulations are carried out under identical conditions, with a constant input power of $P_{in} = 29$ dBm, bias voltages of $V_{GS} = -2.9$ V and $V_{DS} = 28$ V, and a quiescent current of $I_q \approx 48.22$ mA.

From Fig. 11, it can be observed that increasing the number of elements in the MN does not necessarily improve the PAE

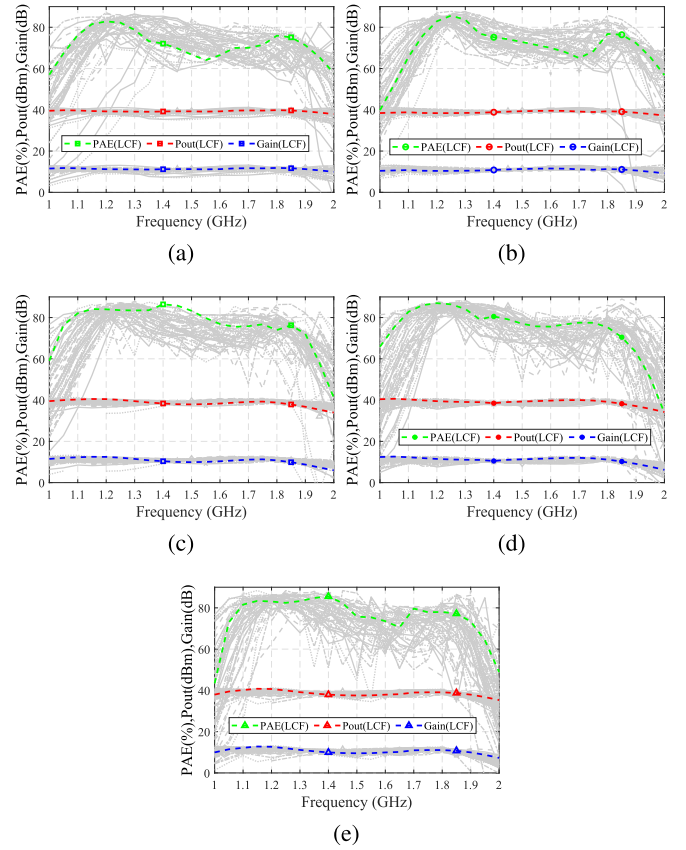


Fig. 11. PAE, output power, and gain of the top 50 topologies for $N_{elem} =$ (a) 4, (b) 5, (c) 6, (d) 7, and (e) 8.

performance over the bandwidth. In Fig. 11(a) and (b), a slight bulge appears at the center of the band, which is mitigated by adding one more element, as shown in Fig. 11(c). However, when comparing the 6-element case with the 7-element case in Fig. 11(d), no significant improvement is observed; in fact, the performance slightly degrades. In the 8-element case shown in Fig. 11(e), pronounced notches begin to appear, including one around 1.65 GHz, whereas the 6-element configuration exhibits a smoother response. Consequently, adding more elements is not beneficial, as the increased number of stubs introduces resonances that result in excessive ripple across the bandwidth. From visual inspection, it can be observed that the six-element MN shown in Fig. 11(c) achieves the widest bandwidth and exhibits shallower efficiency notches, resulting in improved PAE flatness across the band.

Although the operation class is not explicitly enforced, the results indicate that the second harmonic is more suitable for an open-circuit condition on the SC, while the third harmonic tends toward the short-circuit region. In this case, the obtained solution can be approximated to an inverse Class F operation, as shown in Fig. 12. Forcing the second harmonic to a short-circuit condition would require a large phase rotation from the optimum fundamental impedance, which is difficult to achieve with passive networks.

G. Topology Analysis

A useful exercise is to analyze the elements that constitute the topology. In this case, the 6-element solution shown in

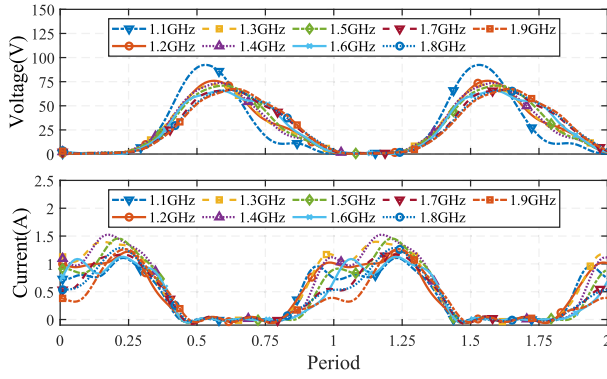


Fig. 12. Waveform at the internal plane of the current source for the best case of the 6-element MN.

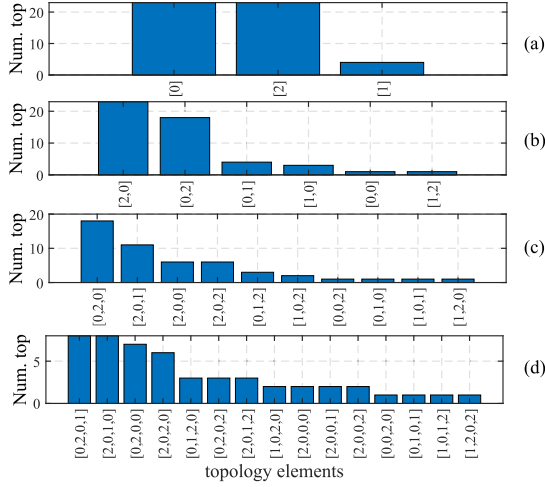


Fig. 13. First N elements for $N =$ (a) 1, (b) 2, (c) 3, and (d) 4, where an STL is represented by 0, an SOS TL by 1, and an SSS TL by 2.

Fig. 11(c) is selected, as it provides the best tradeoff between PAE flatness and a reduced number of elements. Fig. 13 presents a histogram of the 50 best topologies, showing the frequency of occurrence of the different configurations for the first N elements of the topology, for $N = 1, 2, 3$, and 4.

A statistical analysis of the solution convergence can be performed, since the simulations are carried out in the ADS using the large-signal transistor model. From Fig. 13(a) and (b), it can be observed that the first elements of the OMN are predominantly either an STL or a short-circuited shunt stub. This behavior is directly related to the location of the optimum impedances and to the phase shift required from the MN. A shunt stub connected to the ground is always required to provide DC biasing, since at $f = 1$ Hz, the transfer function must present a short-circuit condition. Consequently, the reflection coefficient $\Gamma_{opt,50\Omega}$ must undergo a phase transition from 180° to the phase corresponding to the optimum impedance. The farther the optimum impedance lies toward the short-circuit region of the SC, the larger the required phase rotation becomes, and therefore the more difficult the impedance matching problem is.

This analysis provides insights into which MN configurations are most suitable based on the number of elements and the impedance distribution on the SC. Moreover, it enables a robustness assessment by identifying the topologies that converge most consistently. This generative tool facilitates the

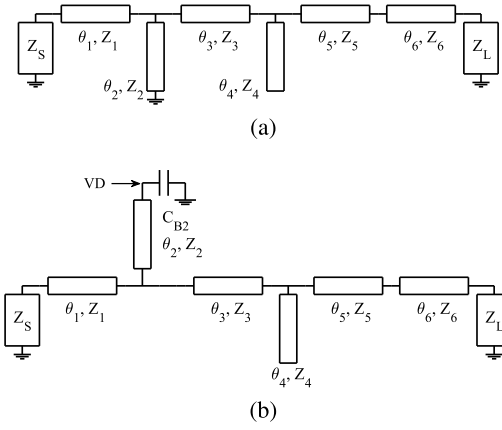


Fig. 14. (a) Proposed OMN topology resulting from the algorithm and (b) modified, extended, proposed OMN.

exploration of new and potentially complex MN configurations [5] and establishes a good seed for layout implementation.

H. Implementation of the OMN

To demonstrate the proposed approach, the MACOM CG2H40010F transistor is used for the physical implementation. The proposed OMN topology is shown in Fig. 14, and the corresponding element values are summarized in Table III, including the electrical lengths and their direct conversion into microstrip lines obtained by the algorithm. The topology, depicted in Fig. 14(a), consists of six elements, including a short-circuit stub. In the automatic search algorithm, at least one short-circuit stub is required to implement the biasing. This stub is replaced by an open-circuit stub with a series capacitor to ground, using two muRata capacitors of $1 \mu\text{F}$ each to create a virtual short-circuit and provide bias to the transistor, as illustrated in Fig. 14(b). A realistic capacitor model is employed instead of an ideal capacitance, since the latter would be overly conservative and unable to capture the resonant behavior associated with practical lumped elements. Using a realistic model allows a more accurate representation of parasitic effects and frequency-dependent behavior.

Fig. 15 compares the ideal response without biasing [Fig. 14(a)], the response including the bias network [Fig. 14(b)], and the final layout EM simulation [Fig. 15(c)]. It can be observed that the fundamental and second-harmonic reflection coefficients remain nearly unchanged, while a slight deviation occurs for the third harmonic, which moves away from the unit circle. This difference is mainly attributed to the replacement of an ideal ground with capacitors exhibiting a finite quality factor. The EM response of the layout follows the same trend, with minor degradation due to TL width discontinuities and finite connection areas.

I. Input MN

In this case, the procedure used to design the IMN is the same as that applied to the OMN, with a few specific considerations. All candidate topologies are evaluated under identical optimization conditions, and the topology exhibiting the flattest in-band response is selected. The IMN topology is shown in Fig. 16. The biasing components Z_6 , θ_6 , and

TABLE III
VALUES OF ELEMENTS OF THE OMN AT $f_{\text{design}} = 1.5$ GHz

MN	θ_1	Z_1	θ_2	Z_2	C_2	θ_3	Z_3	θ_4	Z_4	θ_5	Z_5	R_6	θ_6	Z_6	R_7	C_7	θ_8	Z_8
OMN	15.31	79.68	18.03	55.59	2x1uF	31.55	36.98	24.34	20.00	96.12	74.27	-	99.35	80.00	-	-	-	-
IMN	53.82	29.98	21.68	32.42	-	17.29	28.42	42.81	21.86	22.08	51.86	50	100	90	10	3.3 pF	7.22	33.82
MN	W_1	L_1	W_2	L_2	C_2	W_3	L_3	W_4	L_4	W_5	L_5	R_6	W_6	L_6	R_7	C_7	W_8	L_8
OMN	0.87	4.10	1.6	7.4	2x1uF	3.12	11.17	3.11	11.46	0.87	29.53	-	0.89	31.04	-	-	-	-
IMN	3.89	17.76	3.49	7.18	-	4.17	5.68	5.84	13.87	1.73	7.54	-	0.64	34.89	10	3.3 pF	3.3	2.4

TABLE IV
STATE-OF-THE-ART

Ref.	BW [GHz]	FBW [%]	DE [%]	Pout [dBm]	Gain [dB]	Class
[21]	1.2–3.6	100	63–73	40.5–42.7	10.5–12.8	EFJ
[22]	0.9–2.2	83	63–89	40–43	10–13	E
[23]	0.9–2.3	87	57–88	40.8–44.8	7.5–13	E
[24]	1–1.9	62	64–79	39–42	9–12	Adaptive
[25]	1.4–2.6	60	55–65	39–40	9.5–10.5	J
[26]	1.7–2.7	63	63–73	39.7–41.5	9.5	E
[27]	1.25–1.45	63	63.3–77.5	40.6–42.6	12.4–14.5	E
[28]	1.45–2.45	51	70–81	40.1–42.2	10.4–12.6	F
T.W.	1.1–1.9	53	72.3–84	39.6–42.4	10.6–14.4	F⁻¹

FBW: Fractional Bandwidth

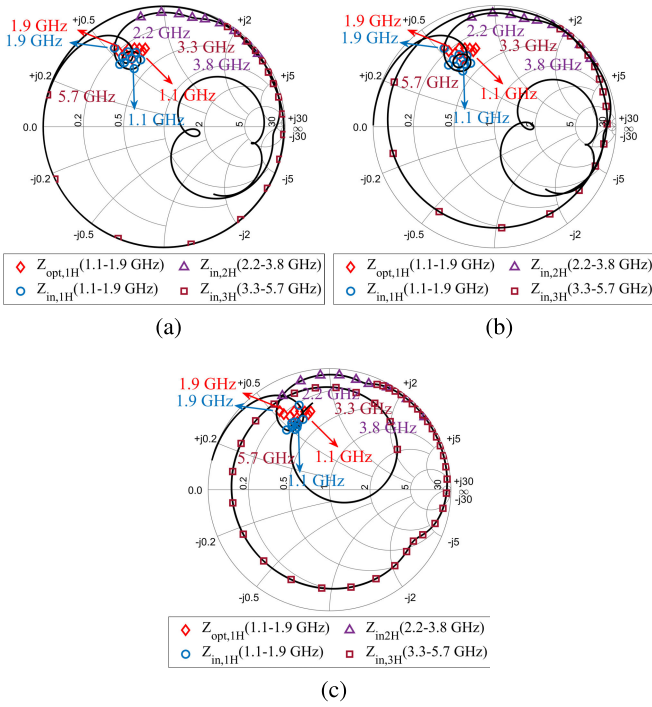


Fig. 15. Input reflection coefficient of (a) OMN resulting from the algorithm, (b) extended OMN including all elements, and (c) OMN EM simulation of the complete layout.

C_6 are treated as a single block, while R_7 , C_7 , θ_6 , and Z_8 are fixed blocks whose positions and values are not subject to optimization. Transmission line 8 is mandatory to ensure proper soldering to the transistor pads. Consequently, only the first five elements of the network are optimized. This approach is adopted because it provides improved stability from a circuit perspective. The gate bias is implemented through a high-impedance TL and a 50- Ω resistor.

The corresponding electrical lengths and their direct conversion into microstrip lines are summarized in Table III. Fig. 17(a) illustrates the reflection coefficient at the output

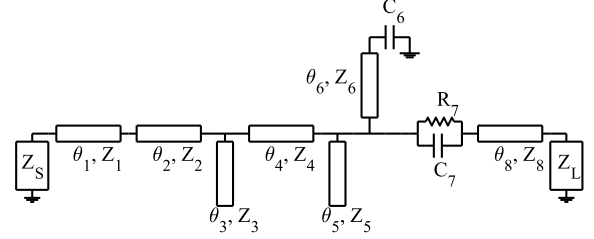


Fig. 16. Schematic of the IMN resulting from the algorithm, with element values given in Table III.

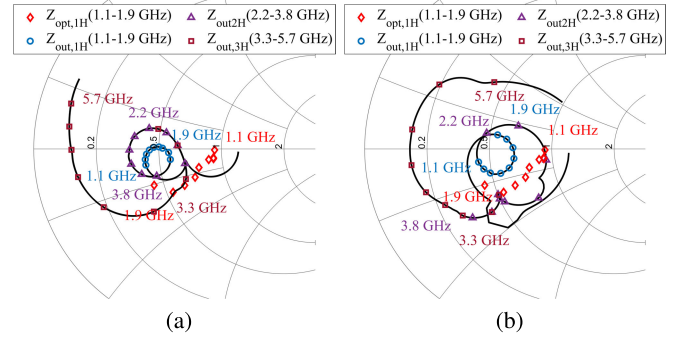


Fig. 17. Output reflection coefficient of the IMN (a) resulting from the algorithm and (b) EM simulation of the complete MN.

of the IMN, and Fig. 17(b) shows the full EM simulation of the layout, for the fundamental frequency (blue circles), the second harmonic (purple triangles), and the third harmonic (maroon squares). The optimal impedances for the fundamental are indicated by red diamonds and are obtained from source—pull simulations once the OMN is designed and connected to the transistor. In this case, the optimal impedance trajectory exhibits Foster behavior, which facilitates simultaneous matching of the first three harmonics. Some minor discrepancies are observed between the ideal microstrip lines. The use of real capacitor models near the gate requires adjustment due to lumped-element resonances and impedance displacement. Furthermore, since the input MN ensures stability, additional fine-tuning may be required.

IV. EXPERIMENTAL VALIDATION

The experimental validation is carried out using the values reported in Table III. These ideal values are transformed into microstrip transmission (Table III) lines and subsequently fine-tuned to achieve the best performance in terms of PAE over the frequency band from 1.1 to 1.9 GHz.

The ideal layout and the fabricated prototype are shown in Fig. 18. Once the parameters are obtained through the algorithm, they are transferred to the layout stage and reoptimized due to the connection nodes of the TLs, for maximum PAE. Although some differences exist, the EM optimization

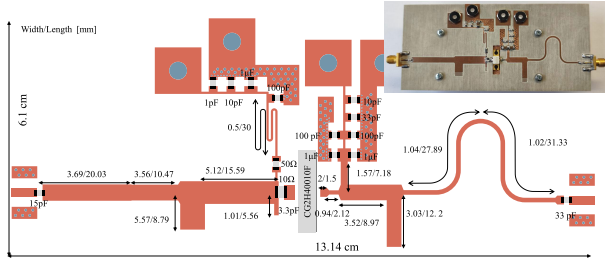


Fig. 18. Layout and manufactured prototype in RO4003C $T = 0.813$ mm.

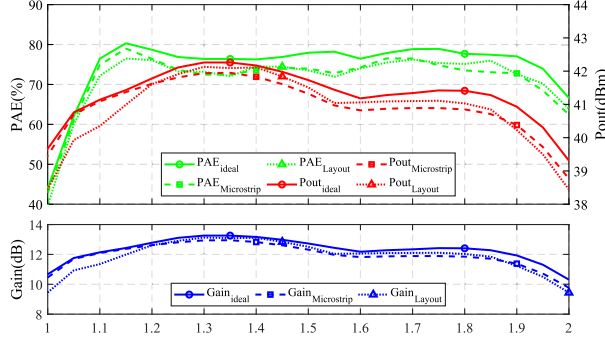


Fig. 19. Comparison between ideal TLs, microstrip lines, and layout (EM) for the PAE, output power, and gain.

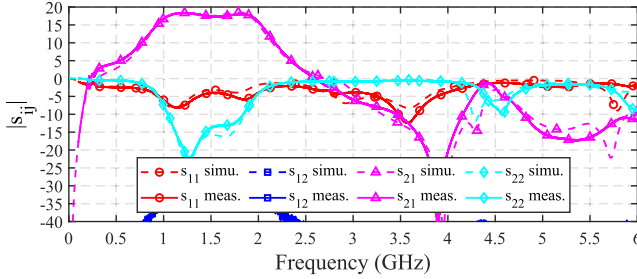


Fig. 20. Comparison of s-parameters of the simulated and measured manufactured device.

time remains short because the initial design provides a good seed. A comparison among the ideal TLs, their microstrip implementations, and the final EM-simulated layout is shown in Fig. 19. It can be observed that all responses follow the same trend, with some degradation due to unavoidable losses, TL discontinuities, and EM effects. Both designs are implemented on a Rogers RO4003C substrate with a thickness of $h = 0.813$ mm, and all reactive lumped components are sourced from Murata. DC-block capacitors of 15 pF at the input and 33 pF at the output are employed. These values are chosen to be sufficiently large to minimize their impact on the input and output MNs while ensuring their self-resonant frequencies lie outside the operating band.

The bias conditions are set to $V_{DS} = 28$ V and $V_{GS} = -2.9$ V, corresponding to a drain current of $I_D = 48.22$ mA. The final layout of the structure and the fabricated prototype are depicted in Fig. 18. The overall dimensions of the prototype are 131.3×46.7 mm. The meandered TL sections in the OMN are introduced solely to reduce the physical footprint of the circuit and do not affect its electrical functionality. The small-signal parameters are shown in Fig. 20, where the measured results are represented by solid lines and the simulated results

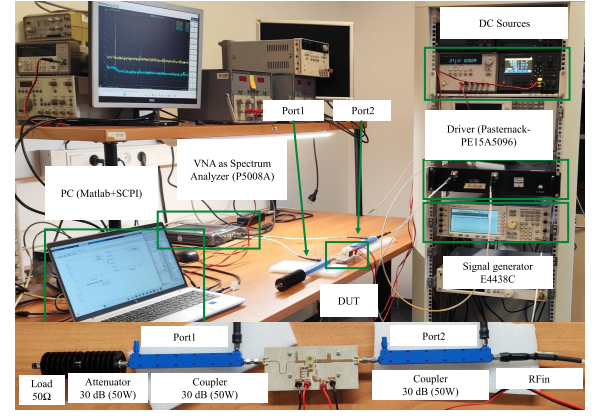


Fig. 21. Large-signal measurement setup with a double-receptor spectrum analyzer.

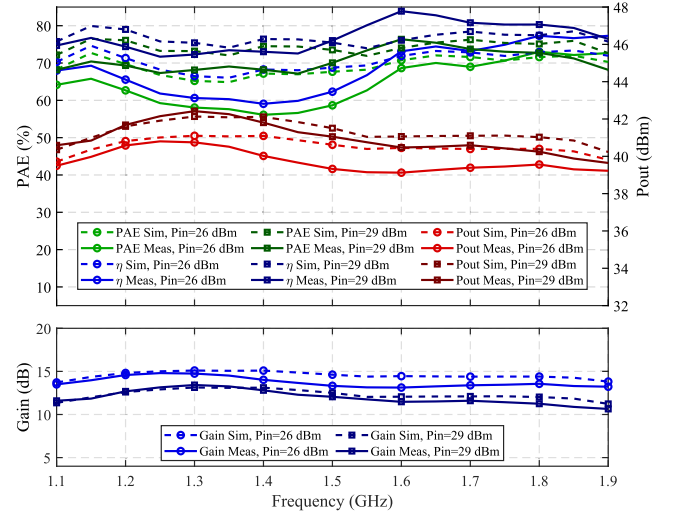


Fig. 22. Large-signal comparison between simulation and measurements of output power, PAE, and gain.

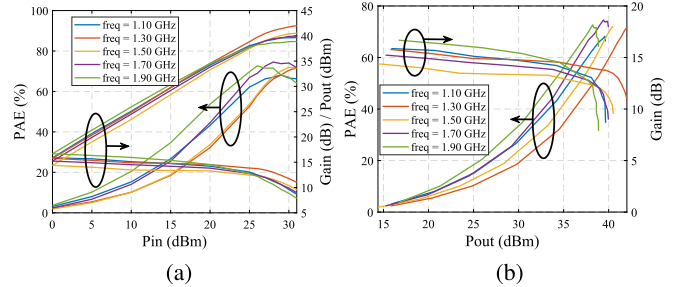


Fig. 23. Measured large-signal parameters: (a) with respect to the input power and (b) with respect to the output power.

by dashed lines. An excellent agreement can be observed between the measurements and the simulations.

The measurement setup for the large-signal characterization is shown in Fig. 21, where two directional couplers are used at the input and output of the amplifier to monitor the input and output power of the DUT using a dual-channel spectrum analyzer. This configuration avoids disturbing the main signal path and ensures that the impedance seen by the device remains as designed. The large-signal parameters are depicted in Fig. 22, where the dotted lines represent the large-signal simulation and the solid lines correspond to the measurement

results. Both the saturation power and the 3-dB input back-off point are 29 and 26 dBm, respectively. At saturation, the amplifier achieves a bandwidth from 1.1 to 1.9 GHz, with a drain efficiency (DE) greater than 70%, gain ranging from 10.6 to 13.4 dB, and output power between 39.6 and 42.4 dBm. In Fig. 23, the PAE, gain, and P_{out} are shown under large-signal conditions as a function of the input power, while the PAE and gain are also presented as a function of the output power. Table IV presents the comparison within the state of the art, showing that the proposed amplifier achieves performance comparable to that of previously reported amplifiers.

V. CONCLUSION

This article has presented an algorithmic framework for the automatic generation and optimization of MN topologies in PA design. The proposed method enables systematic exploration of feasible solutions while addressing key challenges such as non-Foster impedance behavior and harmonic overlap. By combining topology generation and filtering with a unified cost-function optimization, the algorithm efficiently evaluates a large number of candidates and provides a global view of the tradeoffs between efficiency, bandwidth, and complexity. Experimental results of a GaN-based PA operating from 1.1 to 1.9 GHz validate the approach, showing high efficiency and good agreement between simulations and measurements. The results demonstrate that optimal performance is not necessarily achieved by increasing network complexity, highlighting the importance of topology selection. The proposed method provides a reliable starting point for layout optimization, significantly reducing overall design time.

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